

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4067B**

### **MSI**

## **16-channel analogue multiplexer/demultiplexer**

Product specification  
File under Integrated Circuits, IC04

January 1995

# 16-channel analogue multiplexer/demultiplexer

# HEF4067B MSI

### DESCRIPTION

The HEF4067B is a 16-channel analogue multiplexer/demultiplexer with four address inputs ( $A_0$  to  $A_3$ ), an active LOW enable input ( $\bar{E}$ ), sixteen independent inputs/outputs ( $Y_0$  to  $Y_{15}$ ) and a common input/output ( $Z$ ).

The device contains sixteen bidirectional analogue switches, each with one side connected to an independent input/output ( $Y_0$  to  $Y_{15}$ ) and the other side connected to the common input/output ( $Z$ ).

With  $\bar{E}$  LOW, one of the sixteen switches is selected (low impedance ON-state) by  $A_0$  to  $A_3$ . All unselected switches are in the high impedance OFF-state. With  $\bar{E}$  HIGH all switches are in the high impedance OFF-state, independent of  $A_0$  to  $A_3$ .

The analogue inputs/outputs ( $Y_0$  to  $Y_{15}$  and  $Z$ ) can swing between  $V_{DD}$  as a positive limit and  $V_{SS}$  as a negative limit.  $V_{DD}$  to  $V_{SS}$  may not exceed 15 V.

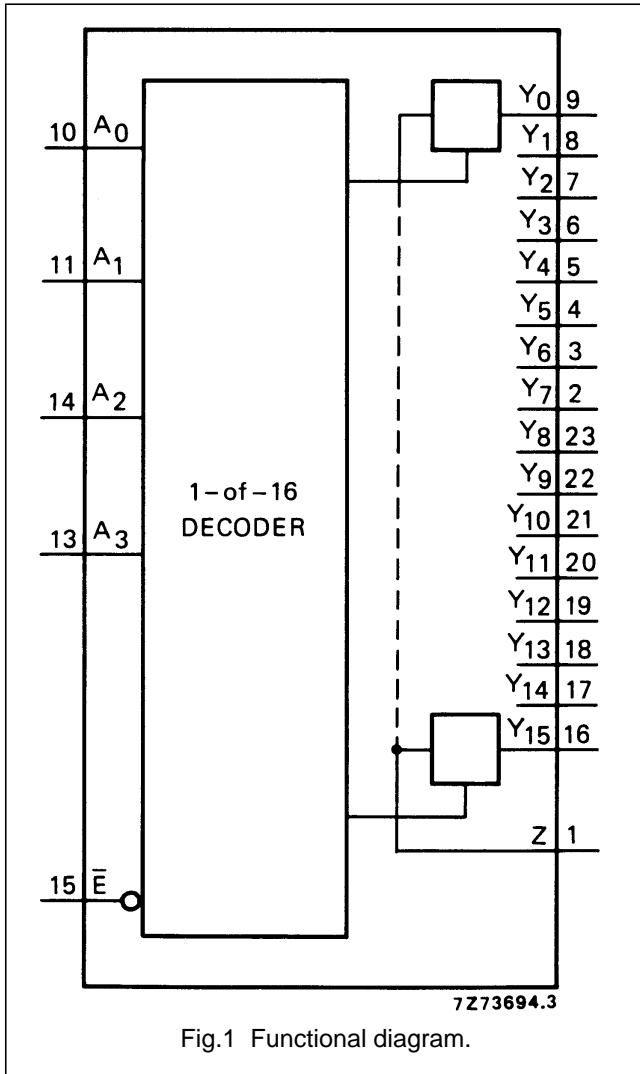


Fig.1 Functional diagram.

### FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

HEF4067BP(N): 24-lead DIL; plastic (SOT101-1)

HEF4067BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)

HEF4067BT(D): 24-lead SO; plastic (SOT137-1)

( ): Package Designator North America

### PINNING

- $Y_0$  to  $Y_{15}$  independent inputs/outputs
- $A_0$  to  $A_3$  address inputs
- $\bar{E}$  enable input (active LOW)
- $Z$  common input/output

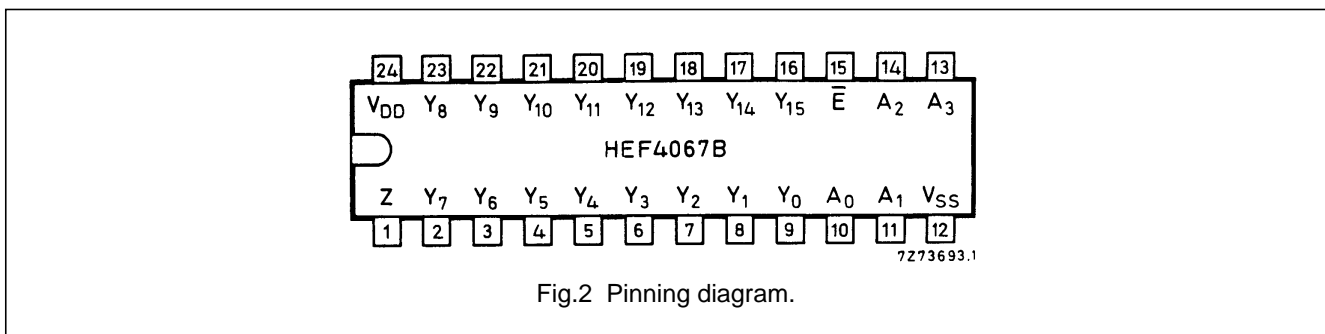


Fig.2 Pinning diagram.

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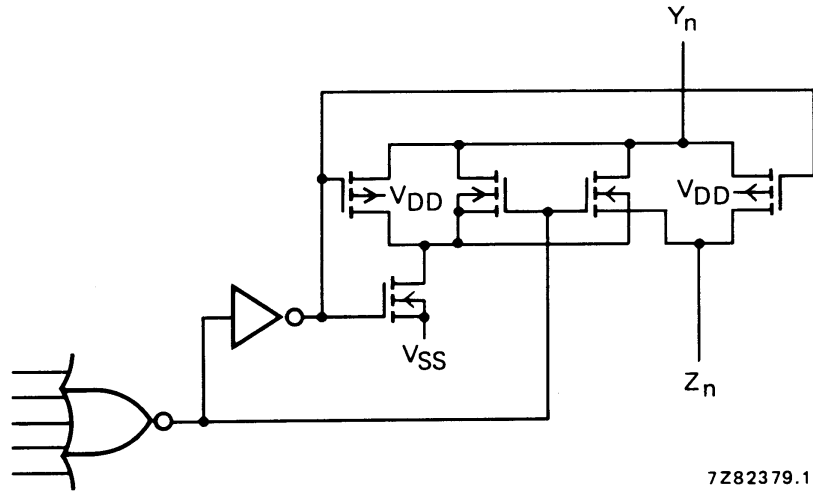


Fig.3 Schematic diagram (one switch).

FUNCTION TABLE

INPUTS					CHANNEL
$\bar{E}$	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON
L	L	L	L	L	Y <sub>0</sub> - Z
L	L	L	L	H	Y <sub>1</sub> - Z
L	L	L	H	L	Y <sub>2</sub> - Z
L	L	L	H	H	Y <sub>3</sub> - Z
L	L	H	L	L	Y <sub>4</sub> - Z
L	L	H	L	H	Y <sub>5</sub> - Z
L	L	H	H	L	Y <sub>6</sub> - Z
L	L	H	H	H	Y <sub>7</sub> - Z
L	H	L	L	L	Y <sub>8</sub> - Z
L	H	L	L	H	Y <sub>9</sub> - Z
L	H	L	H	L	Y <sub>10</sub> - Z
L	H	L	H	H	Y <sub>11</sub> - Z
L	H	H	L	L	Y <sub>12</sub> - Z
L	H	H	L	H	Y <sub>13</sub> - Z
L	H	H	H	L	Y <sub>14</sub> - Z
L	H	H	H	H	Y <sub>15</sub> - Z
H	X	X	X	X	none

Note

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial

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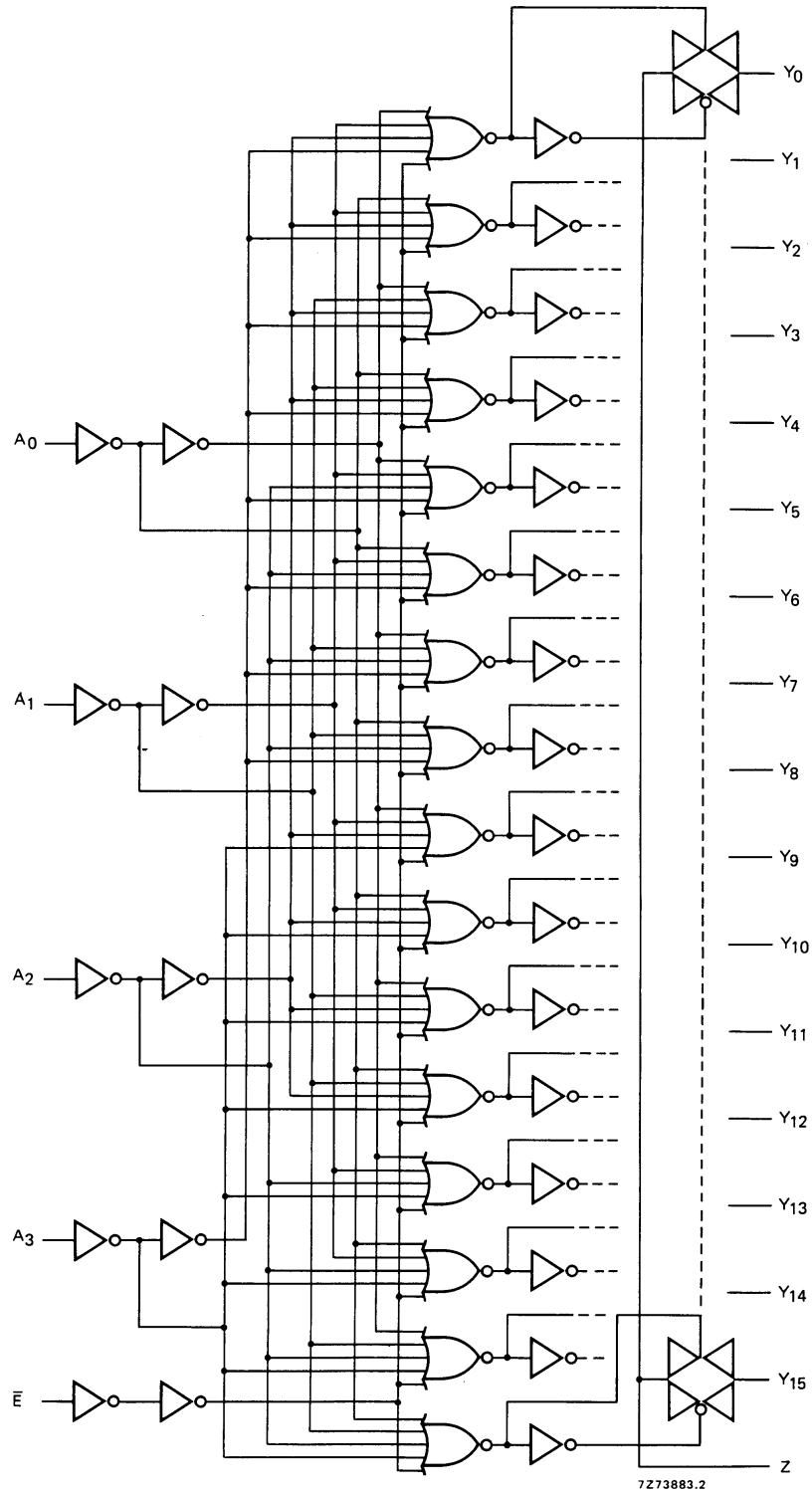


Fig.4 Logic diagram.

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DC CHARACTERISTICS

T<sub>amb</sub> = 25 °C

	V <sub>DD</sub> V	SYMBOL	TYP.	MAX.		CONDITIONS
ON resistance	5	R <sub>ON</sub>	350	2500	Ω	V <sub>is</sub> = V <sub>SS</sub> to V <sub>DD</sub> see Fig.5
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R <sub>ON</sub>	115	340	Ω	V <sub>is</sub> = V <sub>SS</sub> see Fig.5
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R <sub>ON</sub>	120	365	Ω	V <sub>is</sub> = V <sub>DD</sub> see Fig.5
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR <sub>ON</sub>	25	–	Ω	V <sub>is</sub> = V <sub>SS</sub> to V <sub>DD</sub> see Fig.5
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I <sub>oZZ</sub>	–	–	nA	$\bar{E}$ at V <sub>DD</sub>
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I <sub>oZY</sub>	–	–	nA	$\bar{E}$ at V <sub>SS</sub>
	10		–	–	nA	
	15		–	200	nA	

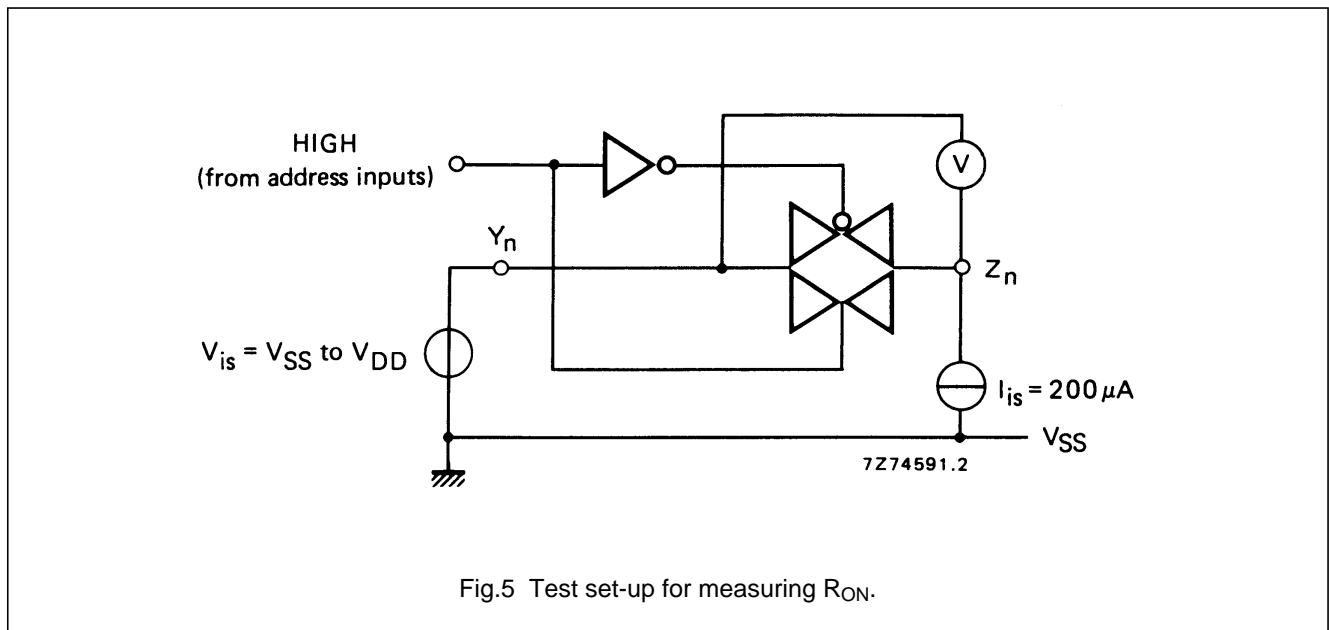
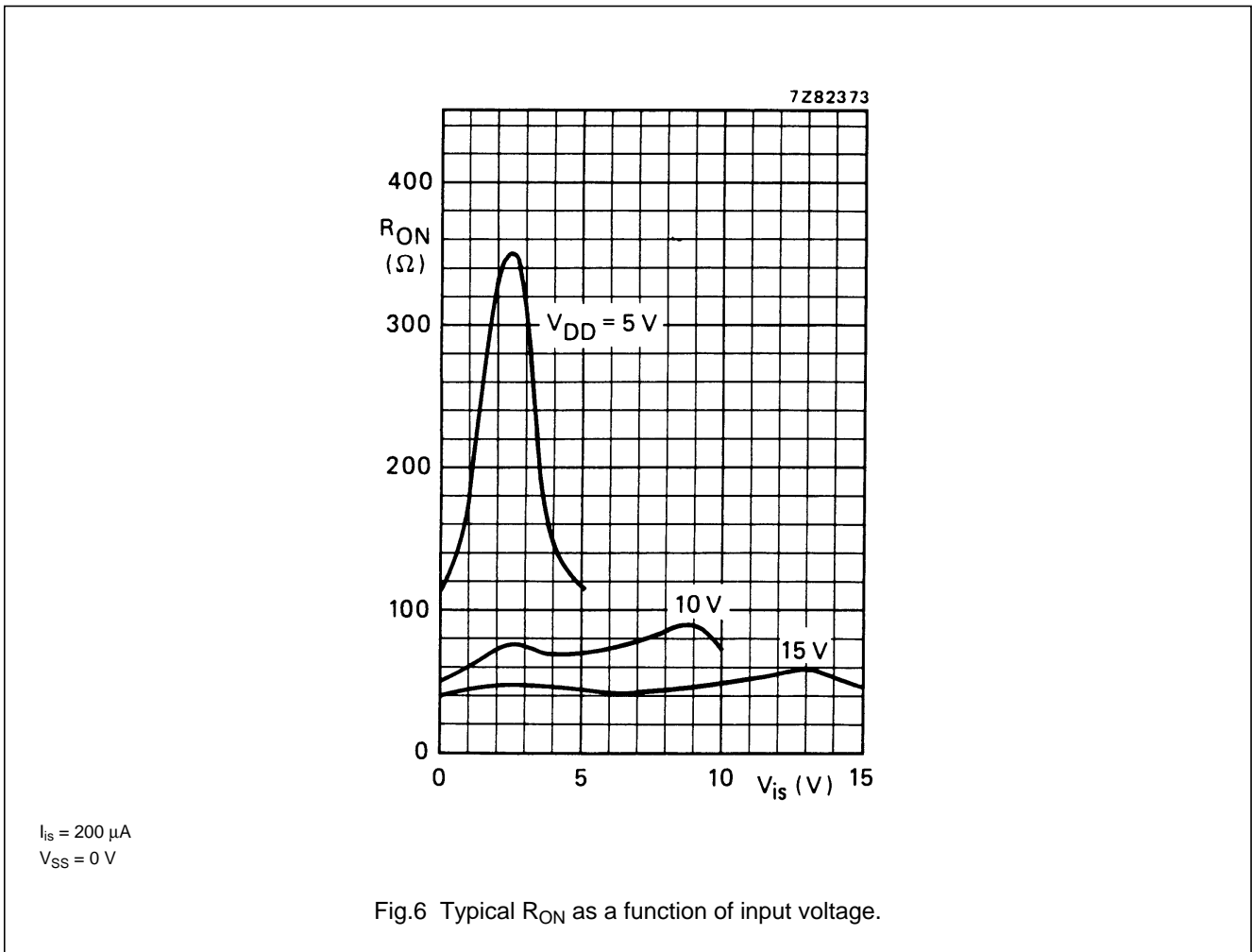


Fig.5 Test set-up for measuring R<sub>ON</sub>.

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**NOTE**

To avoid drawing  $V_{DD}$  current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no  $V_{DD}$  current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed  $V_{DD}$  or  $V_{SS}$ .

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### AC CHARACTERISTICS

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C; input transition times  $\leq 20$  ns

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5	$1\ 100 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$5\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$13\ 300 f_i + \sum (f_o C_L) \times V_{DD}^2$	

### AC CHARACTERISTICS <sup>(1), (2)</sup>

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	TYP.	MAX.						
Propagation delays	5	$t_{PHL}$	30	60	ns	note 3				
							HIGH to LOW	15	25	ns
	5	25	50	ns						
					LOW to HIGH	10	20	ns		
									15	20
	5	190	380	ns						
					$A_n \rightarrow V_{OS}$	HIGH to LOW	70	145		
									10	70
	15	100	ns							
				5	175	345	ns			
								LOW to HIGH	70	140
10	50	100	ns							
				15	50	100	ns			
								Output disable times	5	$t_{PHZ}$
HIGH	140	280	ns							
				15	130	260	ns			
									5	215
LOW	180	355	ns							
				10	170	340	ns			
								15	170	340
Output enable times	5	$t_{PZH}$	155							
				HIGH	70	135	ns			
								15	50	100
	5	170	340							
				LOW	70	140	ns			
								10	50	100
15	50	100	ns							

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### AC CHARACTERISTICS

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	TYP.	MAX.	
Distortion, sine-wave response	5		0,25	%	note 6
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 8
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 9
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 10
	10		40	MHz	
	15		70	MHz	

### Notes

- $V_{is}$  is the input voltage at a Y or Z terminal, whichever is assigned as input.
- $V_{os}$  is the output voltage at a Y or Z terminal, whichever is assigned as output.
- $R_L = 10$  k $\Omega$  to  $V_{SS}$ ;  $C_L = 50$  pF to  $V_{SS}$ ;  $\bar{E} = V_{SS}$ ;  $V_{is} = V_{DD}$  (square-wave); see Fig.7.
- $R_L = 10$  k $\Omega$ ;  $C_L = 50$  pF to  $V_{SS}$ ;  $\bar{E} = V_{SS}$ ;  $A_n = V_{DD}$  (square-wave);  $V_{is} = V_{DD}$  and  $R_L$  to  $V_{SS}$  for  $t_{PLH}$ ;  $V_{is} = V_{SS}$  and  $R_L$  to  $V_{DD}$  for  $t_{PHL}$ ; see Fig.7.
- $R_L = 10$  k $\Omega$ ;  $C_L = 50$  pF to  $V_{SS}$ ;  $\bar{E} = V_{DD}$  (square-wave);  
 $V_{is} = V_{DD}$  and  $R_L$  to  $V_{SS}$  for  $t_{PHZ}$  and  $t_{PZH}$ ;  
 $V_{is} = V_{SS}$  and  $R_L$  to  $V_{DD}$  for  $t_{PLZ}$  and  $t_{PZL}$ ; see Fig.7.
- $R_L = 10$  k $\Omega$ ;  $C_L = 15$  pF; channel ON;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );  
 $f_{is} = 1$  kHz; see Fig.8.
- $R_L = 1$  k $\Omega$ ;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );

$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB; see Fig.9.}$$

- $R_L = 10$  k $\Omega$  to  $V_{SS}$ ;  $C_L = 15$  pF to  $V_{SS}$ ;  $\bar{E}$  or  $A_n = V_{DD}$  (square-wave); crosstalk is  $|V_{os}|$  (peak value); see Fig.7.

- $R_L = 1$  k $\Omega$ ;  $C_L = 5$  pF; channel OFF;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );

$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB; see Fig.8.}$$

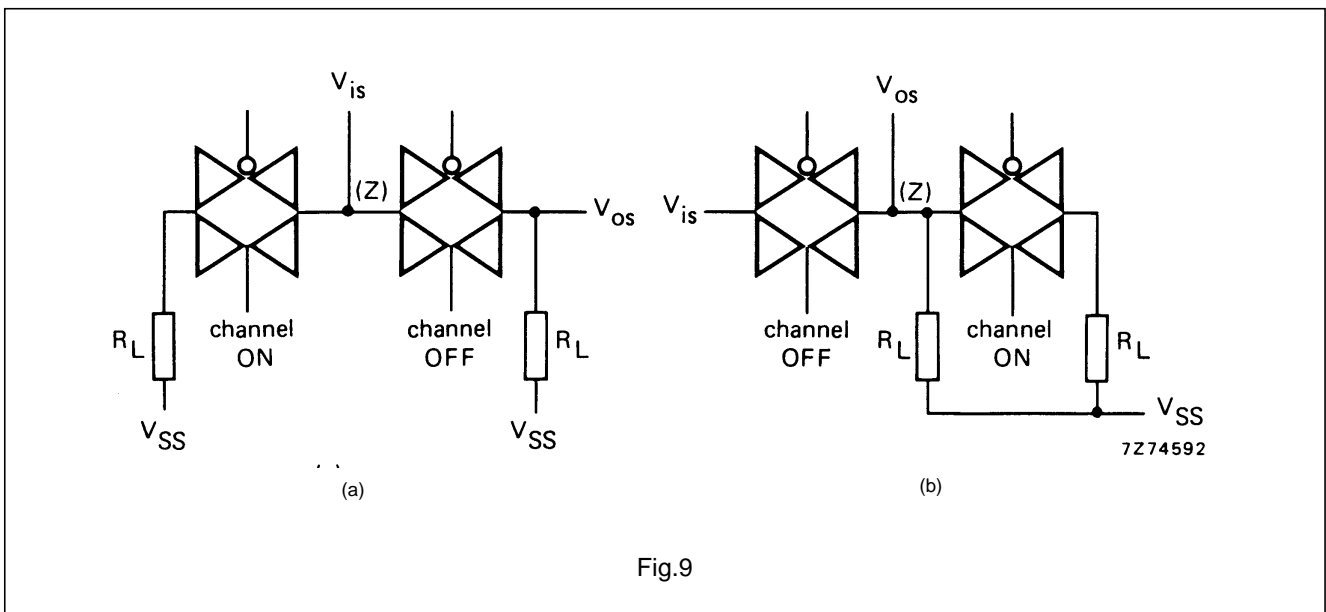
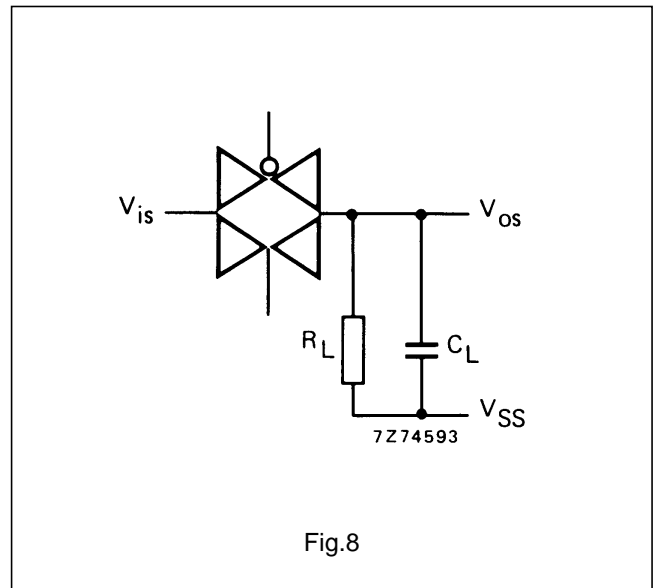
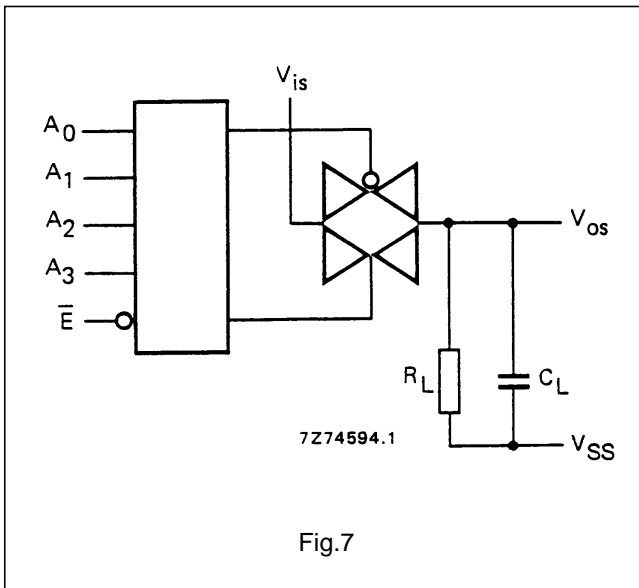
- $R_L = 1$  k $\Omega$ ;  $C_L = 5$  pF; channel ON;  $V_{is} = \frac{1}{2} V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2} V_{DD}$ );

$$20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB; see Fig.8.}$$



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**APPLICATION INFORMATION**

Some examples of applications for the HEF4067B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

**NOTE**

If break before make is needed, then it is necessary to use the enable input.