EL5100, EL5101, EL5300

200MHz Slew Enhanced VFA

FN7330
Rev 3.00
May 3, 2007

The EL5100, EL5101, and EL5300 represent high-speed voltage feedback amplifiers based on the current feedback amplifier architecture. This gives the typical high slew rate benefits of a CFA family along with the stability and ease of use associated with the VFA type architecture. This family is available in single, dual, and triple versions, with 200MHz, 400MHz, and 700MHz versions. This family operates on single 5V or ±5V supplies from minimum supply current. The EL5100 and EL5300 also feature an output enable function, which can be used to put the output in to a high-impedance mode. This enables the outputs of multiple amplifiers to be tied together for use in multiplexing applications.

Features

- Pb-free plus anneal available (RoHS compliant)
- Specified for 5V or ±5V applications
- Power-down to 17µA/amplifier
- -3dB bandwidth = 200MHz
- ±0.1dB bandwidth = 20MHz
- Low supply current = 2.5mA
- Slew rate = 2200V/µs
- Low offset voltage = 4mV max
- Output current = 100mA
- A_{VOL} = 1000
- Diff gain/phase = 0.08%/0.1°

Applications

- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

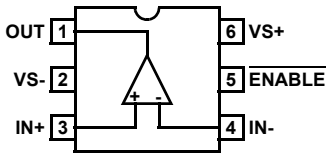
Ordering Information

PART NUMBER	PART MARKING	TAPE AND REEL	PACKAGE	PKG. DWG. #
EL5100IS	5100IS	-	8 Ld SOIC (150 mil)	MDP0027
EL5100IS-T7	5100IS	7”	8 Ld SOIC (150 mil)	MDP0027
EL5100IS-T13	5100IS	13”	8 Ld SOIC (150 mil)	MDP0027
EL5100ISZ (Note)	5100ISZ	-	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5100ISZ-T7 (Note)	5100ISZ	7”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5100ISZ-T13 (Note)	5100ISZ	13”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL5100IW-T7	y	7” (3k pcs)	6 Ld SOT-23	MDP0038
EL5100IW-T7A	y	7” (250 pcs)	6 Ld SOT-23	MDP0038
EL5101IW-T7	2	7” (3k pcs)	5 Ld SOT-23	MDP0038
EL5101IW-T7A	2	7” (250 pcs)	5 Ld SOT-23	MDP0038
EL5300IU	5300IU	-	16 Ld QSOP (150 mil)	MDP0040
EL5300IU-T7	5300IU	7”	16 Ld QSOP (150 mil)	MDP0040
EL5300IU-T13	5300IU	13”	16 Ld QSOP (150 mil)	MDP0040
EL5300IUZ (Note)	5300IUZ	-	16 Ld QSOP (150 mil) (Pb-free)	MDP0040
EL5300IUZ-T7 (Note)	5300IUZ	7”	16 Ld QSOP (150 mil) (Pb-free)	MDP0040
EL5300IUZ-T13 (Note)	5300IUZ	13”	16 Ld QSOP (150 mil) (Pb-free)	MDP0040

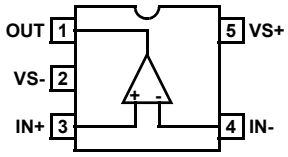
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

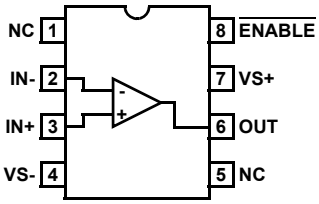
EL5100
(6 LD SOT-23)
TOP VIEW



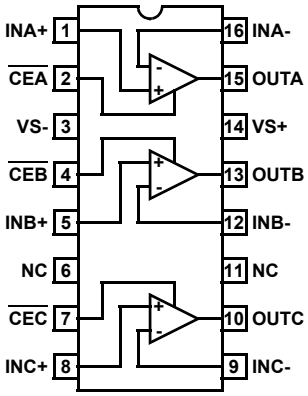
EL5101
(5 LD SOT-23)
TOP VIEW



EL5100
(8 LD SOIC)
TOP VIEW



EL5300
(16 LD QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- 13.2V
Input Voltage . . . . . .±V_S
Differential Input Voltage . . . . . .±4V
Maximum Output Current. 80mA
Maximum Slewrate from V_S+ to V_S- 1V/µs

Thermal Information

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature Range . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .+150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S = ±5V, GND = 0V, T_A = +25°C, V_{CM} = 0V, V_{OUT} = 0V, V_{ENABLE} = GND or OPEN, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage		-4	1	4	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		8		µV/°C
IB	Input Bias Current	V_{IN} = 0V	-6	2	6	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	-2.5	0.5	2.5	µA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		8		nA/°C
PSRR	Power Supply Rejection Ratio		70	90		dB
CMRR	Common Mode Rejection Ratio	V_{CM} from -3V to +3V	60	75		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	-3		+3	V
R_{IN}	Input Resistance	V_{IN} = -3V to +3V	0.7	1.2		MΩ
C_{IN}	Input Capacitance			1		pF
$I_{S,ON}$	Supply Current - Enabled	Per amplifier	2.1	2.5	2.9	mA
$I_{S,OFF}$	Supply Current - Shut Down	V_S+, per amplifier	-5	0	5	µA
		V_S-, per amplifier	5	17	25	µA
PSOR	Power Supply Operating Range		3.3		12	V
AVOL	Open Loop Gain	R_L = 1kΩ to GND, V_{OUT} from -2.5V to +2.5V	55	60		dB
V_{OP}	Positive Output Voltage Swing	R_L = 150Ω to GND	3.2	3.4		V
		R_L = 1kΩ to GND	3.6	3.8		V
V_{ON}	Negative Output Voltage Swing	R_L = 150Ω to GND		-3.4	-3.2	V
		R_L = 1kΩ to GND		-3.8	-3.6	V
I_{OUT}	Output Current	R_L = 10Ω to 0V	±60	±100		mA
V_{IH-EN}	ENABLE pin Voltage for Power Up		V_S+ -4			V
V_{IL-EN}	ENABLE pin Voltage for Shut Down				V_S+ -1	V
I_{EN}	Enable Pin Current	Enabled, V_{EN} = 0V	-1		1	µA
		Disabled, V_{EN} = 5V	5	17	25	µA

Closed Loop AC Electrical Specifications V_S = ±5V, T_A = 25°C, V_{ENABLE} = 0V, A_V = +1, R_F = 0Ω, R_L = 150Ω to GND, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth (V_{OUT} = 200mV_{P-P})	V_S = ±5V, A_V = 1, R_F = 0Ω	150	200		MHz
SR	Slew Rate	R_L = 100Ω, V_{OUT} = -3V to +3V, A_V = +2	1500	2200	4500	V/µs
t_R,t_F	Rise Time, Fall Time	±0.1V step		2.8		ns
OS	Overshoot	±0.1V step		10		%
t_{PD}	Propagation Delay	±0.1V step		3.2		ns
t_S	0.1% Settling Time	V_S = ±5V, R_L = 500Ω, A_V = 1, V_{OUT} = ±2.5V		20		ns
dG	Differential Gain	A_V = 2, R_L = 150Ω, V_{INDC} = -1 to +1V		0.08		%
dP	Differential Phase	A_V = 2, R_L = 150Ω, V_{INDC} = -1 to +1V		0.1		°
e_N	Input Noise Voltage	f = 10kHz		10		nV/√Hz
i_N	Input Noise Current	f = 10kHz		7		pA/√Hz
t_{DIS}	Disable Time			180		ns
t_{EN}	Enable Time			650		ns

Typical Performance Curves

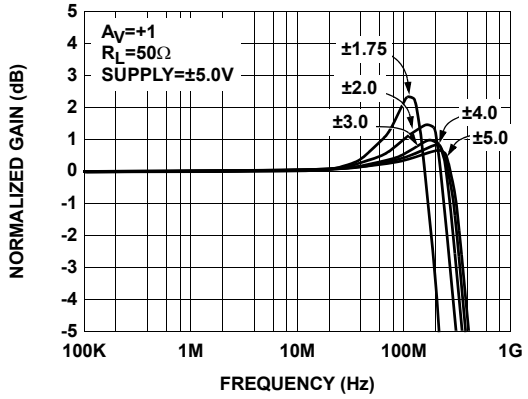


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS C_L

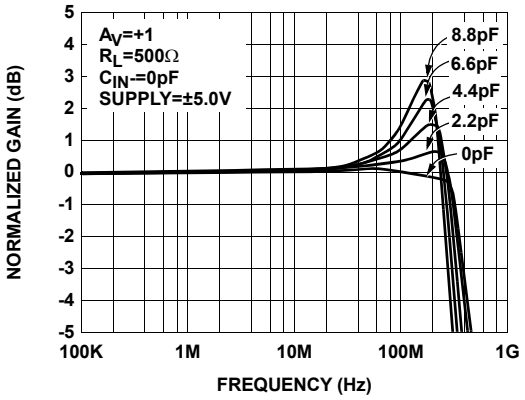


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS C_L

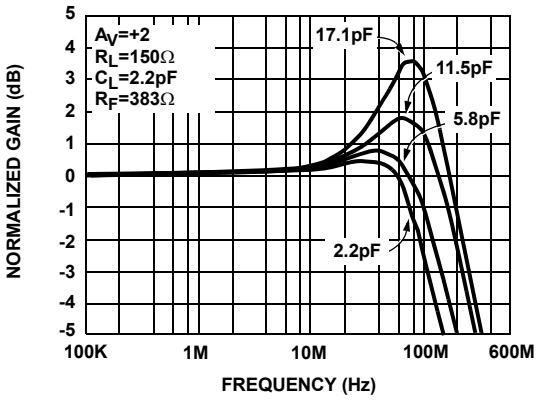


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS C_{IN}-

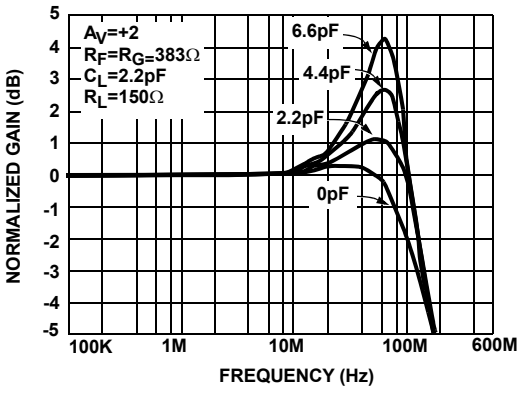


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS C_{IN}-

Typical Performance Curves (Continued)

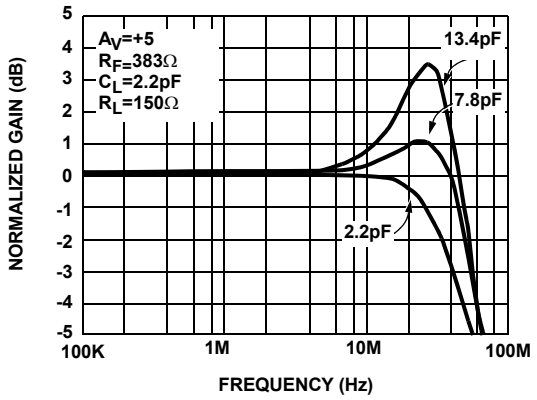


FIGURE 5. GAIN vs FREQUENCY FOR VARIOUS C_{IN} (-)

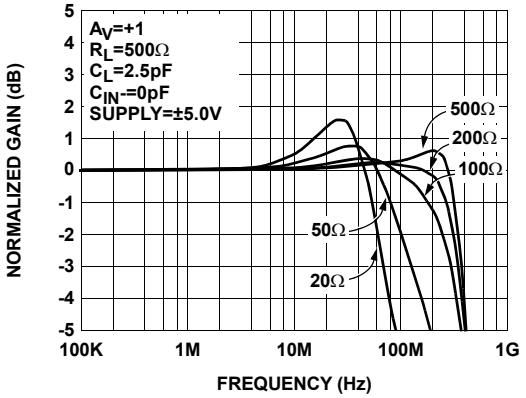


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS R_L

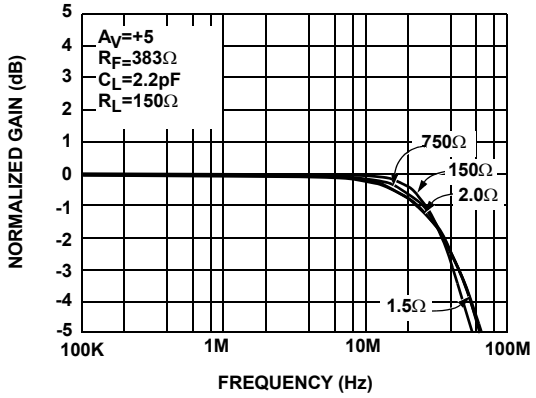


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS R_L

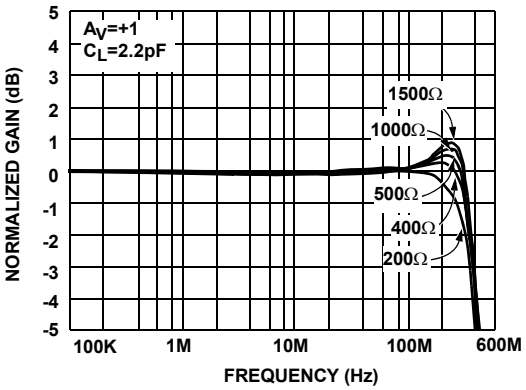


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_L

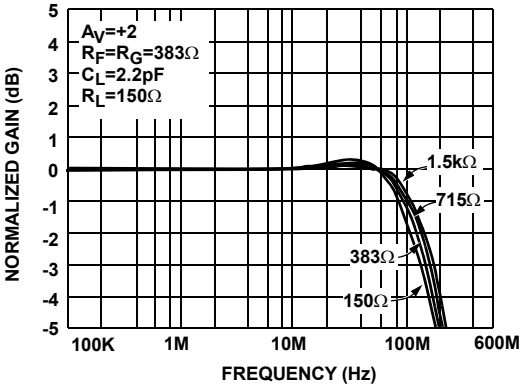


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_L

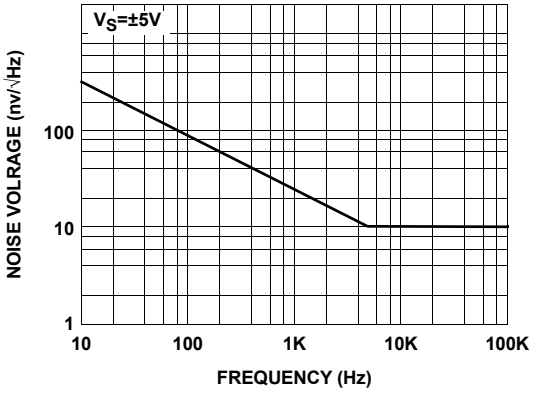


FIGURE 10. EQUIVALENT INPUT VOLTAGE NOISE vs FREQUENCY

Typical Performance Curves (Continued)

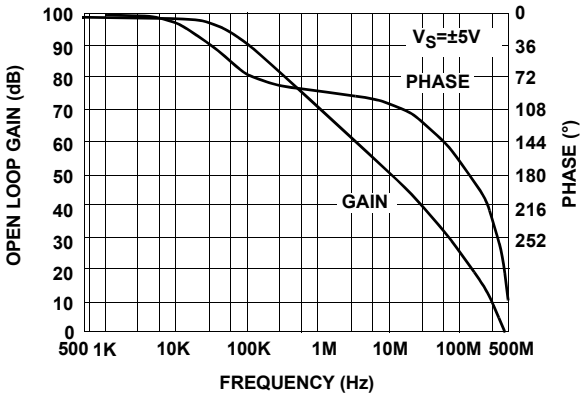


FIGURE 11. OPEN LOOP GAIN AND PHASE vs FREQUENCY

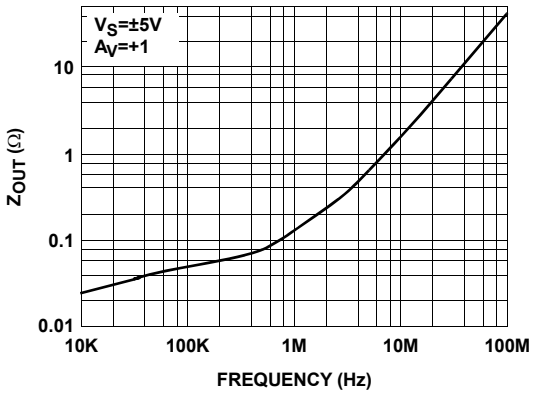


FIGURE 12. Z_{OUT} vs FREQUENCY

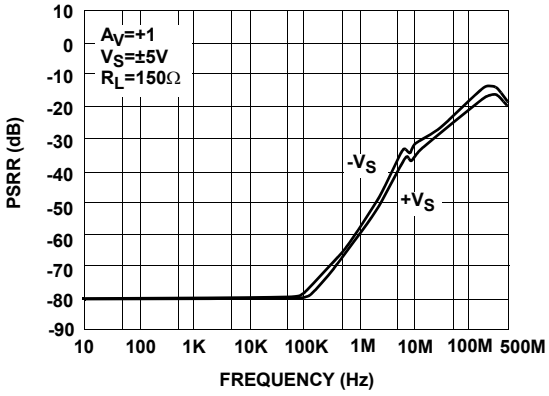


FIGURE 13. PSRR vs FREQUENCY

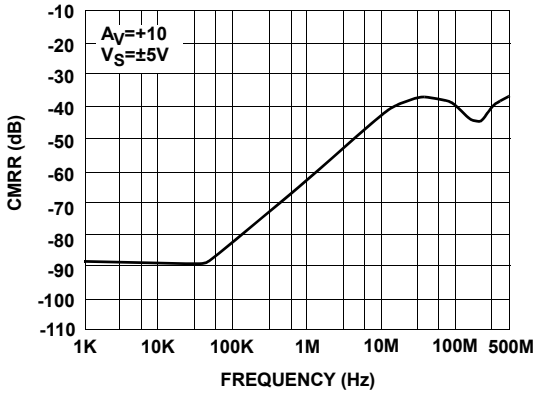


FIGURE 14. CMRR vs FREQUENCY

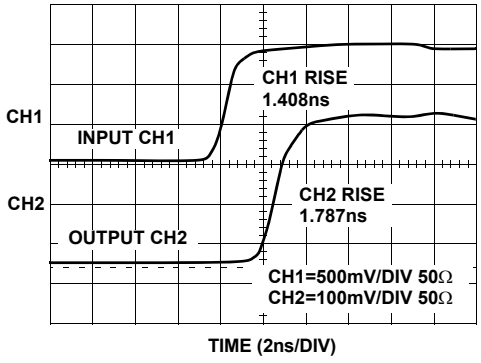


FIGURE 15. LARGE SIGNAL RISE TIME

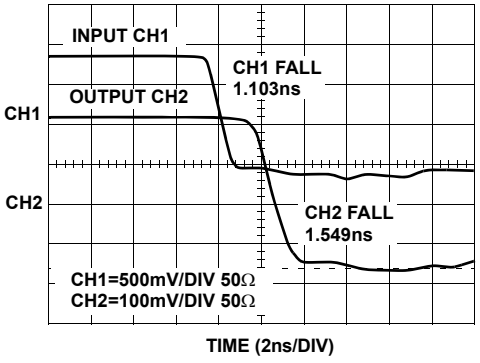


FIGURE 16. LARGE SIGNAL FALL TIME

Typical Performance Curves (Continued)

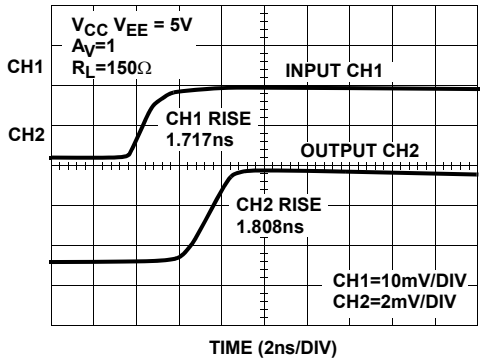


FIGURE 17. SMALL SIGNAL RISE TIME

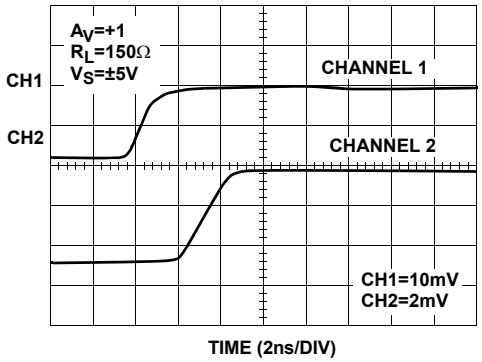


FIGURE 18. SMALL SIGNAL RISE TIME

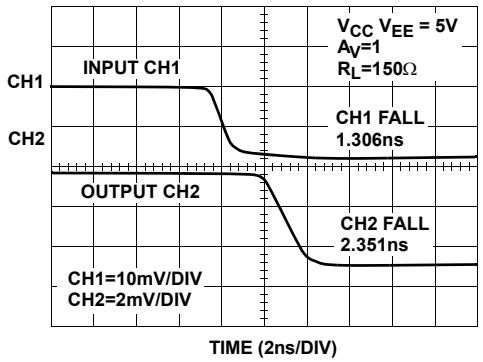


FIGURE 19. SMALL SIGNAL FALL TIME

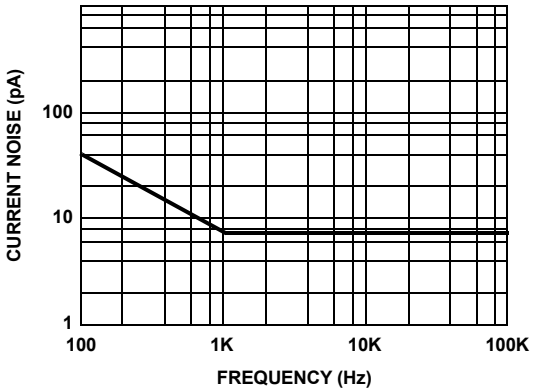


FIGURE 20. CURRENT NOISE

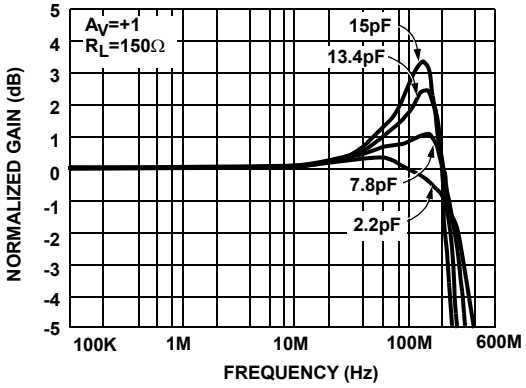


FIGURE 21. GAIN vs FREQUENCY FOR VARIOUS C_L

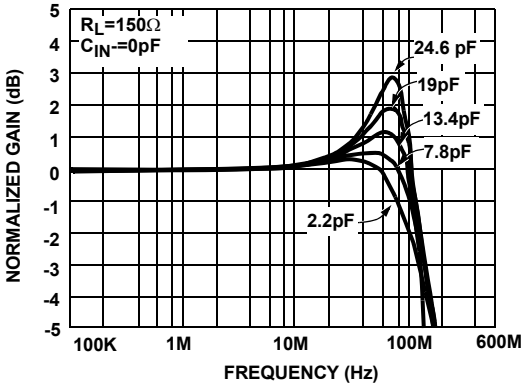


FIGURE 22. GAIN vs FREQUENCY FOR VARIOUS C_L

Typical Performance Curves (Continued)

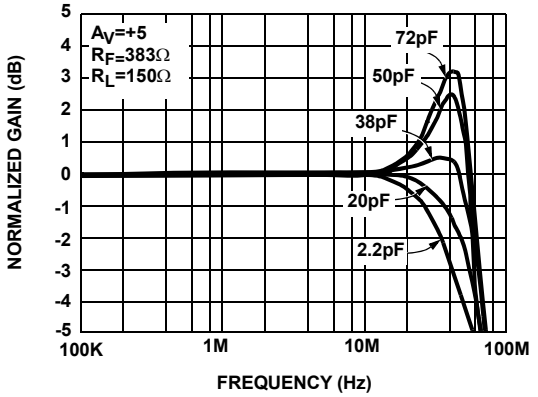


FIGURE 23. GAIN vs FREQUENCY FOR VARIOUS C_L

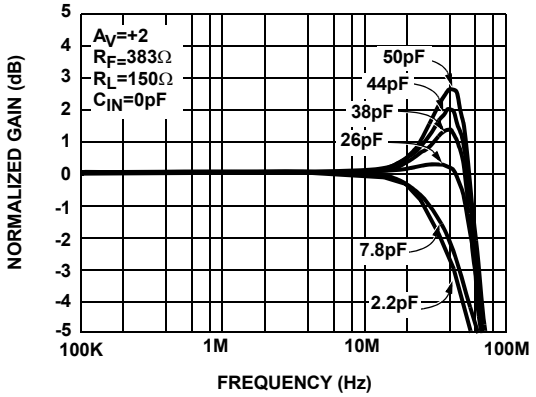


FIGURE 24. GAIN vs FREQUENCY FOR VARIOUS C_L

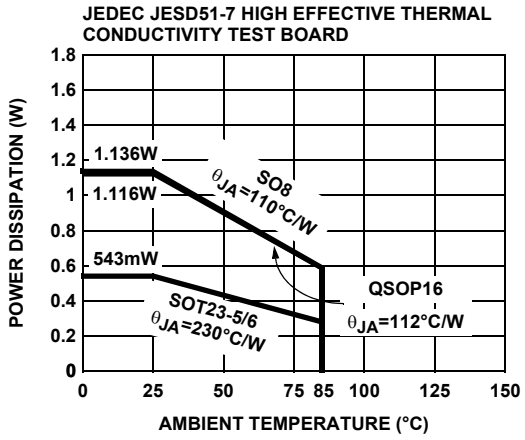


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

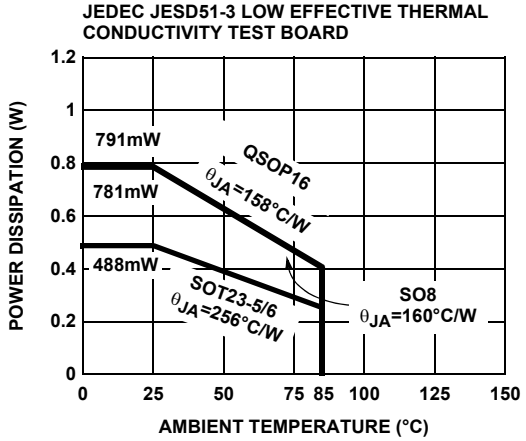


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

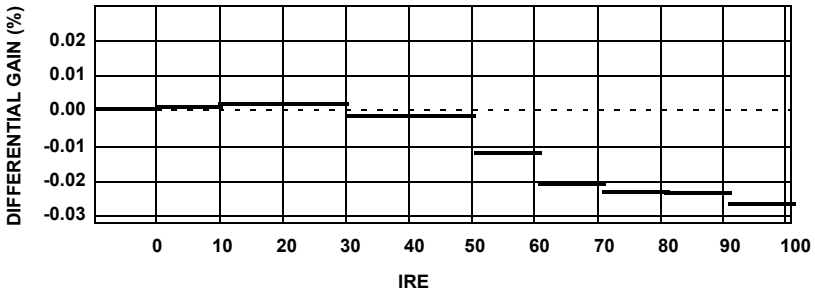


FIGURE 27. DIFFERENTIAL GAIN (%)

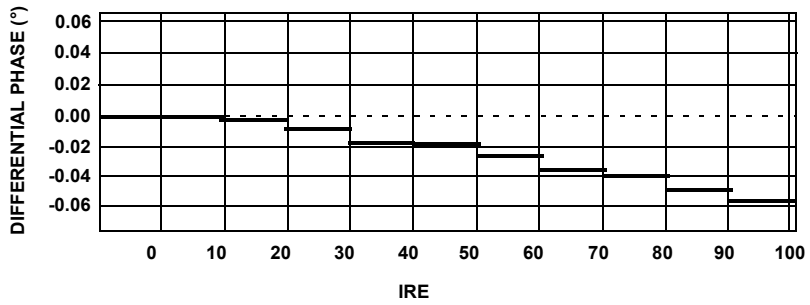


FIGURE 28. DIFFERENTIAL PHASE (°)

Application Information

Video Amplifier with Reduced Size Output Capacitance

If you have a video line driver Z = 75Ω, the DC decoupling capacitor could be relatively large.

$$C = \frac{1}{2\pi \times R \times f} =$$

f = 10Hz, R = Z = 75Ω, C = 132µF

By using the circuit below, C could be reduced to C2 = 22µF.

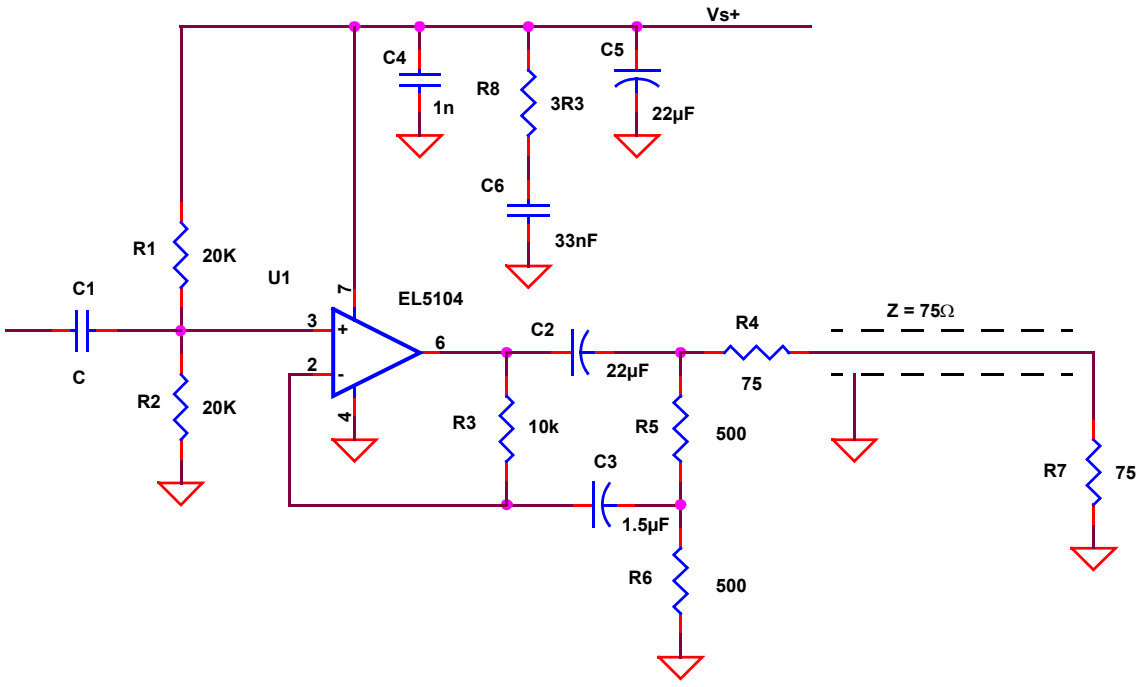


FIGURE 29.

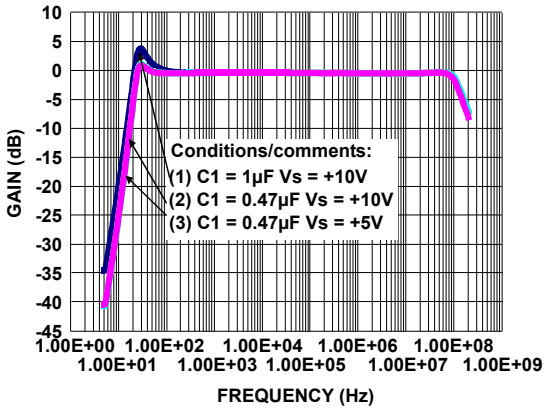


FIGURE 30. VIDEO-

The test result is shown on Figure 30.

By selecting a different value for C1, we could reduce the effect, created by C3 R3 and get flat response from 16Hz with an 1/5 value, price and size output capacitor. There is another, very important issue by using high bandwidth amplifiers.

In the past when the bandwidth of the operational amplifier ended at a few hundred kHz even at few MHz, the power-supply bypass was not a very critical issue, since a 0.1µF capacitor “did the job”, but today’s amplifiers could have bandwidth, what used to be reserved for microwave circuits not to long time ago.

Therefore that high bandwidth amplifiers require the same respect what we reserve for microwave circuits. Particularly the power supply bypass and the pcb-layout could very heavily influence the performance of a modern high bandwidth amplifiers. It could happen above a few MHz, but it will happen above 100MHz, that the capacitor will behave like an inductor.

The reason for that is the very small but not zero value serial inductance of the capacitor.

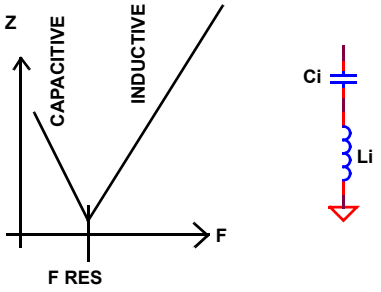


FIGURE 31.

The capacitor will behave as a capacitor up to its resonance frequency, above the resonance frequency it will behave as an inductor.

Just 1nHy inductance serial with 1nF capacitance will have serial resonance at:

$$F = \frac{1}{2\pi\sqrt{L \times C}}$$

C = 1nF, L = 1nHy, F = 159 MHz

And an other 1nHy is very easy to get together with the inductance of traces on the pcb, and therefore you could encounter resonances from ca 50MHz and above anywhere. So if the amplifier has a bandwidth of a few hundred MHz, the proper power supply by-pass could become a serious if not difficult task.

Intuitively, you would use capacitors value 0.1µF parallel with a few µF tantalum, and to cure the effect of it's serial resonance put a smaller one parallel to it.

The result will surprise to you, because you will get even something worse than without the small capacitor.

What is happening there? Just look what we get:

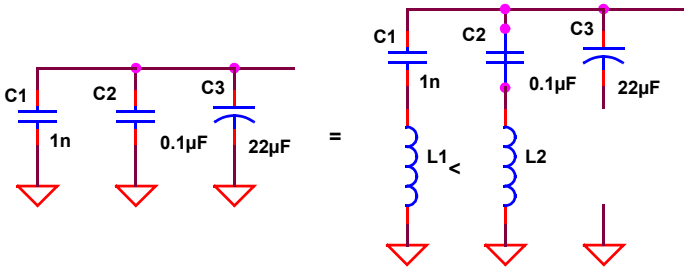


FIGURE 32.

Above its serial resonance C2* the ideal capacitance of C2 is a short, the Tantalum capacitor for high frequencies is not effective, the left over is C1 capacitor and L1 + L2 inductors, we get a parallel tank circuit, which is at it's resonance a high impedance path and do not carry any high frequency current, it does not work as bypass at all!

The impedance of a parallel tank circuit at resonance is dependent from it's Q. High Q high impedance.

The Q of a parallel tank circuit could be reduced by bypassing it with a resistor, or adding a resistor in serial to one of the reactive components. Since the bypassing would short the DC supply we do have to go to add resistor in serial to the reactive component, we will ad a resistor serial with the inductor. (See Figure 33.)

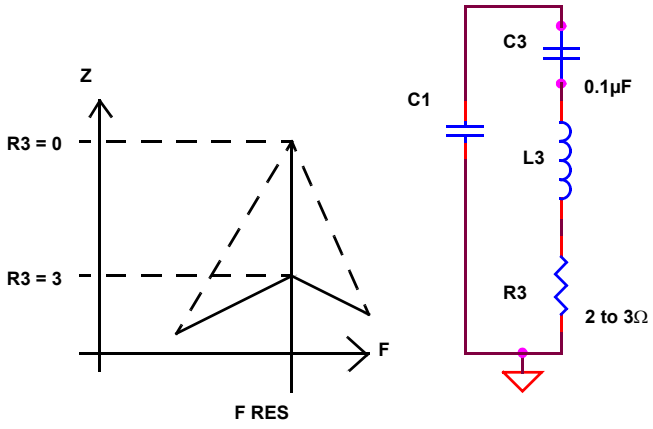


FIGURE 33.

The final power supply bypass circuit will look:

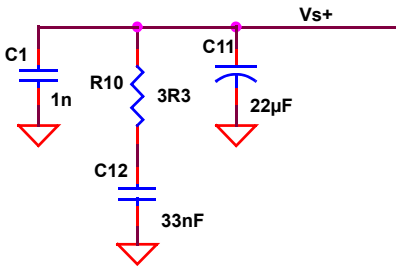
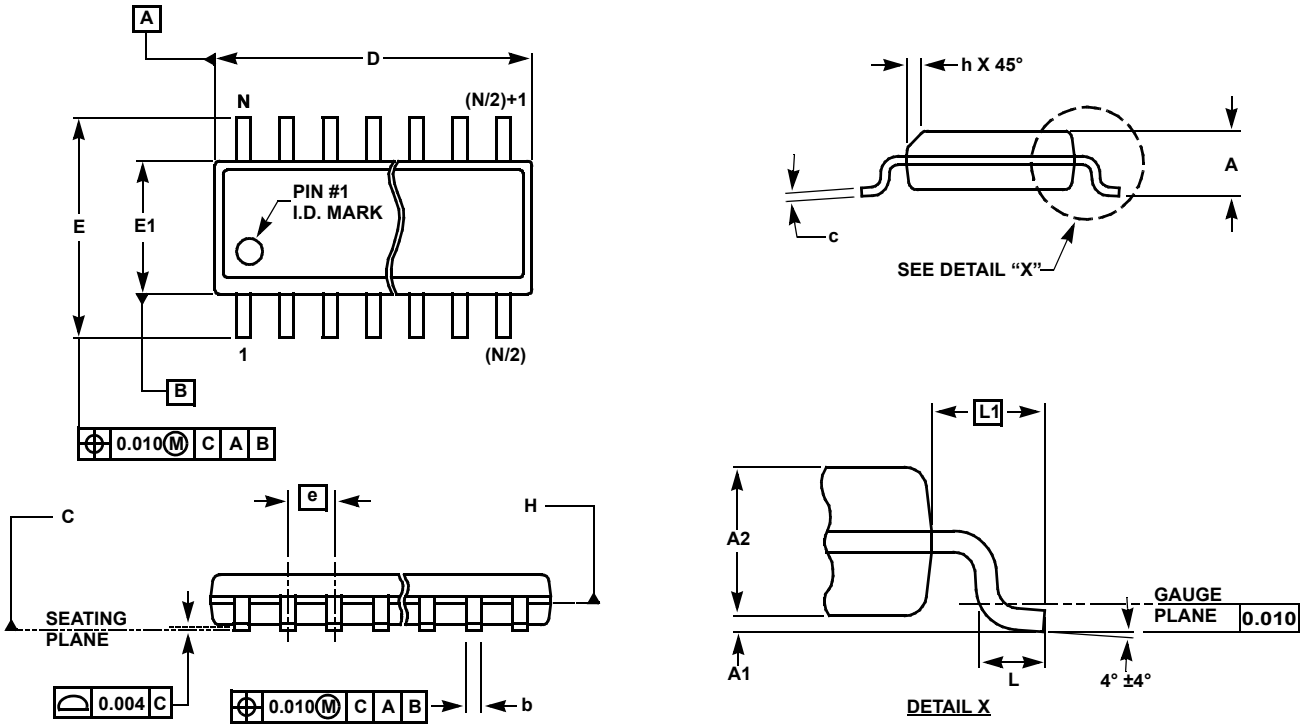


FIGURE 34.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

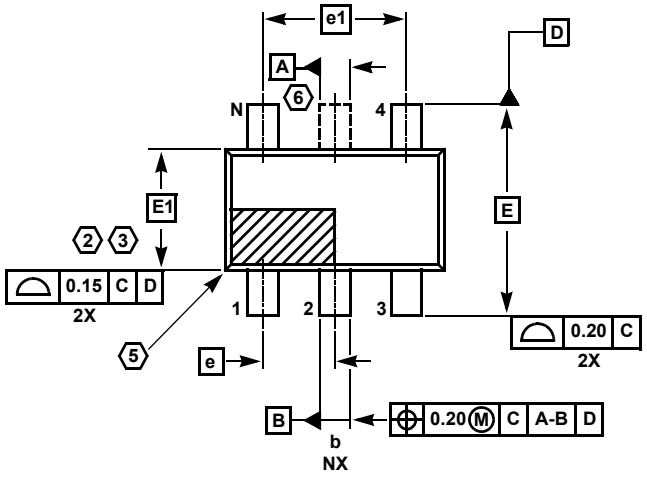
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

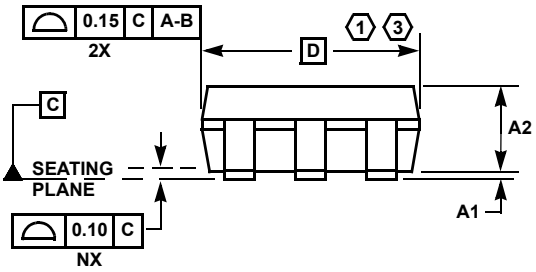
Rev. M 2/07

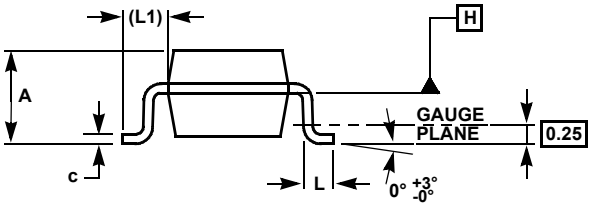
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

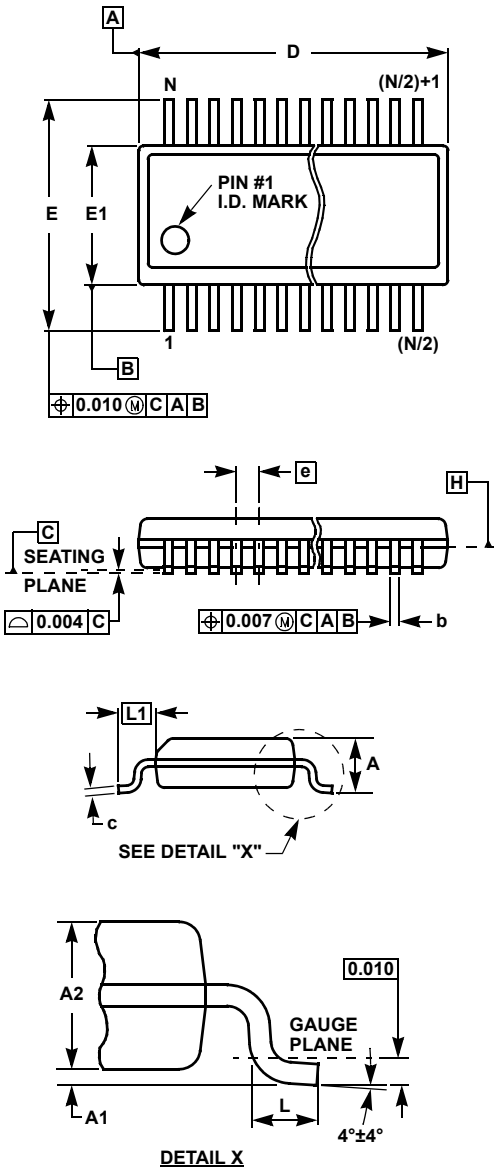
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.