April 2015

FPF2411 — IntelliMAX™ 6 V / 6 A - Rated Bi-Directional Switch with Slew Rate Control and RCB

Features

- Capability: 6 V
- Low R_{ON}
  - 10 mΩ at 5 V at PWRA or PWRB (Typ.)
  - 12 mΩ at 3.8 V at PWRA or PWRB (Typ.)
- Maximum Current Capability: 6 A (Bi-Directional)
- Ultra-Low I_Q:<1 µA
- Active LOW Control Pin
- 2 ms Long Slew Rate
- Reverse Current Blocking (RCB) during OFF
- Robust ESD Capability:
  - 5 kV HBM, 2 kV CDM
  - 15 kV Air Discharge
  - 8 kV Contact Discharge Under IEC 61000-4-2

Applications

- Smartphone / Tablet PC
- Mobile Devices
- Portable Media Devices

Description

The FPF2411 is a 6 V / 6 A-rated bi-directional load switch, consisting of a slew-rate-controlled, low-on-resistance, P-channel MOSFET switch with protection features. The slew-rate-controlled turn-on characteristic prevents inrush current and the resulting excessive voltage droop on the input power rails. The input voltage range operates from 2.3 V to 5.5 V.

Bi-directional switching allows reverse current from V_{OUT} to V_{IN}. The switching is controlled by active-LOW logic input the ONB pin. The FPF2411 is capable of interfacing directly with low-voltage control signal General-Purpose Input / Output (GPIO).

The FPF2411 is available in 12-bump, 1.235 mm x 1.625 mm Wafer-Level Chip-Scale Package (WLCSP) with 0.4 mm pitch.

Ordering Information

Part Number	Top Mark	R_{ON} (Typ.) at 3.8 V_{IN}	Output Discharge	ONB Pin Functionality	Package
FPF2411BUCX_F130	QR	12 mΩ	No	Active LOW	12-Ball Wafer-Level Chip-Scale Package (WLCSP), 3 x 4 Array, 0.4 mm Pitch, 250 µm Ball

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Application Diagrams

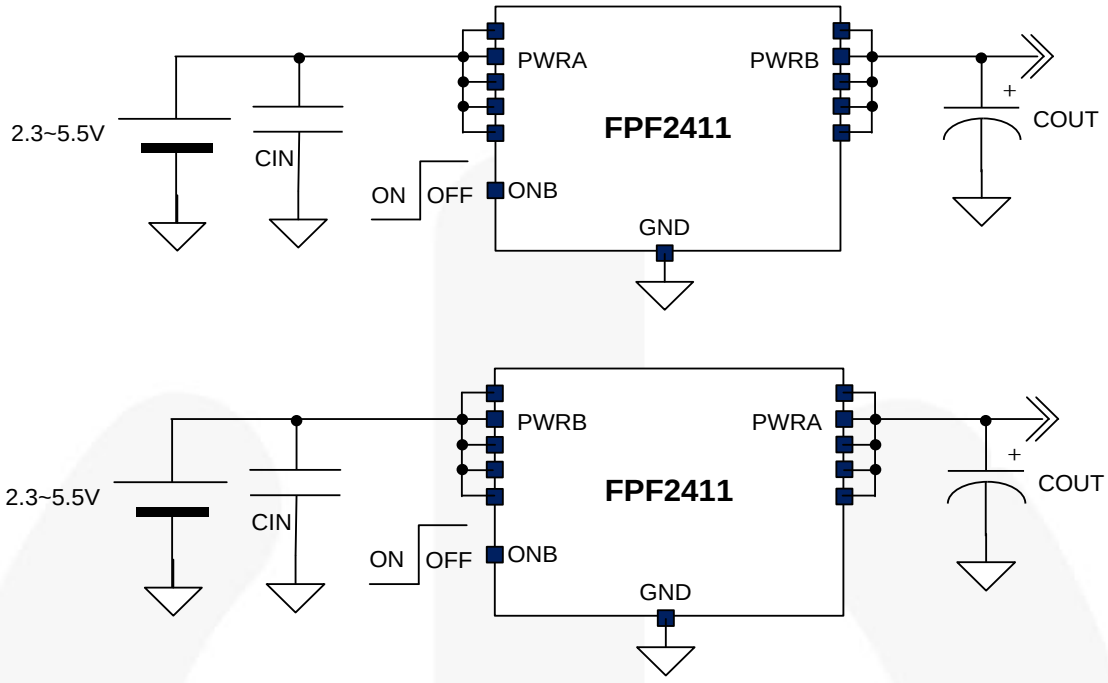
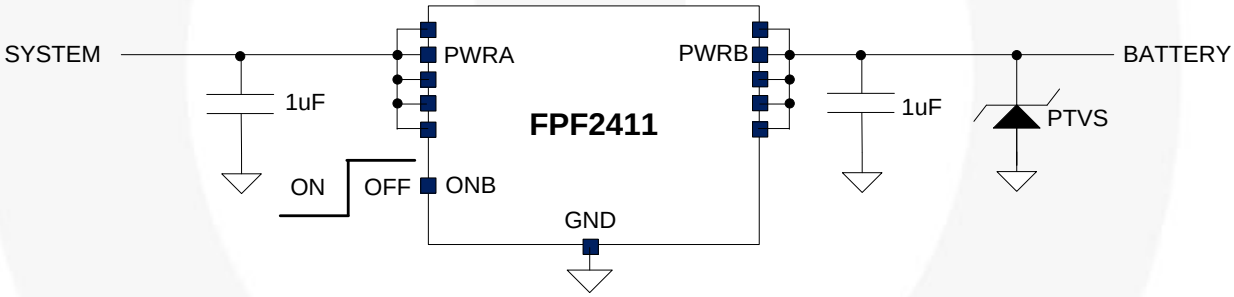


Figure 1. High-Level Application Diagrams



Note: Adding a PTVS such as RDP3101B is recommended at PWRB node in order to avoid device damage from surge or equivalent stress.

Figure 2. Battery Isolation Application

Block Diagrams

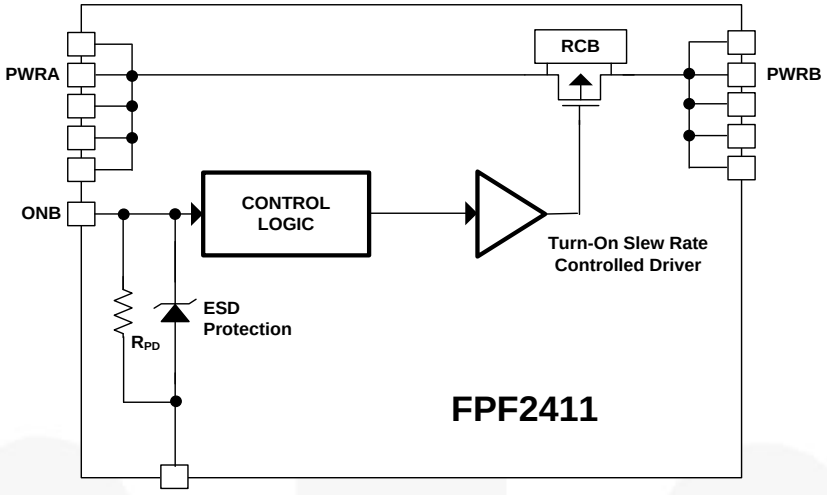


Figure 3. Block Diagram

Application Scenario

Table 1. PWRA and PWRB can be Input or Output, Depending on Scenario

PWRA	PWRB	ONB	Operations
X	X	HIGH	OFF state PWRA and PWRB are isolated. Current more than I_{SD} or I_{RCB} is NOT allowed.
2.3~5.5 V	Open	HIGH → LOW	Turn-on with 2 ms of t_R at PWRB.
Open	2.3~5.5 V	HIGH → LOW	Turn-on with 2 ms of t_R at PWRA.
2.3~5.5 V	Open	LOW	ON state Operating current is from PWRA. No problem with 6 A DC current flowing.
Open	2.3~5.5 V	LOW	ON state Operating current is from PWRB. No problem with 6 A DC current flowing.
2.3~5.5 V	Open	LOW → HIGH	Turn-off with 1 ms of t_F at PWRB.
Open	2.3~5.5 V	LOW → HIGH	Turn-off with 1 ms of t_F at PWRA.

Note:

1. X = Don't care.

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Timing Diagrams

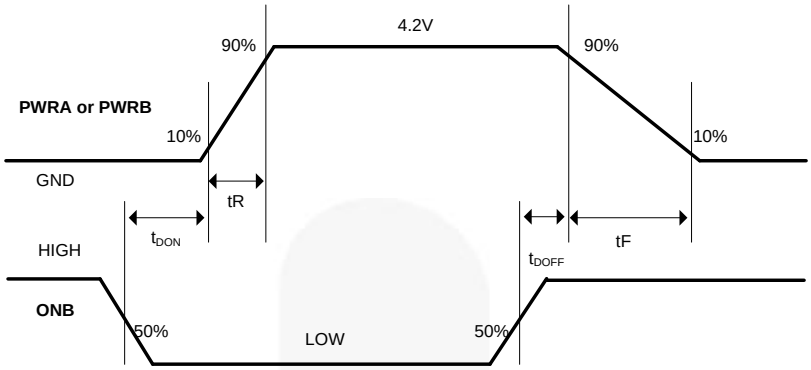
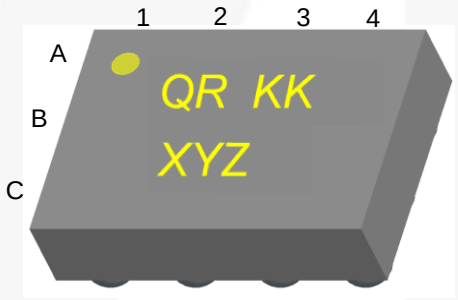


Figure 4. Dynamic Behavior

Pin Configuration



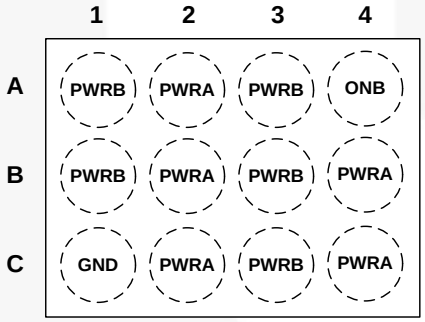
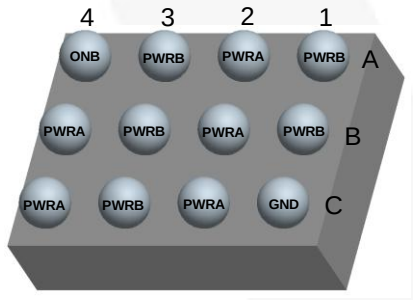


Figure 5. Top View



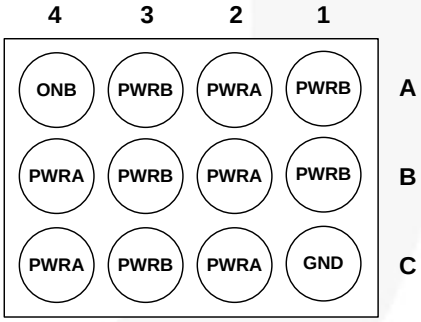


Figure 6. Bottom View

Pin Descriptions

Pin #	Name	Description
A2, B2, B4, C2, C4	PWRA	Power Input / Output: Bi-directional power path
A1, A3, B1, B3, C3	PWRB	Power Input / Output: Bi-directional power path
C1	GND	Ground
A4	ONB	ON/OFF Control Input: Active LOW.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{PIN}	PWRA, PWRB, ONB to GND		-0.3	6.0	V
I_{SW}	Maximum Continuous Switch Current			6	A
t_{PD}	Total Power Dissipation at T_A=25°C			1.48	W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Junction Temperature		-65	+150	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient (1in.^{2} Pad of 2 oz. Copper)			84.1(2)	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	5		kV
		Charged Device Model, JESD22-C101	2		
	IEC61000-4-2 System Level	Air Discharge (PWRA, PWRB, ONB to GND)	15		
		Contact Discharge (PWRA, PWRB, ONB to GND)	8		

Note:

2. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{PWRn}	PWRA, PWRB	2.3	5.5	V
T_A	Ambient Operating Temperature	-40	85	°C

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DC / AC Characteristics

Unless otherwise noted, V_{IN}=2.3 to 5.5 V, T_A=-40 to 85°C; typical values are at PWRA or PWRB=4.2 V and T_A=25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PWRA} V_{PWRB}	Input Voltage		2.3		5.5	V
I_{SD}	Shutdown Current	PWRA=ONB=5.5 V, PWRB=Open OR PWRB=ONB=5.5 V, PWRA=Open			1	µA
I_{PWRA} I_{PWRB}	Quiescent Current	ONB=GND, I_{OUT}=0 mA			1	µA
R_{ON}	On-Resistance	PWRA, PWRB=3.8 V, I_{OUT}=200 mA, T_A=25°C		12	17	mΩ
		PWRA, PWRB=5 V, I_{OUT}=200 mA, T_A=25°C		10	16	
V_{IH}	ONB, Input Logic HIGH Voltage[3]	PWRn=4.5 V, I_{LOAD}=50 µA, T_A (Max.) = 60°C	4.3			V
		PWRn=3.6 V, I_{LOAD} =50 µA, T_A (Max.) = 60°C	3.4			
V_{IL}	ONB, Input Logic LOW Voltage[3]	PWRn=4.5 V, I_{LOAD} =50 µA, T_A (Max.) = 60°C			0.4	
		PWRn=3.6 V, I_{LOAD} =50 µA, T_A (Max.) = 60°C			0.4	
R_{PD}	Pull-Down Resistance at ONB			500	700	kΩ
Dynamic Characteristics: *see definitions below*						
t_{DON}	Turn-On Delay[4,5,6]	PWRA or PWRB =4.2 V, R_L=10 Ω, C_L=1 µF, ONB=HIGH to LOW		1.5		ms
t_R	Rise Time[4,5,6]			3.0		
t_{ON}	Turn-On Time[4,5,6]			4.5		
t_{DOFF}	Turn-Off Delay[4,5,7]	PWRA or PWRB =4.2 V, R_L=100 Ω, C_L=1 µF, ONB=LOW to HIGH		5.5		ms
t_F	Fall Time[4,5,7]			1.0		
t_{OFF}	Turn-Off Time[4,5,7]			6.5		

Notes:

3. V_{IH}/V_{IL} is tested under 50 µA current load
4. This parameter is guaranteed by design and characterization; not production tested.
5. $t_{DON}/t_{DOFF}/t_R/t_F$ are defined in Figure 4.
6. $t_{ON}=t_R + t_{DON}$.
7. $t_{OFF}=t_F + t_{DOFF}$.

Table 2. V_{IH} / V_{IL} [V]

I_{LOAD} \ V_{BAT}	2.7 V	3.7 V	4.35 V
0.1 mA	1.8 / 0.7	2.9 / 0.9	3.4 / 1.0
1 mA	1.1 / 0.7	2.1 / 0.9	2.8 / 1.0
3 mA	1.1 / 0.7	2.1 / 0.9	2.7 / 1.0
5 mA	1.0 / 0.7	2.0 / 0.9	2.7 / 1.0
10 mA	0.9 / 0.7	1.9 / 0.8	2.4 / 0.9
30 mA	0.9 / 0.7	1.5 / 0.8	2.2 / 0.9
50 mA	0.9 / 0.7	1.2 / 0.8	1.9 / 0.9
100 mA	0.9 / 0.7	1.0 / 0.8	1.1 / 0.9

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Typical Performance Characteristics

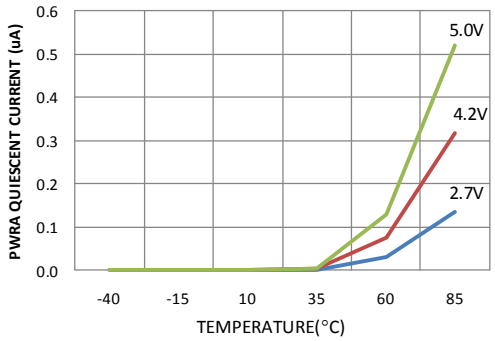

Figure 7. PWRA Quiescent Supply Current vs. Temperature

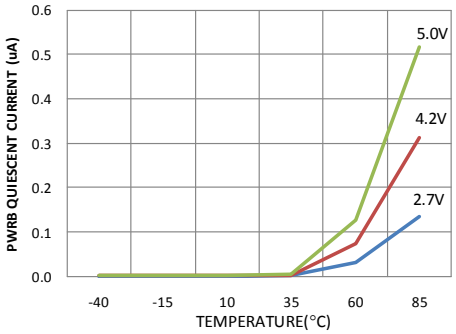

Figure 8. PWRB Quiescent Supply Current vs. Temperature

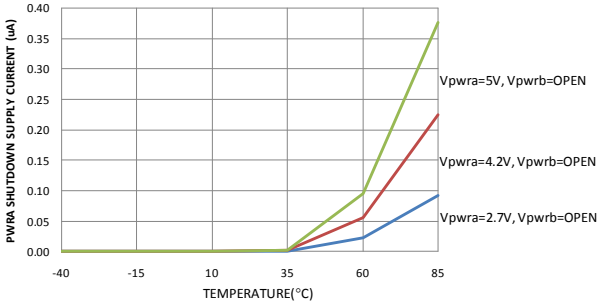

Figure 9. PWRA Shutdown Supply Current vs. Temperature

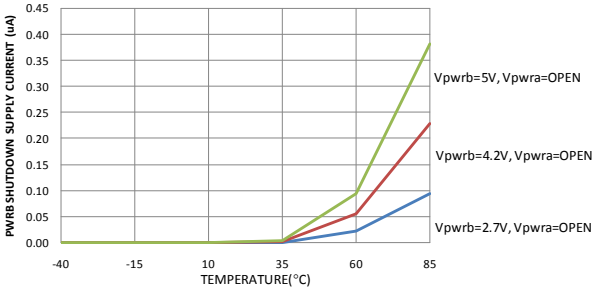

Figure 10. PWRB Shutdown Supply Current vs. Temperature

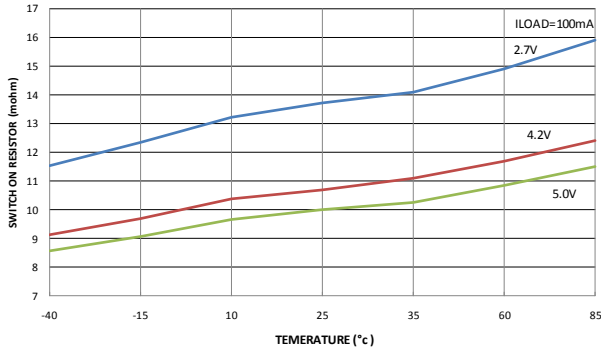

Figure 11. Switch On Resistance vs. Temperature

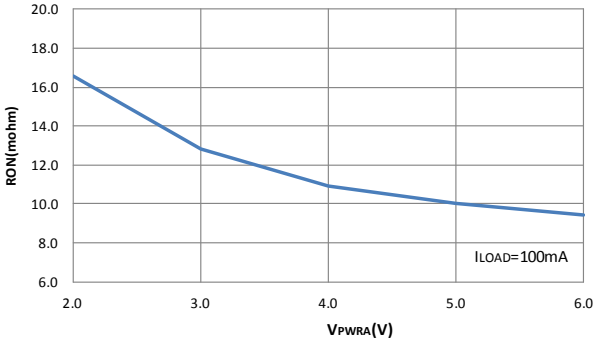

Figure 12. On Resistance vs. PWRA Voltage

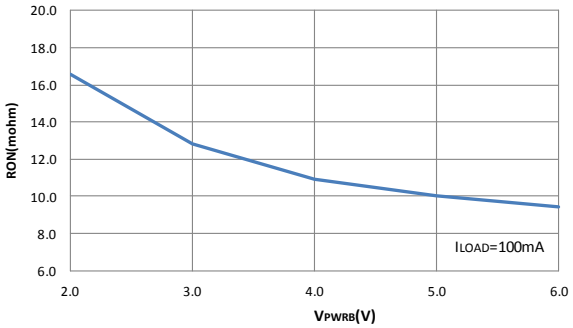

Figure 13. On Resistance vs. PWRB Voltage

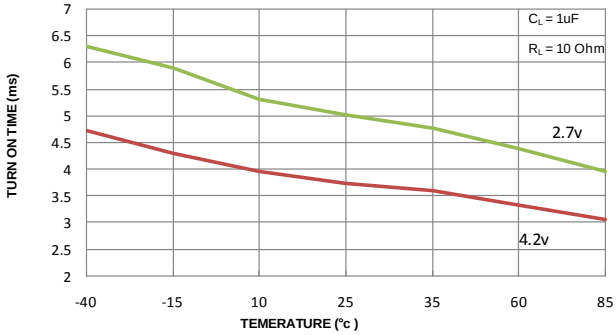

Figure 14. Switch On Time vs. Temperature

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Typical Performance Characteristics (Continued)

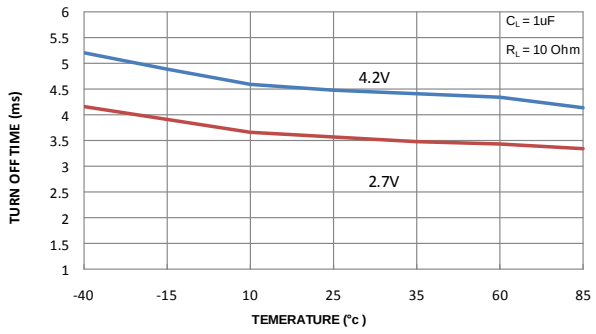

Figure 15. Switch Off Time vs. Temperature

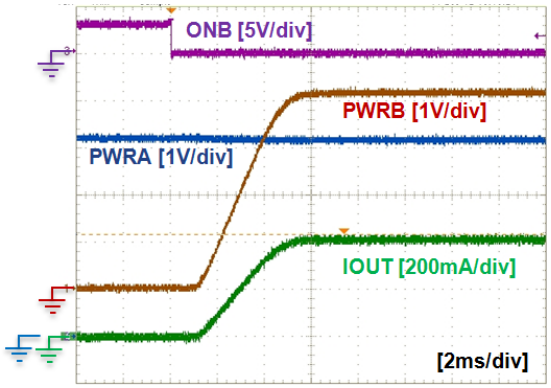

Figure 16. Turn-On Response (V_{IN}=4.2 V, C_{IN}=1 µF, C_{OUT}=1 µF, R_L=10 Ω)

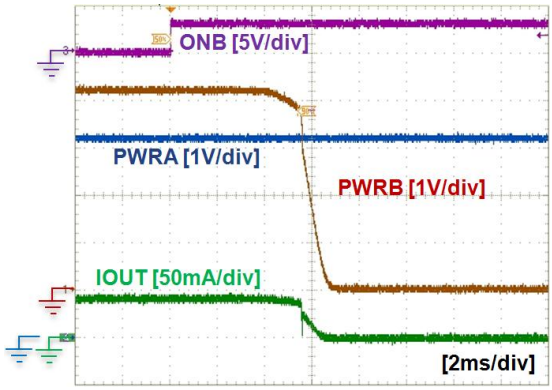

Figure 17. Turn-OFF Response (V_{IN}=4.2 V, C_{IN}=1 µF, C_{OUT}=1 µF, R_L=100 Ω)

Operation and Application Description

The FPF2411 is an ultra-low-R_{ON} P-channel load switch with bi-directional controlled turn-on and Reverse Current Blocking (RCB). The core is a 12 mΩ P-channel MOSFET and controller capable of functioning over a wide input operating range of 2.3 V to 5.5 V. The ONB pin, active-LOW; controls the state of the switch. RCB functionality blocks unwanted reverse current during OFF states by power switch isolation between PWRA and PWRB.

Inrush Current

Inrush current occurs when the device is turned on. Inrush current is dependent on output capacitance and slew rate control capability, as expressed by:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN} - V_{INITIAL}}{t_R} + I_{LOAD}$$

where:

C_{OUT}: Output capacitance;
t_R: Slew rate or rise time at V_{OUT};
V_{IN}: Input voltage;
$V_{INITIAL}$: Initial voltage at C_{OUT}, usually GND; and
I_{LOAD}: Load current.

Higher inrush current causes higher input voltage drop, depending on the distributed input resistance and input capacitance. High inrush current can cause problems.

FPF2411 has a 3 ms of slew rate capability under 4.2 V_{IN} at 1 µF of C_{OUT} and 10 Ω of R_L. Inrush current can be minimized and no input voltage drop appears, as shown in Figure 16.

Reverse-Current Blocking

The reverse-current blocking feature protects the input source against current flow from output to input when the load switch is off by changing the internal body diode direction.

Bypass Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor; a capacitor must be placed between the PWRA or PWRB and GND pins. A ceramic capacitor of at least 1 µF placed close to the pins is usually sufficient.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance on normal and short-circuit operation. Using wide traces or large copper planes for all pins (PWRA, PWRB, ONB, and GND) minimizes the parasitic electrical effects and the case-to-ambient thermal impedance.

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WLCSP Packing - Embossed Tape
FPF2411BUCX Pin1 at 1 o'clock Rev0

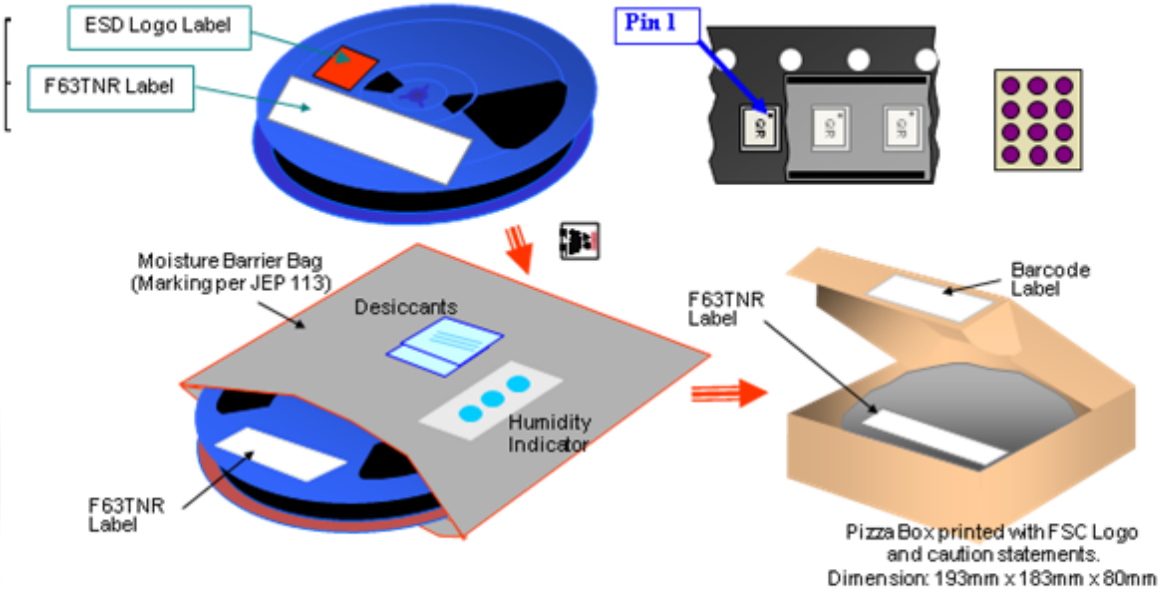
FAIRCHILD SEMICONDUCTOR®

Packing Description:

WLCSP products are classified under Moisture Sensitive Level 1 and are packed in moisture barrier bag for added protection.

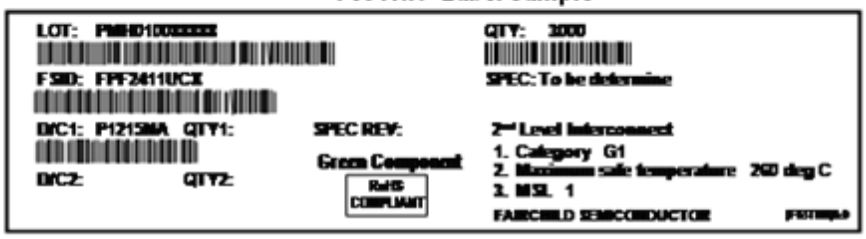
The carrier tape is made from dissipative polystyrene or polycarbonate resin. The cover tape is a multilayer film primarily composed of polyester film, adhesive layer, heat activated sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3000 units per 178 mm diameter reel. Up to three reels are packed in each intermediate box. The reels is made of polystyrene plastic (anti-static coated or intrinsic).

These full reels are individually barcode labeled and placed inside a pizza box made of recyclable corrugated brown paper with a Fairchild logo printing. The reel is packed single reel in the pizza box. And these pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

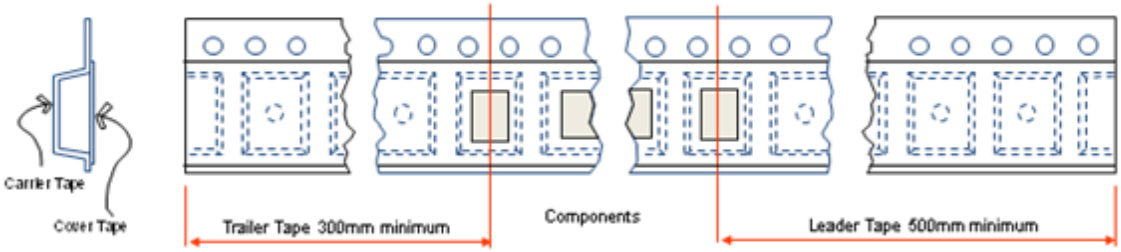


ESD Logo Label sample

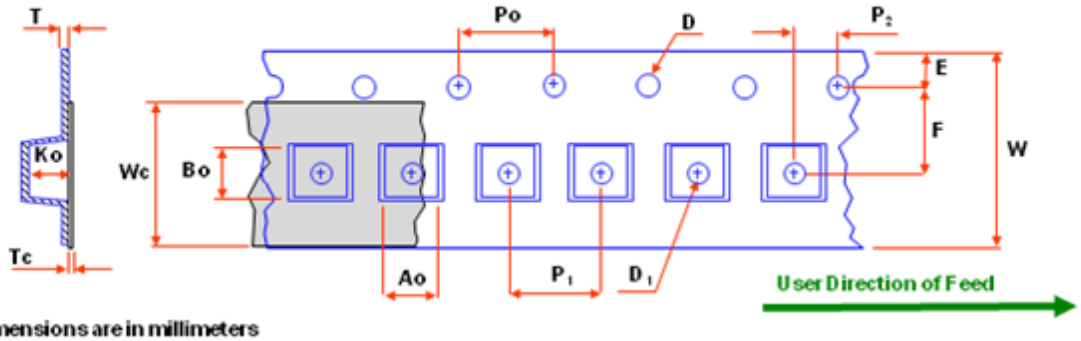
F63TNR Label sample



Tape Leader and Trailer Configuration



WLCSP Embossed Tape Dimension



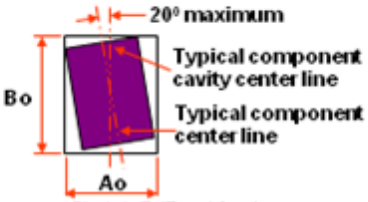
Dimensions are in millimeters

Package	Ao +/-0.05	Bo +/-0.05	D +0.10	D1 min.	E +/-0.1	F +/-0.1	Ko +/-0.05	P1 TYP	Po TYP	P2 +/-0.05	T TYP	Tc +/-0.005	W +/-0.3	Wc TYP
FPF2411UCX	1.55	1.95	1.50	0.5	1.75	3.5	0.75	4	4	2.0	0.25	0.06	8	5.3

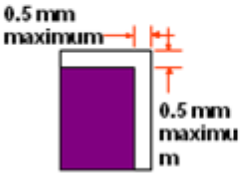
Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

20 deg maximum component rotation

Sketch A (Side or Front Sectional View)
Component Rotation

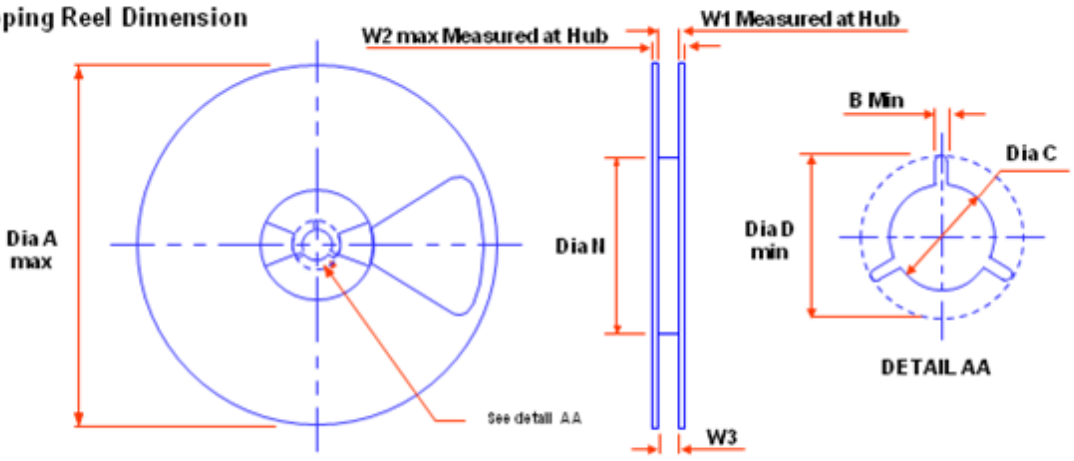


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

Shipping Reel Dimension

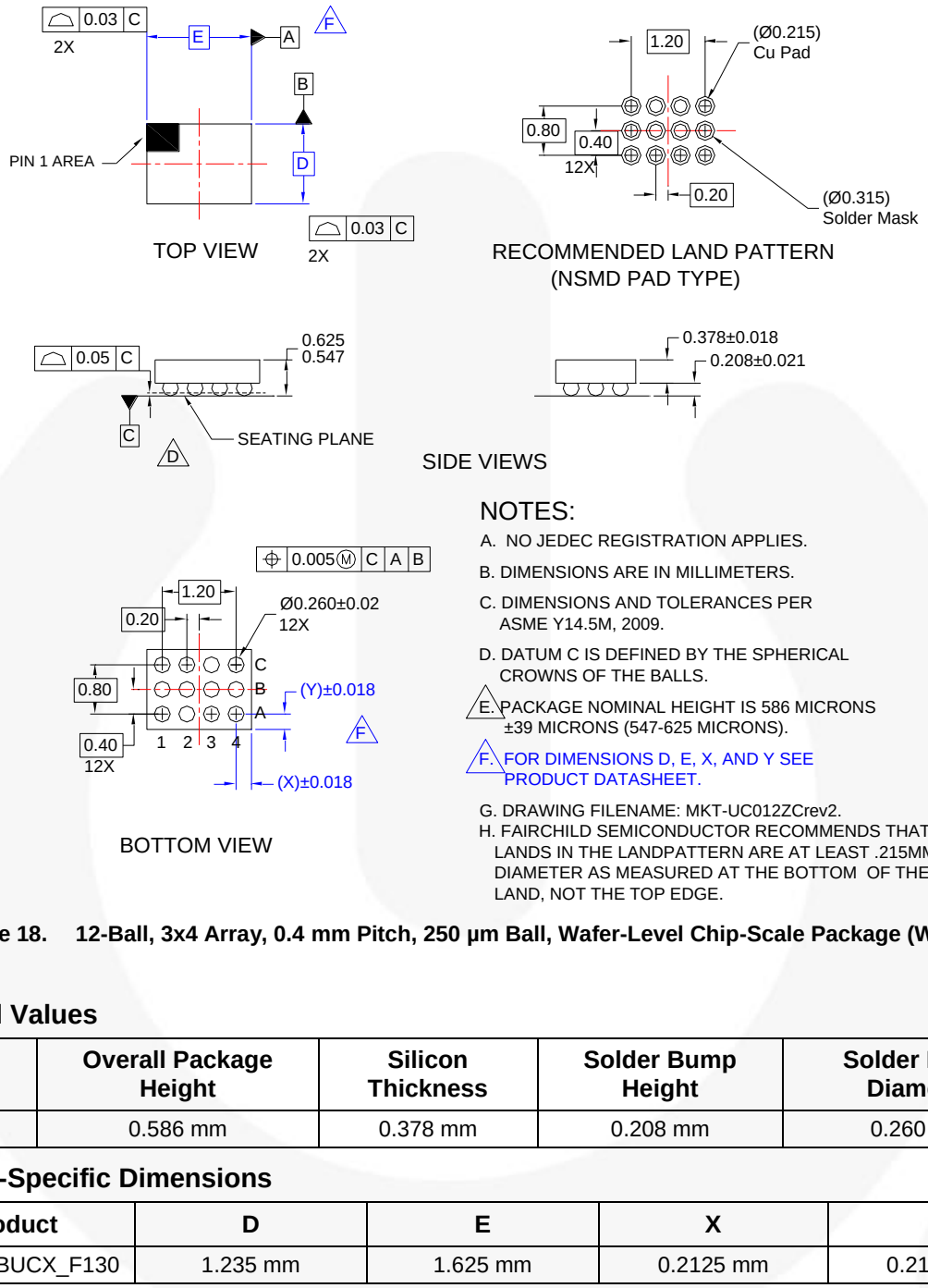


Dimensions are in millimeters

Tape Width	Dia A max	Dim B min	Dia C +.5/-.2	Dia D min	Dim N min	Dim W1 +2/-0	Dim W2 max	Dim W3 (LSL - USL)
8	178	1.5	13	20.2	55	8.4	14.4	7.9~10.4

Rev 1 , 25102011

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC012ZCrev2.

H. FAIRCHILD SEMICONDUCTOR RECOMMENDS THAT LANDS IN THE LANDPATTERN ARE AT LEAST .215MM DIAMETER AS MEASURED AT THE BOTTOM OF THE LAND, NOT THE TOP EDGE.

Figure 18. 12-Ball, 3x4 Array, 0.4 mm Pitch, 250 µm Ball, Wafer-Level Chip-Scale Package (WLCSP)

Nominal Values

Bump Pitch	Overall Package Height	Silicon Thickness	Solder Bump Height	Solder Bump Diameter
0.4 mm	0.586 mm	0.378 mm	0.208 mm	0.260 mm

Product-Specific Dimensions

Product	D	E	X	Y
FPF2411BUCX_F130	1.235 mm	1.625 mm	0.2125 mm	0.2175 mm

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TRADEMARKS

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