TPS22920x 3.6-V, 4-A, 5.3-mΩ On-Resistance, Integrated Load Switch with Controlled Turn-on

1 Features

- Input Voltage Range: 0.75 V to 3.6 V
- Integrated Load Switch
- Integrated Pass-FET r_{DSON} = 2 mΩ (Typ) at 3.6 V
- Typical ON-Resistance
  - r_{ON} = 5.3 mΩ at V_{IN} = 3.6 V
  - r_{ON} = 5.4 mΩ at V_{IN} = 2.5 V
  - r_{ON} = 5.5 mΩ at V_{IN} = 1.8 V
  - r_{ON} = 5.8 mΩ at V_{IN} = 1.2 V
  - r_{ON} = 6.1 mΩ at V_{IN} = 1.05 V
  - r_{ON} = 7.3 mΩ at V_{IN} = 0.75 V
- CSP-8 Package 0.9 mm × 1.9 mm, 0.5 mm Pitch
- 4-A Maximum Continuous Switch Current
- Shutdown Current 5.5-µA Max
- ON-Logic Available in Both Active High/Low:
  - TPS22920 is Active High
  - TPS22920L is Active Low
- Low Threshold Control Input
- Controlled Slew-Rate to Avoid Inrush Current
- Quick Output Discharge Resistor
- ESD Performance Tested Per JESD 22
  - 4000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Notebook / Netbook Computer
- Tablet PC
- PDAs / Smartphones
- GPS Navigation Devices
- MP3 Players

3 Description

The TPS22920x is a small, space-saving load switch with controlled turn on to reduce inrush current. The device contains a N-channel MOSFET that can operate over an input voltage range of 0.75 V to 3.6 V and switch currents up to 4 A. An integrated charge pump biases the NMOS switch in order to achieve a minimum switch ON resistance (r_{ON}). The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

The TPS22920x has a 1250-Ω on-chip resistor for quick output discharge when the switch is turned off which insures that the output is not left floating.

The TPS22920x has an internally controlled rise time in order to reduce inrush current.

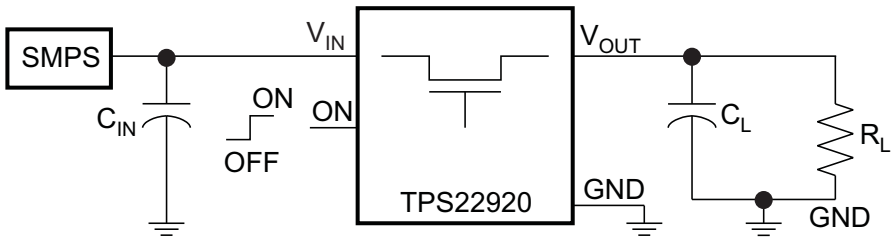
The TPS22920x is available in an ultra-small, space-saving 8-pin CSP package and is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22920x	DSBGA (8)	1.90 mm x 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (April 2015) to Revision D — **Page**

- Added Information about backside coating to *Device Comparison* table ... 3

Changes from Revision November 2014 (B) to Revision C — **Page**

- Added TPS22920L to the datasheet. ... 1

Changes from Revision A (July 2013) to Revision B — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (June 2011) to Revision A — **Page**

- Updated swapped image issue. ... 7

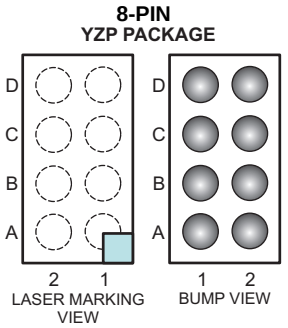
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5 Device Comparison Table

ORDERABLE PART NUMBER	R_{ON} (TYP) AT 3.6 V	RISE TIME (TYP) at 3.6V	QUICK OUTPUT DISCHARGE(1)	BACKSIDE COATING(2)	ENABLE
TPS22920YZPR	5.3 mΩ	880 µS	Yes	No	Active High
TPS22920YZPRB	5.3 mΩ	880 µS	Yes	Yes	Active High
TPS22920LYZPR	5.3 mΩ	627 µS	Yes	Yes	Active Low

(1) This feature discharges the output of the switch to ground through a 1250-Ω resistor, preventing the output from floating. See *Output Pull-Down*.
(2) CSP (DSBGA) devices manufactured with backside coating have an increased resistance to cracking due to the increased physical strength of the package. Devices with backside coating are highly encouraged for new designs.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	D1	-	Ground
ON	D2	I	Switch control input. Do not leave floating
V_{OUT}	A1, B1, C1	O	Switch output
V_{IN}	A2, B2, C2	I	Switch input, bypass this input with a ceramic capacitor to ground

Table 1. Bump Assignments (YZP Package)

D	GND	ON
C	V_{OUT}	V_{IN}
B	V_{OUT}	V_{IN}
A	V_{OUT}	V_{IN}
	1	**2**

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7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	4	V
V_{OUT}	Output voltage range		VIN + 0.3	V
V_{ON}	Input voltage range	–0.3	4	V
I_{MAX}	Maximum Continuous Switch Current		4	A
I_{PLS}	Maximum Pulsed Switch Current, pulse <300 µS, 2% duty cycle		6	A
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.75	3.6	V
V_{OUT}	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{IN} = 2.5 V to 3.6 V	1.2	3.6	V
		V_{IN} = 0.75 V to 2.49 V	0.9	3.6	V
V_{IL}	Low-level input voltage, ON	V_{IN} = 2.5 V to 3.6 V		0.6	V
		V_{IN} = 0.75 V to 2.49 V		0.4	V
T_A	Operating free-air temperature range		–40	85	°C
C_{IN}	Input Capacitor		1(1)		µF

(1) See *Input Capacitor* section in Application Information.

7.4 Thermal Information

THERMAL METRIC(1)		TPS22920x YZP 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	
$R_{\theta JB}$	Junction-to-board thermal resistance	51	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	50	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Unless otherwise noted, V_{IN} = 0.75 V to 3.6 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
I_{IN}	Quiescent Current	I_{OUT} = 0, Switch enabled	V_{IN} = 3.6 V	Full		68	160	µA
			V_{IN} = 2.5 V			40	70	
			V_{IN} = 1.8 V			25	350	µA
			V_{IN} = 1.2 V			103	200	
			V_{IN} = 1.05 V			78	110	µA
			V_{IN} = 0.75 V			37	70	
$I_{IN(leak)}$	Off Supply Current (After Pull Down)	Switch disabled, V_{OUT} = 0		Full			5.5	µA
r_{ON}	On-Resistance	V_{IN} = 3.6 V, I_{OUT} = –200 mA		25°C		5.3	8.8	mΩ
				Full			9.8	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA		25°C		5.4	8.9	mΩ
				Full			9.9	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA		25°C		5.5	9.1	mΩ
				Full			10.1	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA		25°C		5.8	9.4	mΩ
				Full			10.4	
		V_{IN} = 1.05 V, I_{OUT} = –200 mA		25°C		6.1	9.7	mΩ
				Full			10.8	
		V_{IN} = 0.75 V, I_{OUT} = –200 mA		25°C		7.3	11.0	mΩ
				Full			12.4	
RPD	Output pull down resistance(2)	V_{IN} = 3.3 V, Switch disabled, I_{OUT} = 3 mA		Full		1250	1500	Ω
I_{ON}	ON input leakage current	V_{ON} = 0.9 V to 3.6 V or GND		Full			0.1	µA

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.
(2) See *Output Pull-Down* .

7.6 Switching Characteristics: V_{IN} = 3.6 V

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	TPS22920	TPS22920L	UNIT
			TYP	TYP	
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V	970	663	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V	3	2	
t_r	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V	880	627	
t_f	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V	2	2	

7.7 Switching Characteristics: V_{IN} = 0.9 V

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	TPS22920	TPS22920L	UNIT
			TYP	TYP	
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V	840	840	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V	16	16	
t_r	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V	470	470	
t_f	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V	5	5	

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7.8 Typical DC Characteristics

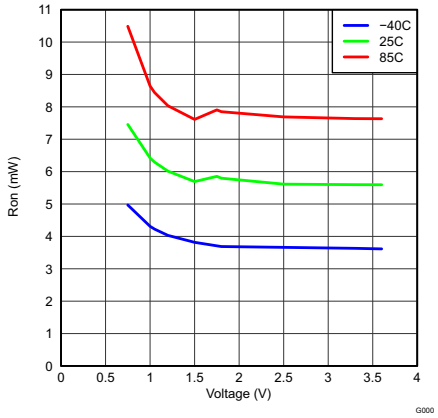


Figure 1. On-State Resistance vs Input Voltage

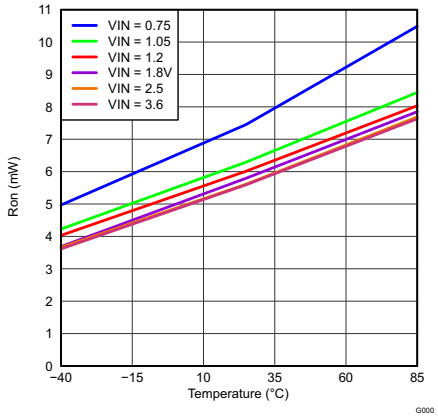


Figure 2. On-State Resistance vs Temperature

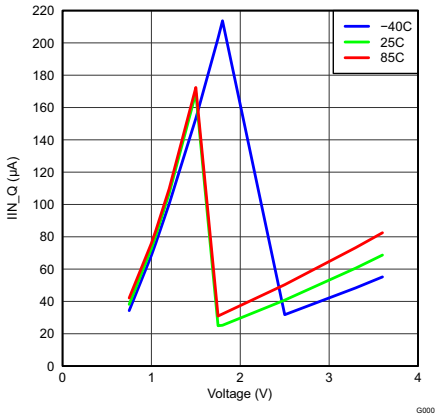


Figure 3. Input Current, Quiescent vs Input Voltage

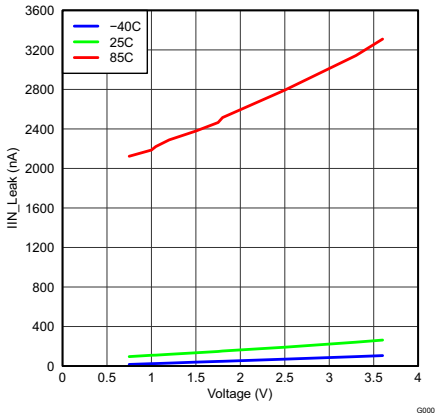


Figure 4. Input Current, Leak vs Input Voltage

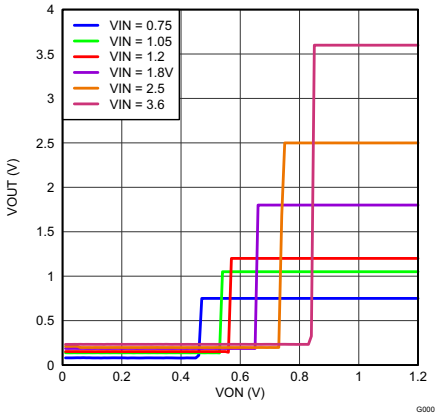


Figure 5. ON Input Threshold

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7.9 TPS22920 Typical AC Characteristics

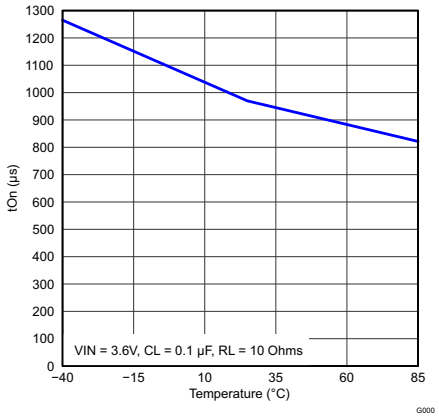


Figure 6. Turn-On Time vs Temperature

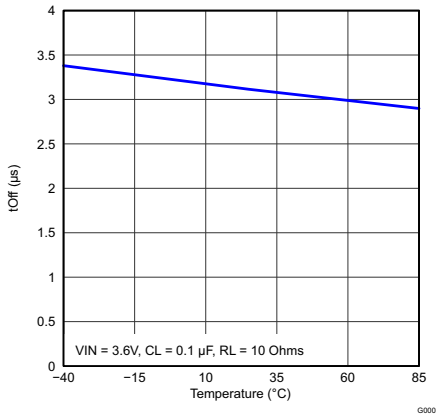


Figure 7. Turn-Off Time vs Temperature

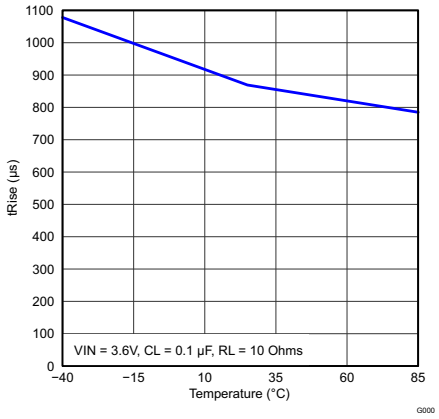


Figure 8. Rise Time vs Temperature

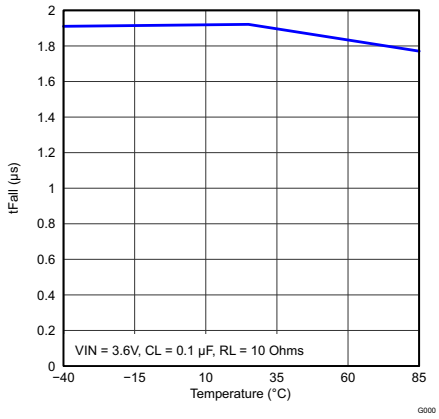


Figure 9. Fall Time vs Temperature

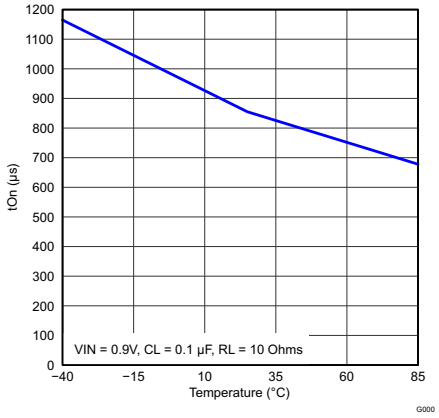


Figure 10. Turn-On Time vs Temperature

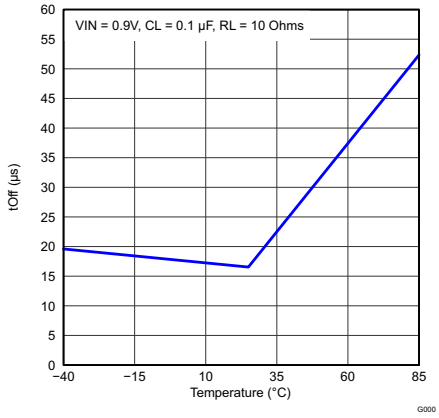


Figure 11. Turn-Off Time vs Temperature

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TPS22920 Typical AC Characteristics (continued)

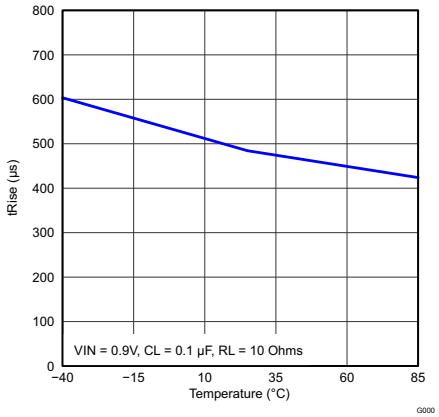


Figure 12. Rise Time vs Temperature

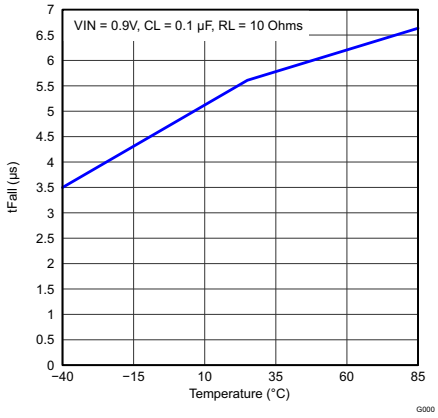


Figure 13. Fall Time vs Temperature

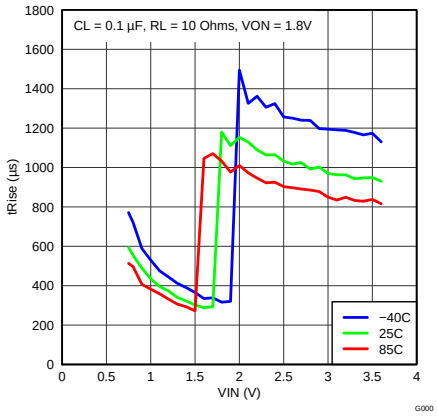


Figure 14. Rise Time vs Input Voltage

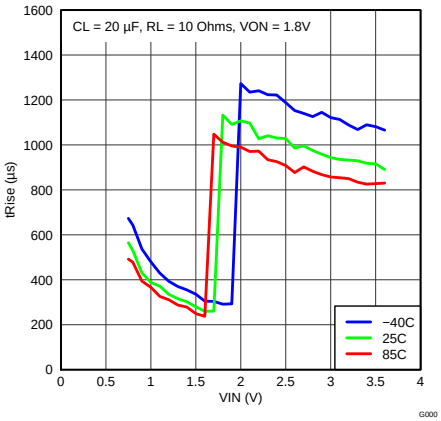
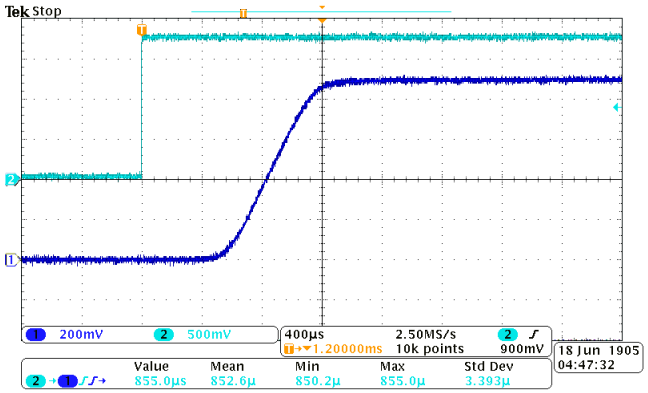
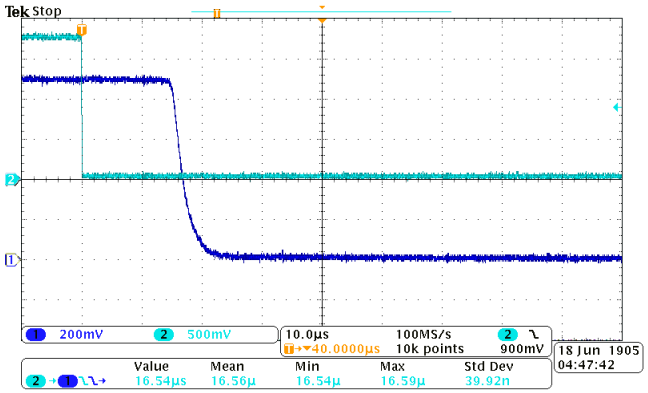


Figure 15. Rise Time vs Input Voltage



V_{IN} = 0.9 V C_{IN} = 1 µF RL = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 16. Turn-On Response

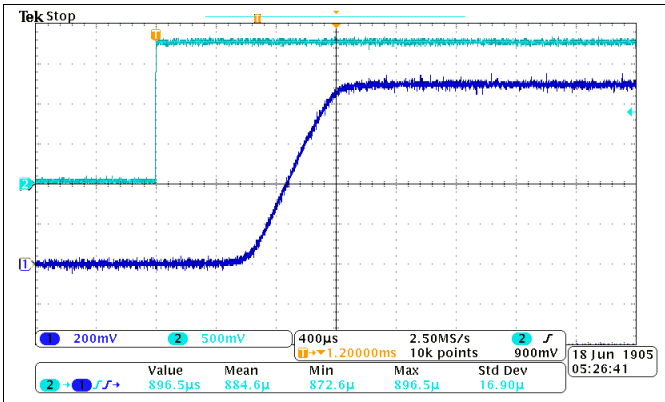


V_{IN} = 0.9 V C_{IN} = 1 µF RL = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 17. Turn-Off Response

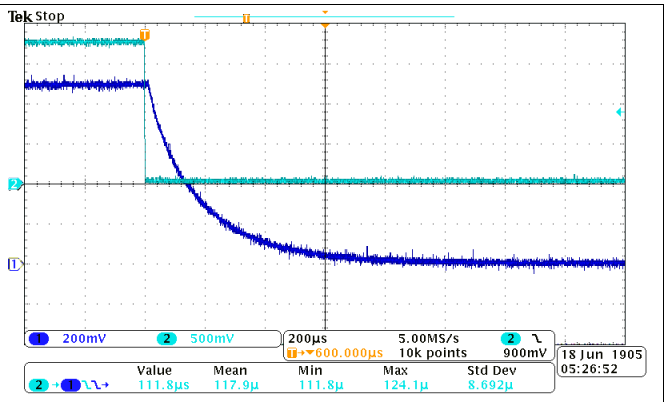
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TPS22920 Typical AC Characteristics (continued)



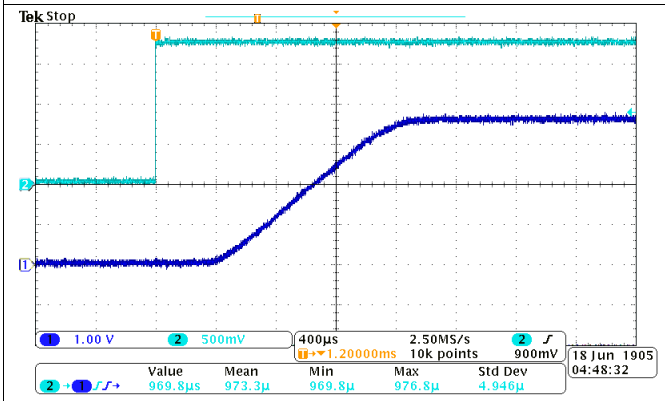
V_{IN} = 0.9 V C_{IN} = 47 µF RL = 10 Ω
T_A = 25°C C_L = 20 µF

Figure 18. Turn-On Response



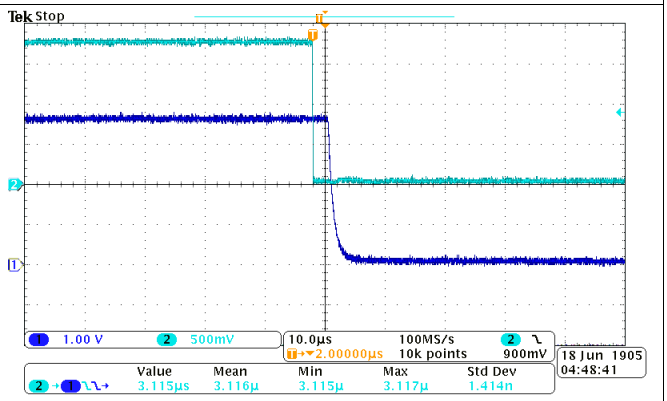
V_{IN} = 0.9 V C_{IN} = 47µF RL = 10 Ω
T_A = 25°C C_L = 20 µF

Figure 19. Turn-Off Response



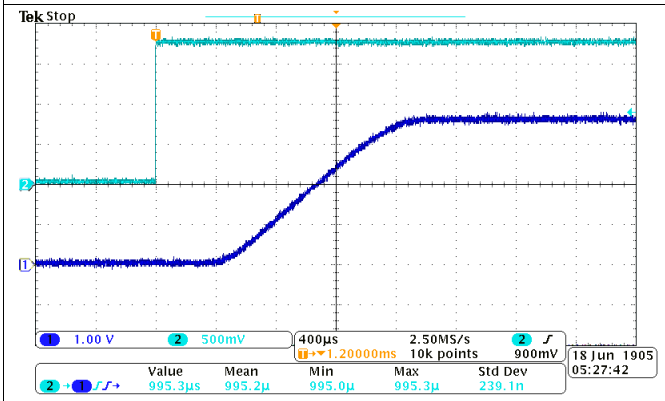
V_{IN} = 3.6V C_{IN} = 1 µF RL = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 20. Turn-On Response



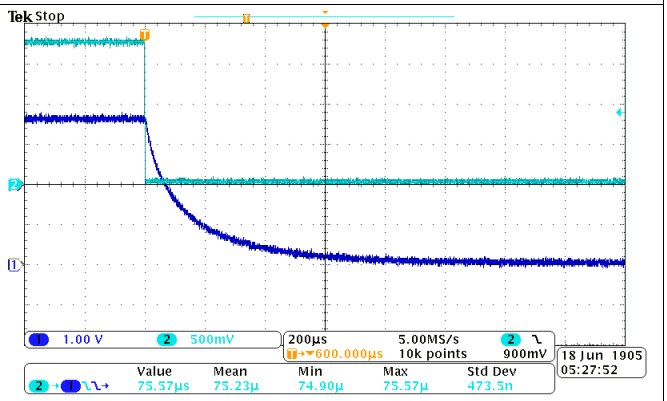
V_{IN} = 3.6 V C_{IN} = 1 µF RL = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 21. Turn-Off Response



V_{IN} = 3.6 V C_{IN} = 47 µF RL = 10 Ω
T_A = 25°C C_L = 20 µF

Figure 22. Turn-On Response



V_{IN} = 3.6 V C_{IN} = 47 µF RL = 10 Ω
T_A = 25°C C_L = 20 µF

Figure 23. Turn-Off Response

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7.10 TPS22920L Typical AC Characteristics

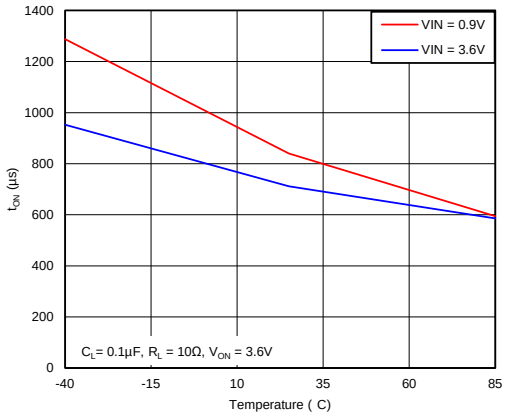


Figure 24. t_{ON} vs Temperature

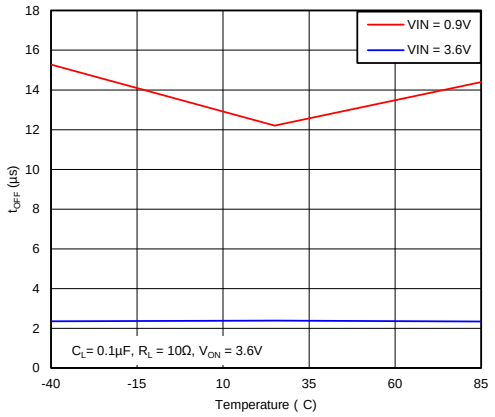


Figure 25. t_{OFF} vs Temperature

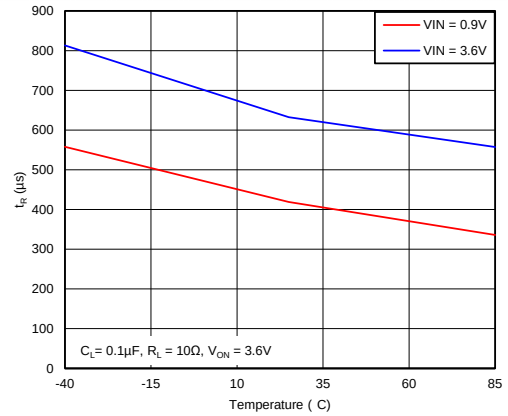


Figure 26. t_R vs Temperature

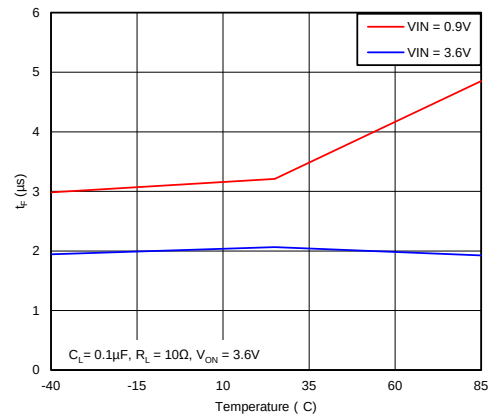


Figure 27. t_F vs Temperature

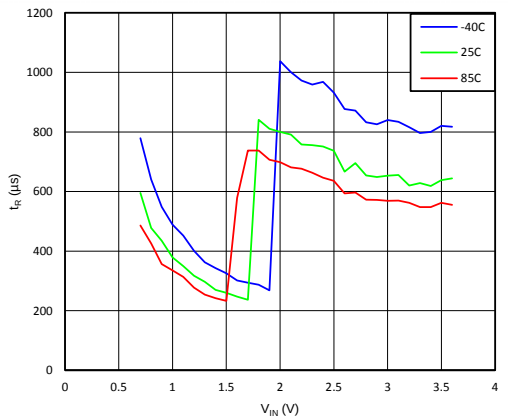


Figure 28. t_R vs V_{IN}

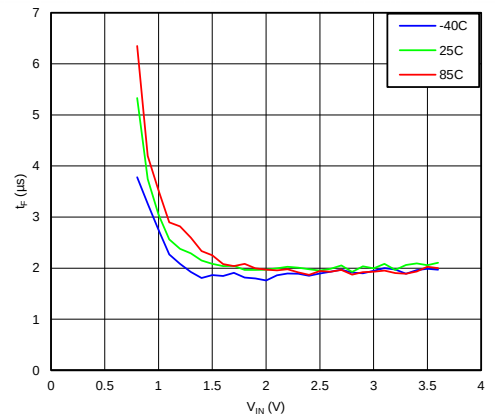


Figure 29. t_F vs V_{IN}

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TPS22920L Typical AC Characteristics (continued)

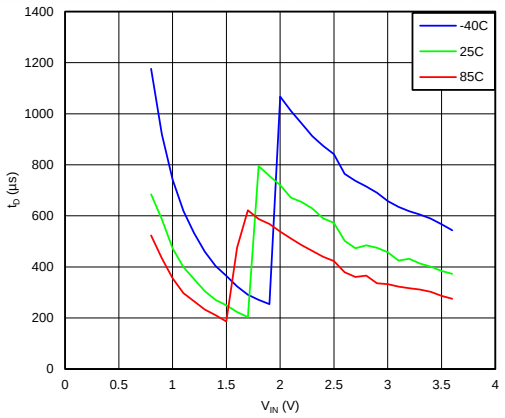


Figure 30. t_D vs V_{IN}

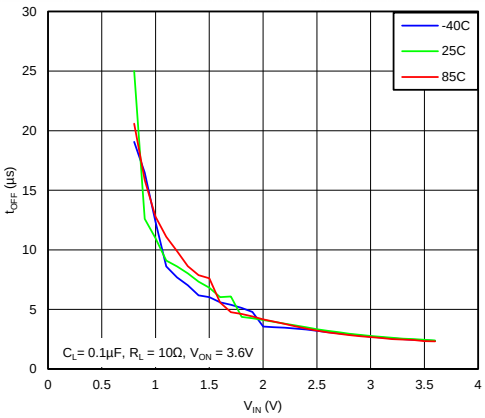


Figure 31. t_{OFF} vs V_{IN}

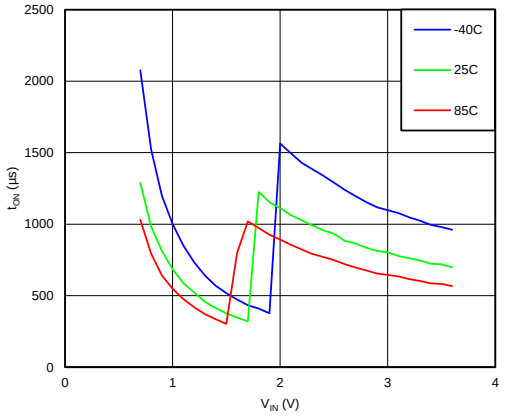
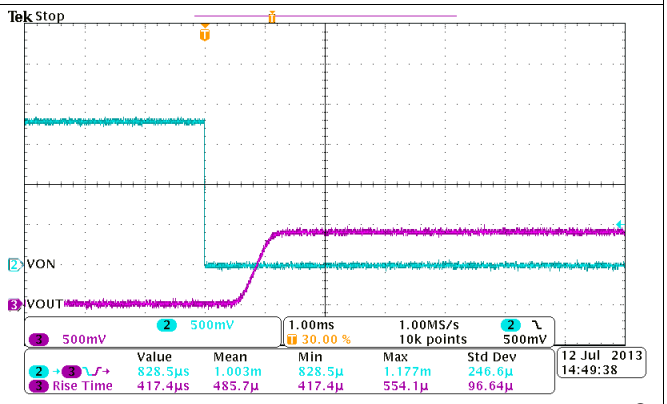
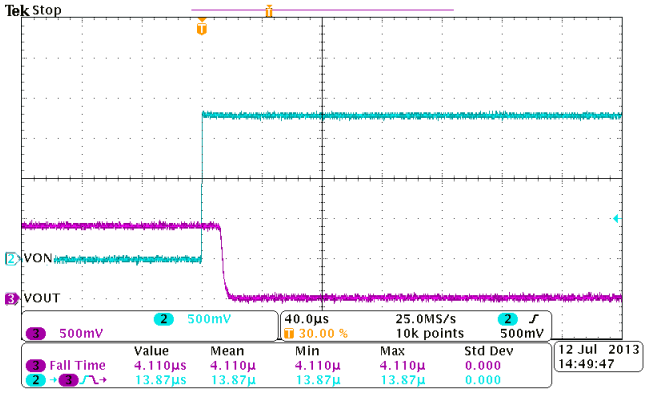


Figure 32. t_{ON} vs V_{IN}



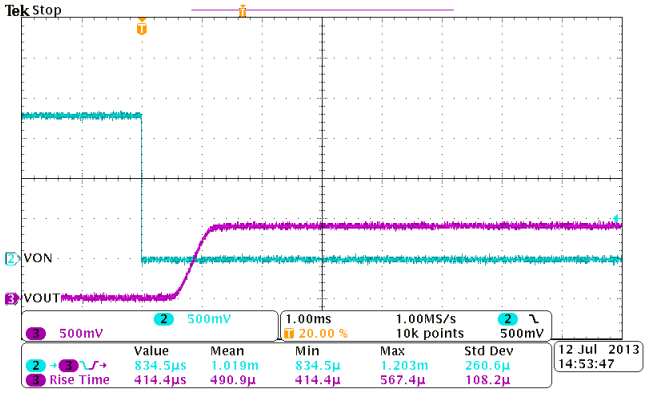
V_{IN} = 0.9 V C_{IN} = 1 µF R_L = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 33. Turn-On Response



V_{IN} = 0.9 V C_{IN} = 1 µF R_L = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 34. Turn-Off Response

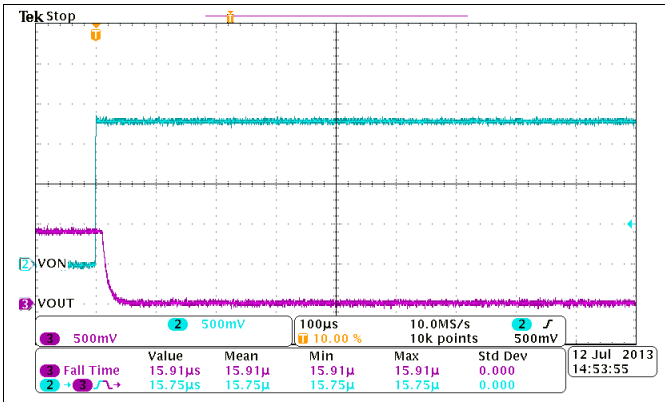


V_{IN} = 0.9 V C_{IN} = 10 µF R_L = 10 Ω
T_A = 25°C C_L = 1 µF

Figure 35. Turn-On Response

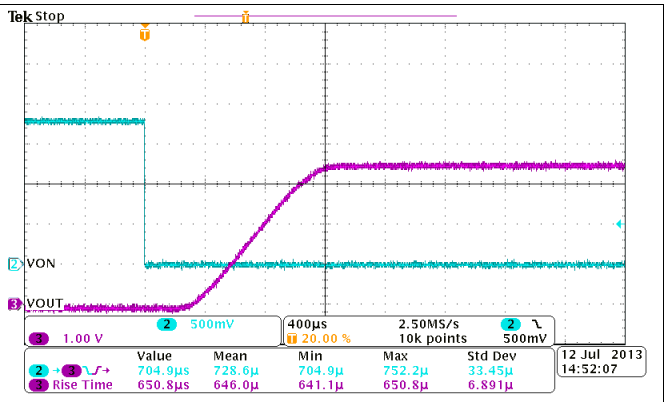
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TPS22920L Typical AC Characteristics (continued)



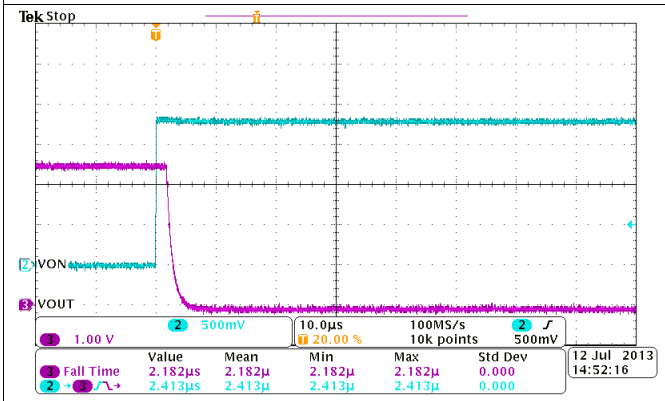
V_{IN} = 0.9 V C_{IN} = 10 µF R_L = 10 Ω
T_A = 25°C C_L = 1 µF

Figure 36. Turn-Off Response



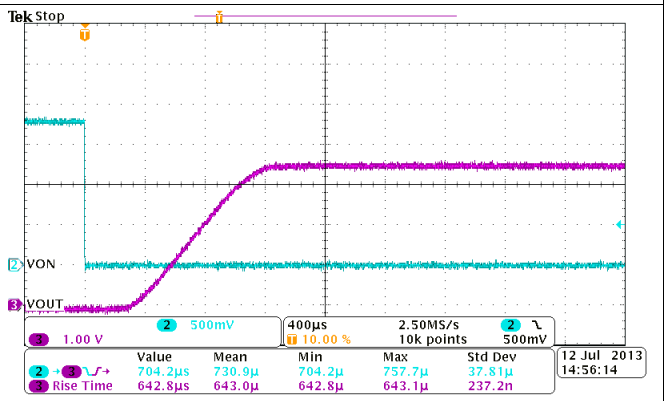
V_{IN} = 3.6 V C_{IN} = 1 µF R_L = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 37. Turn-On Response



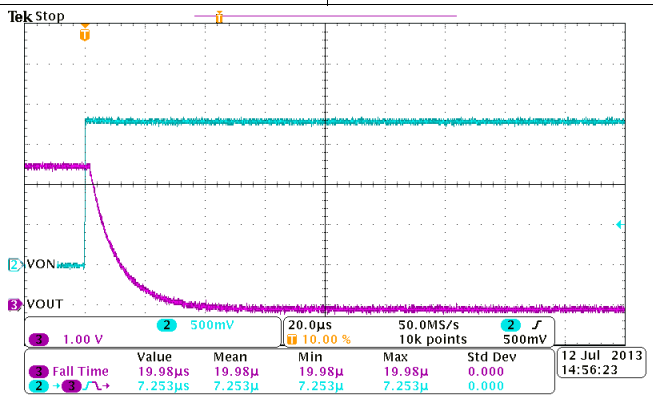
V_{IN} = 3.6 V C_{IN} = 1 µF R_L = 10 Ω
T_A = 25°C C_L = 0.1 µF

Figure 38. Turn-Off Response



V_{IN} = 3.6V C_{IN} = 10 µF R_L = 10 Ω
T_A = 25°C C_L = 1 µF

Figure 39. Turn-On Response

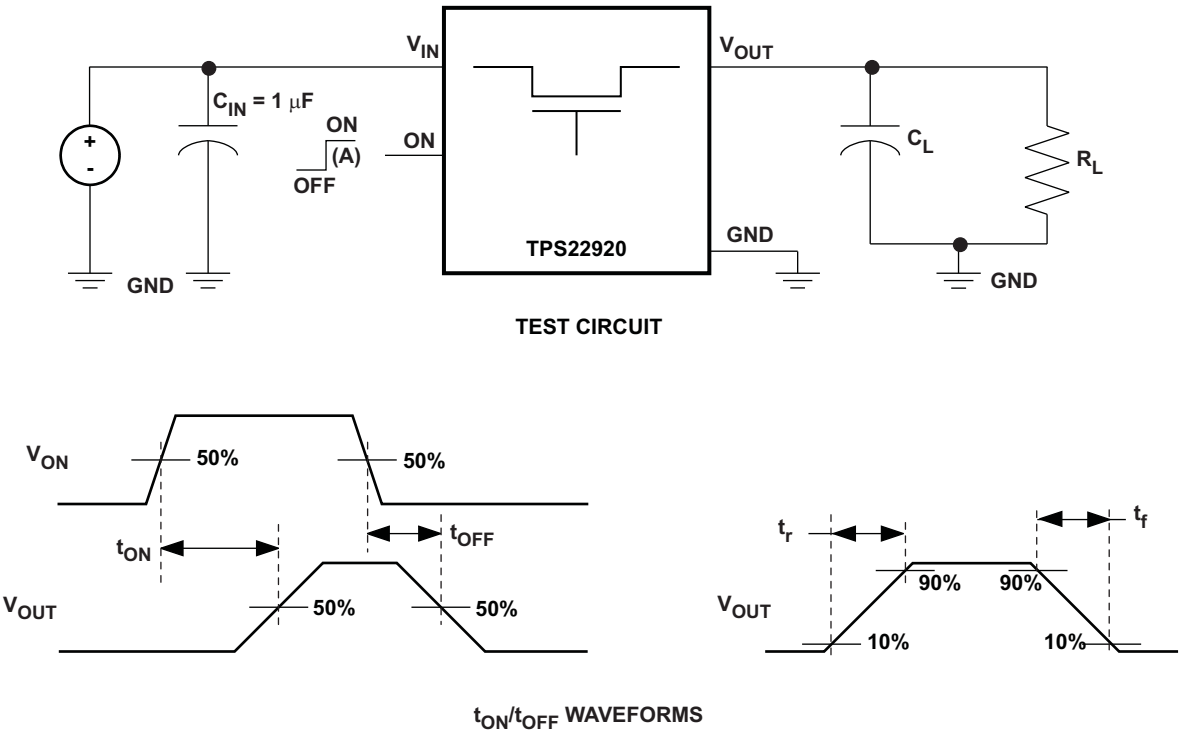


V_{IN} = 3.6 V C_{IN} = 10 µF R_L = 10 Ω
T_A = 25°C C_L = 1 µF

Figure 40. Turn-Off Response

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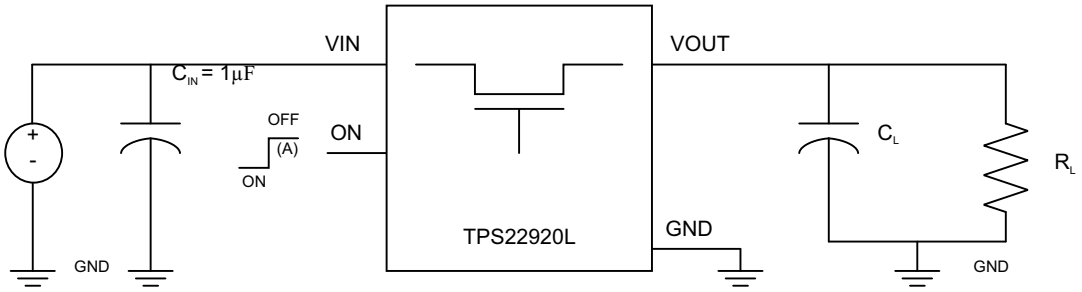
8 Parametric Measurement Information



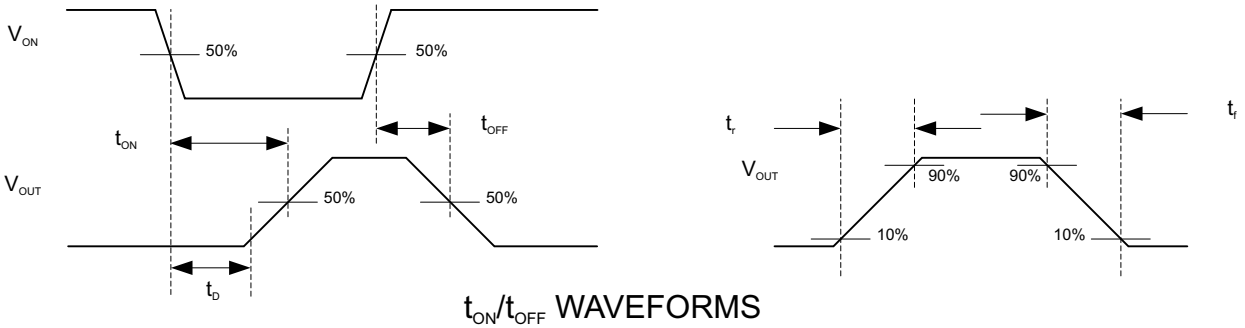
(A) Rise and fall times of the control signal is 100 ns.

Figure 41. TPS22920 Test Circuit and T_{ON}/T_{OFF} Waveforms

Parametric Measurement Information (continued)



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

A. Rise and fall times of the control signal is 100ns.

Figure 42. TPS22920L Test Circuit and t_{ON}/t_{OFF} Waveforms

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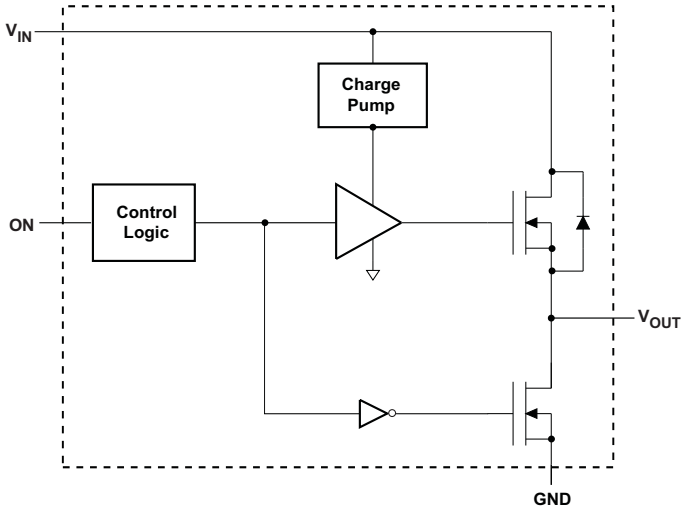
9 Detailed Description

9.1 Overview

The TPS22920x is a single channel, 4-A load switch in a small, space-saving CSP-8 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

This device is also designed to have very low leakage current during off state, which prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pin controls the state of the switch. For TPS22920, asserting ON high enables the switch. For TPS22920L, asserting ON low enables the switch. ON has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

9.3.2 Output Pull-Down

The output pull-down is active when the user is turning off the main pass FET. The pull-down discharges the output rail to approximately 10% of the rail, and then the output pull-down is automatically disconnected to optimize the shutdown current.

9.4 Device Functional Modes

ON	TPS22920		TPS22920L	
	V_{IN} to V_{OUT}	V_{OUT} to GND(1)	V_{IN} to V_{OUT}	V_{OUT} to GND(1)
Logic Low	OFF	ON	ON	OFF
Logic High	ON	OFF	OFF	ON

(1) See *Output Pull-Down* .

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

10.1.2 Output Capacitor

A C_{IN} greater than C_L is highly recommended due to the integral body diode in the NMOS switch. A C_L greater than C_{IN} can cause V_{OUT} to exceed VIN when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

10.2 Typical Application

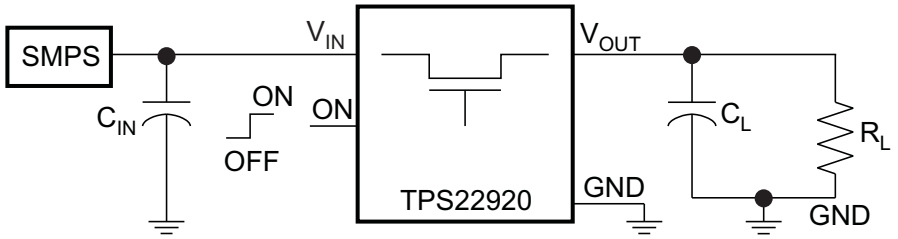


Figure 43. Typical Application Circuit

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
C_L	4.7 µF
Maximum Acceptable Inrush Current	40 mA

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10.2.2 Detailed Design Procedure

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN condition of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- ΔV = Voltage drop from VIN to VOUT
- I_{LOAD} = Load current
- R_{ON} = On-resistance of the device for a specific V_{IN}
- An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Managing Inrush Current

The output capacitors must be charged up from 0-V to V_{IN} when the switch is enabled. This charge arrives in the form of inrush current. Inrush current may be calculated using the following equation:

$$\text{Inrush Current} = C \times \frac{dv}{dt} \quad (2)$$

where

- C = Output capacitance
- $\frac{dv}{dt}$ = Output slew rate

The TPS22920x offers a very slow controlled rise time for minimizing inrush current. This device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. An output capacitance of 4.7 µF will be used since the amount of inrush increases with output capacitance:

$$40\text{mA} = 4.7\mu\text{F} \times \frac{dv}{dt} \quad (3)$$

$$\frac{dv}{dt} = 8.5\text{V/ms} \quad (4)$$

A device with a slew rate less than 8.5 V/ms must be used to ensure an inrush current of less than 40 mA.

The TPS22920 has a typical rise time of 880 µs at 3.3 V. This results in a slew rate of 3.75 V/ms which meets the *Design Requirements*.

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10.2.3 Application Curves

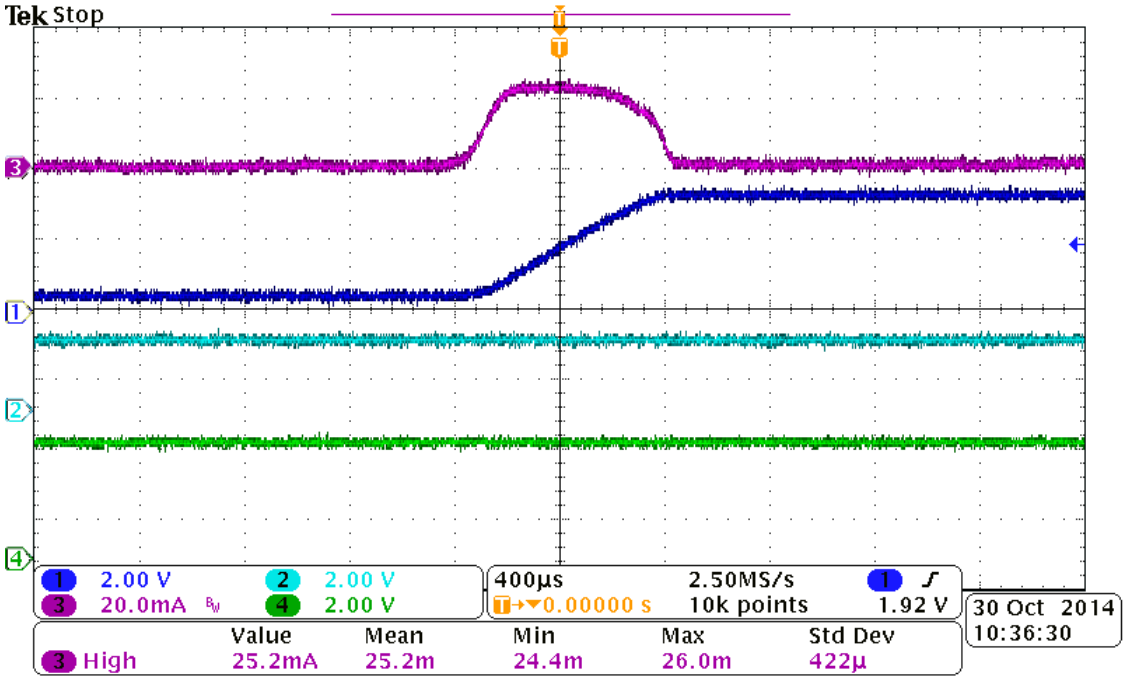


Figure 44. TPS22920 Inrush Current With 4.7-µF Output Capacitor

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11 Power Supply Recommendations

The device is designed to operate from a VIN range of 0.75 V to 3.6 V. The VIN power supply must be well regulated and placed as close to the VIN terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using the minimum recommended input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

12 Layout

12.1 Layout Guidelines

All traces should be as short as possible for best performance. The input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

12.2 Layout Example

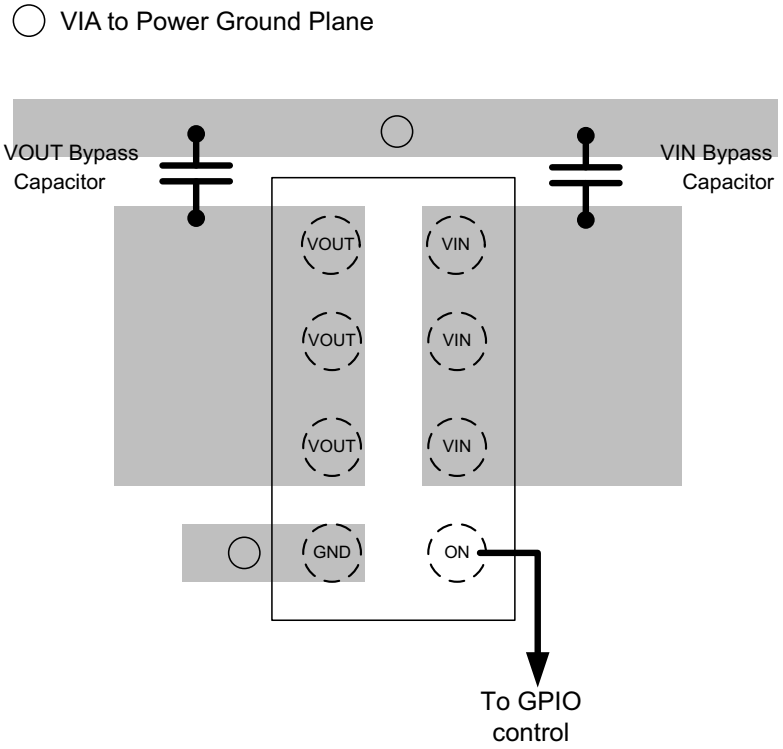


Figure 45. Package Layout Example

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22920	Click here	Click here	Click here	Click here	Click here
TPS22920L	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22920LYZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DV	Samples
TPS22920LYZPT	ACTIVE	DSBGA	YZP	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DV	Samples
TPS22920YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z	Samples
TPS22920YZPRB	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z S	Samples
TPS22920YZPT	ACTIVE	DSBGA	YZP	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

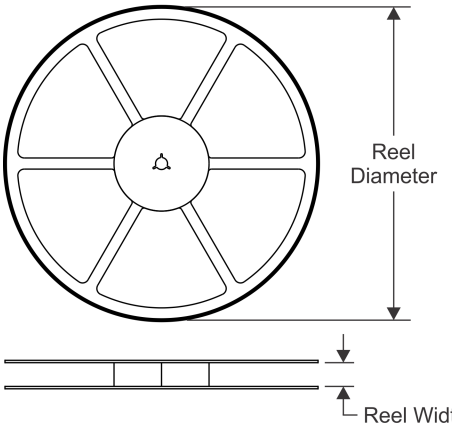
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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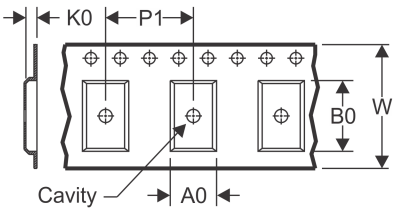
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

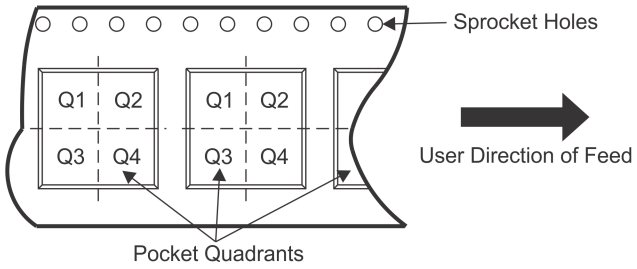


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

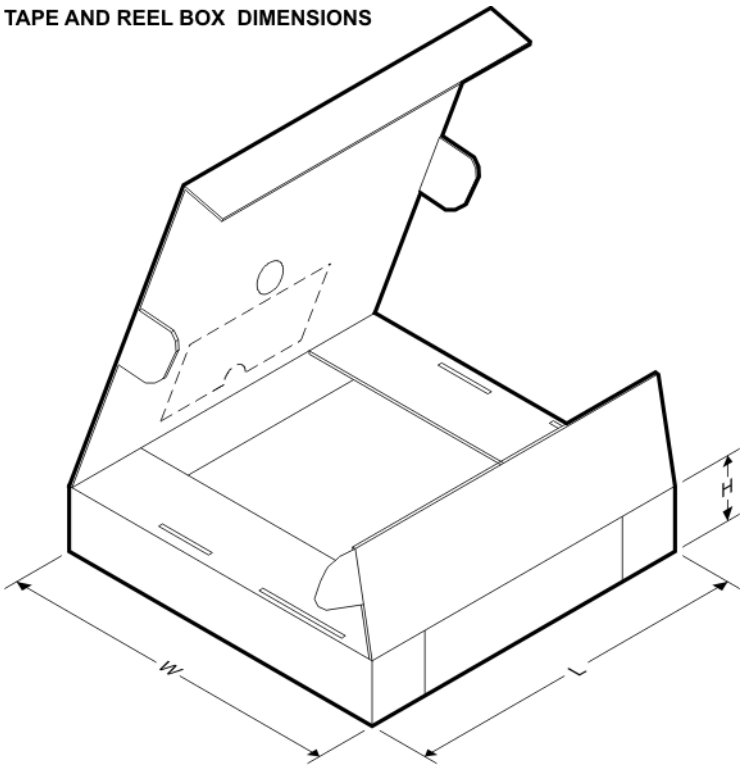
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22920LYZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920LYZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPRB	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

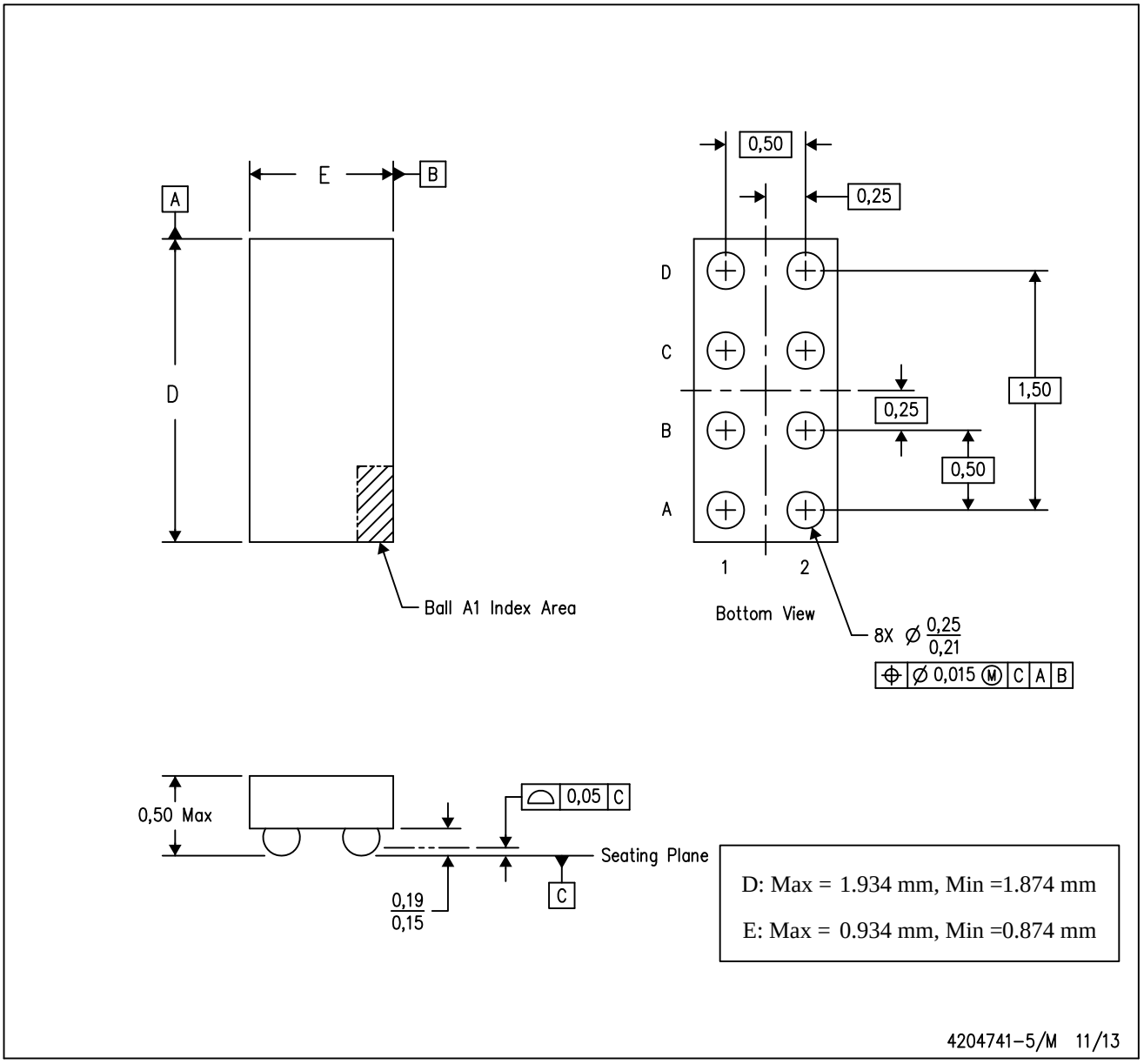
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22920LYZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920LYZPT	DSBGA	YZP	8	250	182.0	182.0	20.0
TPS22920YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920YZPRB	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920YZPT	DSBGA	YZP	8	250	182.0	182.0	20.0

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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