19-3031; Rev 0; 1988

MAXIM

Chopper Stabilized Operational Amplifier

General Description

The Maxim ICL7652 is a chopper-stabilized amplifier, ideal for applications requiring low-level signal amplification and conditioning. This device offers distinct performance advantages over the ICL7650, including improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are slightly reduced.

The ICL7652 virtually eliminates the V_{OS} error term in system error calculations, eliminating the reliability and cost problems associated with potentiometer adjustments. In addition, the 0.01μV/°C V_{OS} drift specification and the excellent long term offset stability eliminate the need for periodic V_{OS} trimming.

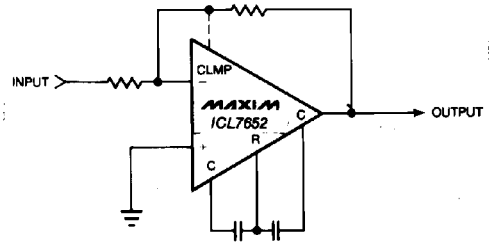
The offset nulling circuit for the 8-lead ICL7652 is controlled by an internal oscillator circuit. The 14-lead version offers the capability of connecting an external oscillator to control the V_{OS} nulling operation. The 14-lead device has an output voltage clamp circuit to minimize overload recovery time.

Applications

The ICL7652 is ideal for all preamplifier circuit applications where low offset voltage is critical and periodic adjustment of the offset is difficult or inaccessible.

Precision Amplifier
Instrumentation Amplifier
Thermocouple Amplifier
Thermistor Amplifier
Strain Gauge Amplifier

Typical Operating Circuit



Inverting Amplifier
with Optional Clamp

(Detailed Circuit Diagram — Figure 5)

Features

- Improved 2nd Source! (See 3rd page for "Maxim Advantage™").
- Low Input Noise Voltage 0.2μV_{p-p}(DC-1Hz)
- Low Offset Voltage: 5μV Max.
- Low DC Input Bias Current: 30pA Max.
- High Gain, CMRR and PSRR (110dB Min.)
- Compensated for Unity Gain Operation
- Excellent Long Term Offset Stability (<100nV/$\sqrt{\text{month}}$)
- Monolithic, Low Power CMOS Design

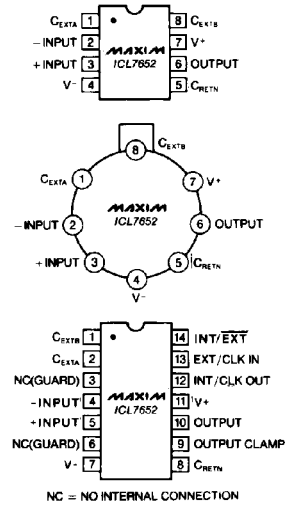
Ordering Information

PART	TEMP RANGE	PACKAGE
ICL7652CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7652CPD	0°C to +70°C	14 Lead Plastic DIP
ICL7652CTV	0°C to +70°C	TO-99 Metal Can
ICL7652IJA	-20°C to +85°C	8 Lead CERDIP
ICL7652IJD	-20°C to +85°C	14 Lead CERDIP
ICL7652ITV	-20°C to +85°C	TO-99 Metal Can
ICL7652C/D	0°C to +70°C	Dice
ICL7652CWE	0°C to +70°C	16 Lead Wide S.O.

NOTE: All devices listed above are available in B versions. Order part number ICL7652B ___.

Pin Configurations

Top View



NC = NO INTERNAL CONNECTION

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

MAXIM is a registered trademark of Maxim Integrated Products.

Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3) to (V^- - 0.3) V
Storage Temperature Range ..... -65°C to 160°C
Operating Temperature Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite

Current into Any Pin 10mA
— while operating (Note 4) 100μA
Continuous Total Power Dissipation (T_A = +25°C)
CERDIP Package (Maxim) 500mW
Plastic Package 375mW
TO-99 Metal Can 250mW
Small Outline 350mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - ICL7652

(V^+ = +5V, V^- = -5V, T_A = +25°C, Test circuit unless noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{OS}	T_A = +25°C		±0.7	±5	μV
		Over Operating Temperature Range (Note 1)		±1.0		
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Operating Temperature Range (Note 1)		0.01	0.05	μV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_{BIAS}	T_A = +25°C		15	30	pA
		0°C ≤ T_A ≤ +70°C		35		
		-20°C < T_A < +85°C		100		
Input Offset Current	I_{OS}	T_A = +25°C		25	60	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±4V,	120	150		dB
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
Common-Mode Voltage Range	CMVR		-4.3	-4.8 to +4.0	3.5	V
Common-Mode Rejection Ratio	CMRR	CMVR = -4.3V to +3.5V	110	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	110	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω, DC to 1Hz		0.2		μV_{p-p}
		DC to 10Hz		0.7		
Input Noise Current	i_n	f = 10Hz		0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		0.5		V/μs
Rise Time	t_r			0.8		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	I_{SUPP}	No Load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	100		μA
Clamp OFF Current (Note 2)		-4.0V < V_{OUT} < +4.0V		1		pA
Offset Voltage vs Time				100		$nV/\sqrt{month}$

Note 1: Operating temperature range for I series parts is -20°C to +85°C, for C series is 0°C to +70°C.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs. clamp current characteristics.
Note 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this not guaranteed.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Chopper Stabilized Operational Amplifier

- **Key Parameters Guaranteed Over Temperature**
- **Lower Supply Current**
- **Improved ESD Protection (Note 5)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS This device conforms to the Absolute Maximum Ratings on adjacent page.

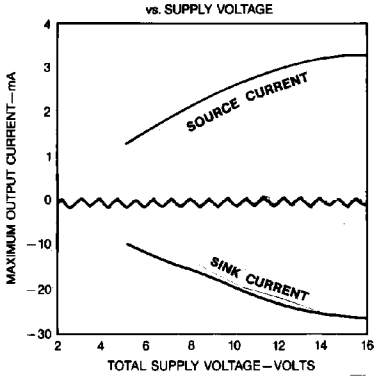
ELECTRICAL CHARACTERISTICS The ICL7652 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, T_A = +25°C, Test circuit, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C ICL7652 — Over Temperature Range ICL7652B (below) **-20°C ≤ T_A ≤ +40°C (Note 1)** **-20°C ≤ T_A ≤ +70°C (Note 1, 7)** **+70°C ≤ T_A ≤ +85°C (Note 1, 7)**		±0.7 ±1.0 **±1.0** **±2.0** **±5.0**	±5.0 **±6.25** **±7.25** **±15**	µV
Average Temperature Coefficient of Input Offset Voltage (Note 1)	$\frac{\Delta V_{OS}}{\Delta T}$	ICL7652 — Over Temperature Range ICL7652B (below) -20°C ≤ T_A ≤ +40°C -20°C ≤ T_A ≤ +70°C (Note 1, 7) +70°C ≤ T_A ≤ +85°C (Note 1, 7)		0.01 0.01 0.01 0.1	0.05 0.05 0.1 0.5	µV/°C
Input Bias Current (Note 6) (Doubles every 10°C above approximately 60°C)	I_{BIAS}	T_A = +25°C **0°C ≤ T_A ≤ +70°C** **-20°C ≤ T_A ≤ +85°C**		15 **35** **100**	30 **100** **200**	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±4V, T_A = +25°C **0°C ≤ T_A ≤ +70°C** **-20°C ≤ T_A ≤ +85°C**	120 **114** **114**	150 **140** **140**		dB
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ R_L = 100kΩ	±4.7	±4.85 ±4.95		V
Common-Mode Voltage Range	**CMVR**	**Over Temperature Range (Note 1)**	**-4.3**	**-4.8 to +4.0**	**3.5**	V
Common-Mode Rejection Ratio	**CMRR**	CMVR = -4.3V to +3.5V, T_A = +25°C **Over Temperature Range (Note 1)**	110 **104**	130 **125**		dB
Power Supply Rejection Ratio	**PSRR**	±3V to ±8V, T_A = +25°C **Over Temperature Range (Note 1)**	110 **104**	130 **125**		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω, DC to 1Hz DC to 10Hz		0.2 0.7		μV_{p-p}
Input Noise Current	i_n	f = 10Hz		0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		0.5		V/µs
Rise Time	t_r			0.8		µs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	I_{SUPP}	**No Load, T_A = +25°C** **Over Temperature Range (Note 1)**		**1.5** **2.0**	**2.0** **3.5**	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	100		µA
Clamp OFF Current (Note 2)		-4.0V ≤ V_{OUT} ≤ +4.0V		1		pA
Offset Voltage vs Time				100		$nV/\sqrt{month}$

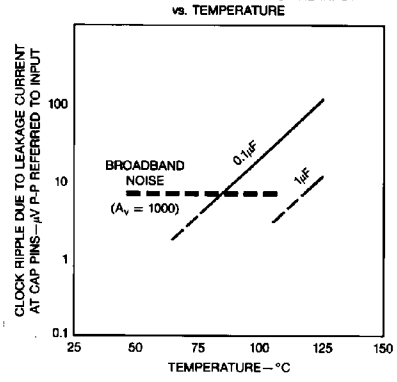
Note 1: Operating temperature range for "I" series parts is -20°C to +85°C, for C series is 0°C to +70°C. This parameter is guaranteed by test correlation.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs. clamp current characteristics.
Note 4: Limiting input current to 100µA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
Note 5: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)
Note 6: $I_{OS} = 2 \cdot I_{BIAS}$.
Note 7: With $C_{EXTA} = C_{EXTB} = 1.0\mu F$

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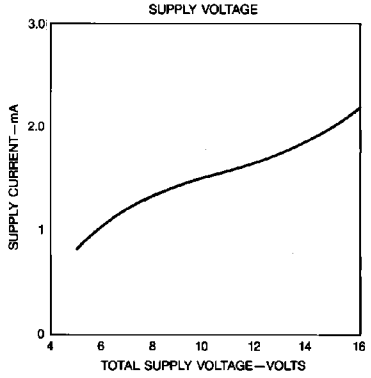
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



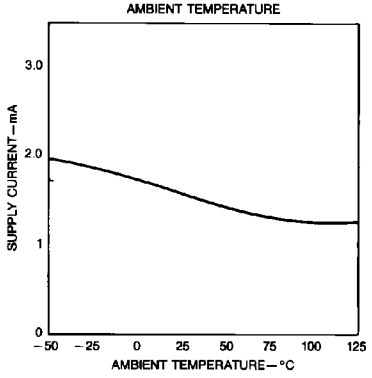
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



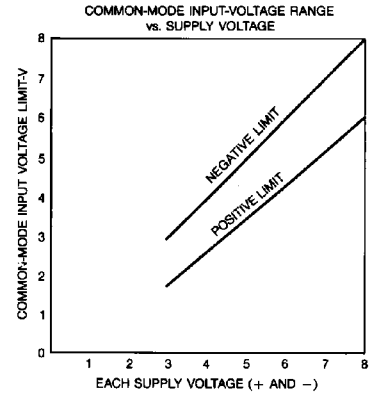
SUPPLY CURRENT vs. SUPPLY VOLTAGE



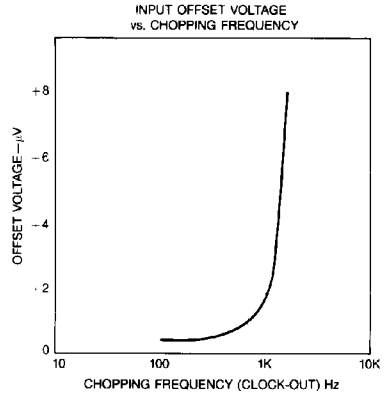
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



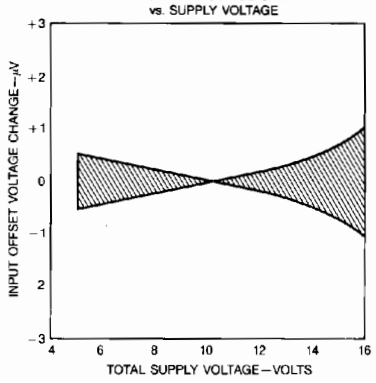
COMMON-MODE INPUT-VOLTAGE RANGE vs. SUPPLY VOLTAGE



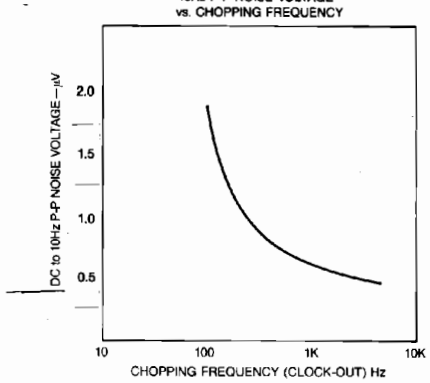
INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY



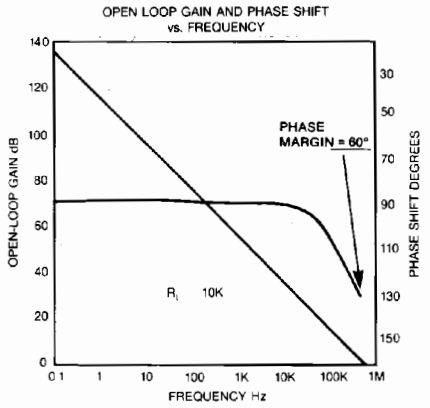
INPUT OFFSET VOLTAGE CHANGE
vs. SUPPLY VOLTAGE



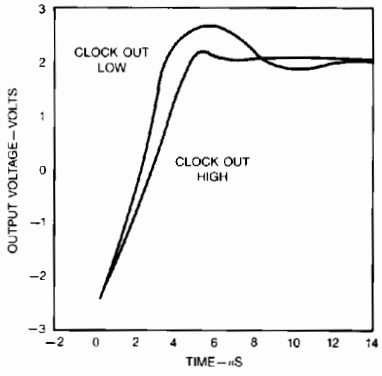
10Hz P-P NOISE VOLTAGE
vs. CHOPPING FREQUENCY



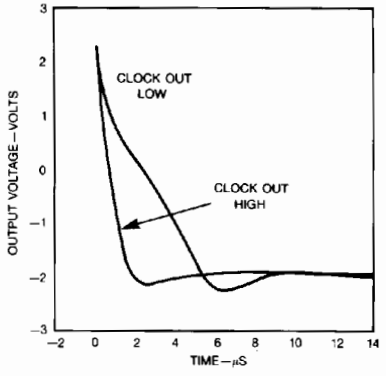
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



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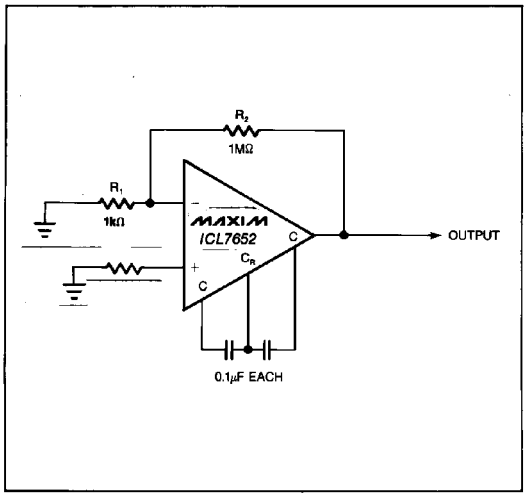


Figure 1. Maxim ICL7652 Test Circuit

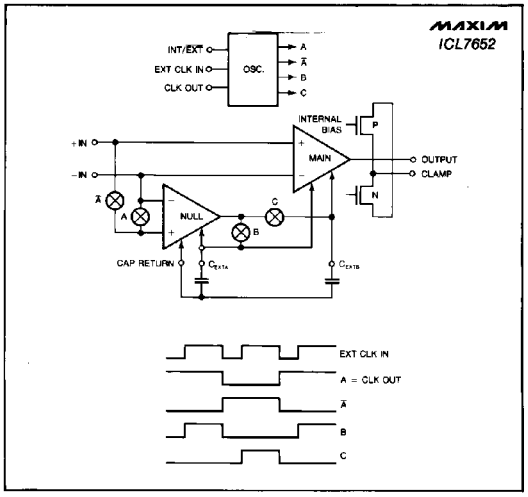


Figure 2. Maxim ICL7652 Block Diagram

Detailed Description

Amplifier

Figure 2 shows the major elements of the ICL7652. Two amplifiers are illustrated, the main amplifier and the nulling amplifier, both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling arrangement, which is independent of the output level, operates over the full power supply and common mode ranges. This device exhibits exceptionally high CMRR, PSRR and A_{VOL}. The nulling connections, which are MOSFET back gates, have inherently high impedance. The two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants.

The chopper frequency charge injection at the input terminals is minimized by careful balance of the input switches. The feed forward-type injection into the compensation capacitor is also minimized. This is the main cause of spikes at the output in this type of circuit.

Output Clamp

This pin allows for reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the summing junction, or to the inverting input pin, a current path between this point and the output occurs just before the output device saturates. This avoids uncontrolled input differential and the consequent charge build-up on the correction-storage capacitors. There is only a slight reduction in the output swing.

Intermodulation

The effects of intermodulation between chopper frequency and input signals have been a problem with previous chopper stabilized amplifiers. These effects are present because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is detected by the zeroing circuit as an error signal. This signal is chopped and fed back, thus injecting sum and difference frequencies. This causes disturbances in the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7652. This reduction is achieved by feeding the nulling circuit with a dynamic current which corresponds to the compensation capacitor current. The intermodulation and gain/phase disturbances in the ICL7652 are held to very low values, and generally can be ignored.

Nulling Capacitor Connection

The C_{EXTA} and C_{EXTB} pins should be connected to the null-storage capacitors, with the common connection made to the C_{RETN}. The outside foil of the capacitors should be connected to C_{RETN}.

Clock Operation

A frequency of 400Hz is generated by the internal oscillator of the ICL7652. This is available at the CLK OUT pin on the 14-lead device. The use of an external clock is also available on these parts. The INT/EXT pin may be left open for normal operation due to the internal pull-up. However, the internal clock must be disabled and this pin must be tied to V^- if an external clock is desired. An external clock signal may then be applied to the EXT CLK IN pin. The duty cycle of the external clock is not critical at low frequencies, since an internal divide by two provides the desired 50% switching duty cycle. However, a 50% to 80% positive duty cycle is preferred for frequencies above 500Hz, since the capacitors are charged only when EXT CLK IN is HIGH. This ensures that any transients have time to settle before the capacitors are turned OFF. The external clock can swing between V^+ and GROUND or V^+ and V^-, and has a logic threshold of about $V^+ - 2.5V$.

To avoid a capacitor imbalance during overload, a strobe signal may be used. Neither capacitor will be charged if a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier. A typical amplifier will drift less than 10μV/s since the leakage of the capacitor pins is quite low at room temperature. Relatively long measurements may be made with little change in offset.

Applications

Output Stage/Load Driving

The ICL7652 is in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. This behavior is apparent when loads are less than the high impedance stage of the output (approximately 18kΩ). The open loop gain, for example, will be 17dB lower with a 1kΩ load than with a 10kΩ load. This lower gain is of little consequence if the amplifier is used strictly for DC, since the DC gain is typically greater than 120dB even with a 1kΩ load. For wideband applications, however, the best frequency response will be achieved with a load resistor of 10kΩ or higher. The result will be a smooth 6dB/octave response from 0.1Hz to 0.5MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Component Selection

C_{EXTA} and C_{EXTB}, the two required external capacitors, have optimum values depending on the clock or chopping frequency. The correct value is 0.1 to 1μF for the preset internal clock frequency. The capacitor value should be scaled proportionally to the relationship between the chopping frequency and the nulling time constant if an external clock is used. A ceramic or other low grade capacitor may prove suitable for many applications, however, a high-quality film-type capacitor such as mylar is preferred. Low dielectric absorption capacitors (such as polypropylene) should be used for lowest settling on initial turn-on. Several seconds may be required to settle to 1μV with ceramic capacitors.

Static Protection

Input diodes provide static protection for all device pins. Strong static fields and discharges, however, should be avoided, as they can cause degraded diode junction characteristics which may result in increased input leakage currents.

Latch-up Avoidance

A parasitic four-layer (p-n-p-n) structure which has characteristics similar to an SCR is a characteristic of a junction-isolated CMOS circuit. This junction may be triggered into a low impedance state under certain circumstances which results in excessive supply current. In an effort to avoid this condition, no voltages greater than 0.3V beyond the supply rails should be applied to any pin. Generally the amplifier supplies should be established either at the same time or before any input signals are applied. However, if this is not possible, the drive circuits should limit the input current flow to under 1mA to avoid latch-up, even under fault conditions.

Thermo-electric Effects

Thermo-electric effects developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc., ultimately limit precision DC measurements. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide it is essential to take special precautions to avoid temperature gradients. All components should be shielded from air movement, especially that caused by power dissipating elements. Power supply voltages and power dissipation should be kept to a minimum, and low thermo-electric coefficient connections should be used where possible. Separation from surrounding heat dissipating elements is advised, and high impedance loads are preferable.

Chopper Stabilized Operational Amplifier

Input Guarding

Low leakage, high impedance, CMOS inputs allow the ICL7652 to make measurements of high impedance sources. Stray leakage paths can decrease input resistance and increase input currents unless inputs are guarded. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. The board should be coated with epoxy or silicone rubber after cleaning to prevent contamination.

Leakage currents may cause trouble even with properly cleaned and coated boards, particularly since the input pins are adjacent to pins that are at supply potentials. A significant reduction in leakage can be accomplished by using guarding to lower the voltage difference between the inputs and adjacent metal runs. By using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board, input guarding of the 8-lead TO-99 package is accomplished. A conductive ring surrounding the inputs, forming a guard, is connected to a low-impedance point that is approximately the same voltage as the inputs. The guard then absorbs the leakage current from the high voltage pins. Typical guard connections are shown in Figure 3.

The 14-lead DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are not used.

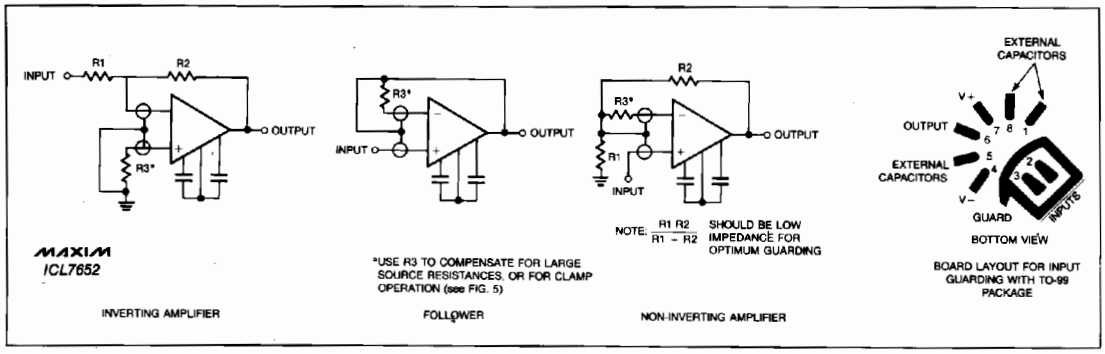


Figure 3. Input Guard Connection

Pin Compatibility

The 8-pin dip of the ICL7652 generally corresponds to that of the industry standard 8-pin devices, μA741, LM101, etc. However, the external null storage capacitors are connected to pins 1 and 8, whereas on most operational amplifiers these are left open or used for offset null or compensation capacitors.

The OP-05 and OP-07 operational amplifiers can also be converted for ICL7652 operation. This can be accomplished by replacing the offset-null potentiometer between pins 1 and 8, and V^+ by two capacitors from those pins to V^-. For LM108 pinout devices, the compensation capacitor is replaced by the external nulling capacitors.

Typical Applications

The ICL7652 is the optimal circuit solution whenever the performance of the system requires significant improvements in the reduction of the input offset voltage and bias currents. Figure 6 illustrates the use of a clamp circuit in a non-inverting amplifier. Since the clamp circuit forces the inverting input to follow the input signal, the usual problems in using a chopper-stabilized amplifier in this application are avoided.

Figures 5 and 6 illustrate basic inverting and non-inverting amplifier circuits. An output clamping circuit is used in both circuits to enhance the overload recovery performance. The supply voltage (± 8V max) and the output drive capability (10kΩ load for full swing) are the only limitations on the replacement of other operational amplifiers by the ICL7652. By using a simple booster circuit, these limitations may be overcome (Figure 7). This enables the full output capabilities of the μA741 (or any other standard device) to be combined with the input capabilities of the ICL7652. Because these devices form a composite amplifier, the loop gain stability should be watched carefully when the feedback network is added.

The provision for lower supply voltages is required when interfacing the ICL7652 with circuits that operate at ± 15V supplies. One approach is to use a highly-efficient voltage divider. This is illustrated in Figure 8 where Maxim's ICL7660 voltage converter is utilized in a backwards fashion.

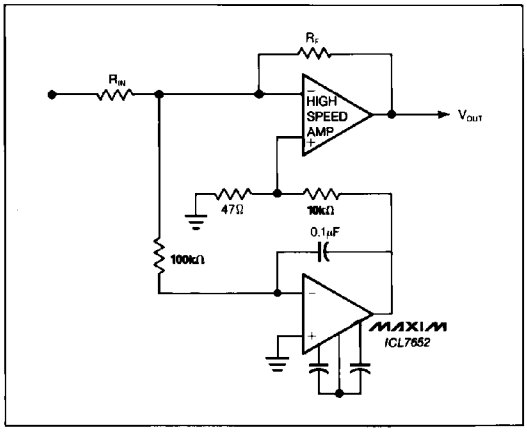


Figure 4. Nulling a High Speed Amplifier

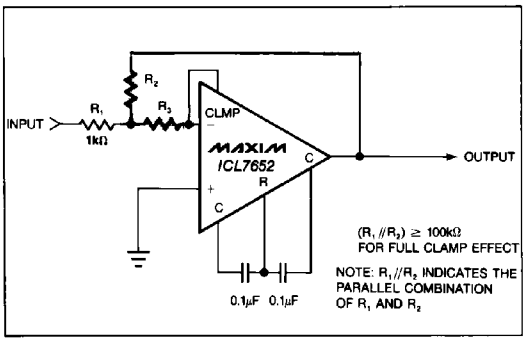


Figure 5. Inverting Amplifier with Optional Clamp

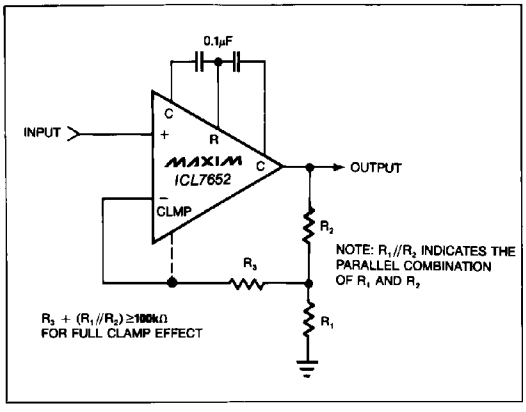


Figure 6. Non-Inverting Amplifier with Optional Clamp

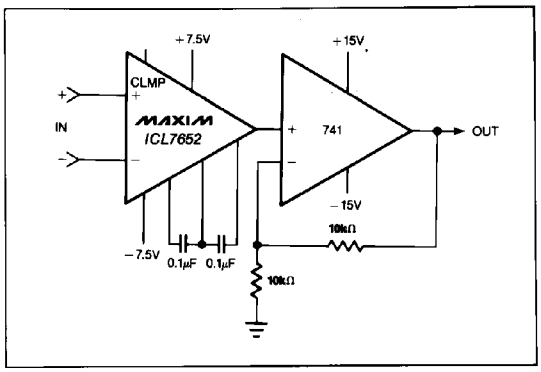


Figure 7. Using 741 to boost Output Drive Capability

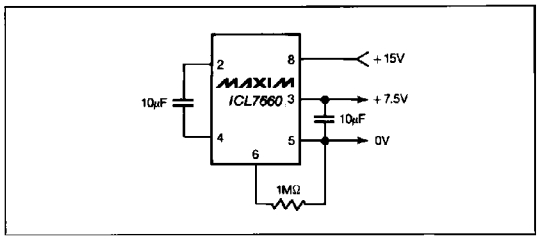
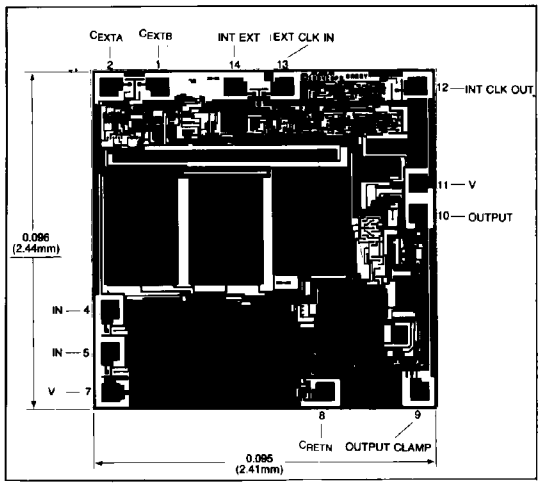
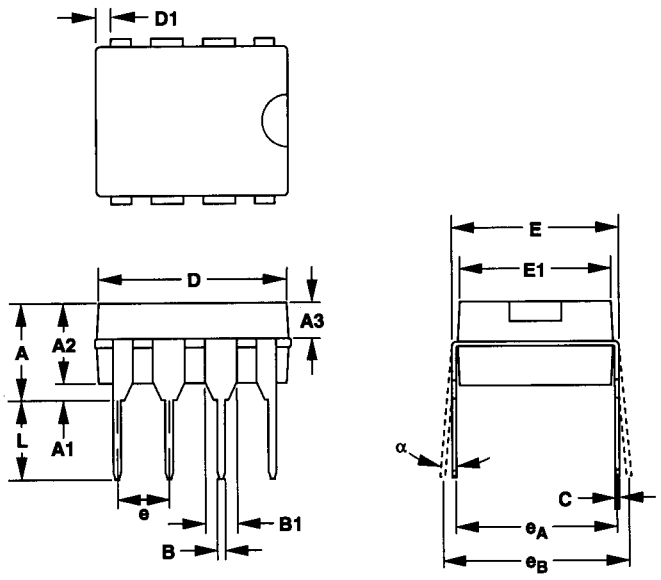


Figure 8. Splitting +15V with ICL7660. Same for -15V (95% Efficiency).

Chip Topography



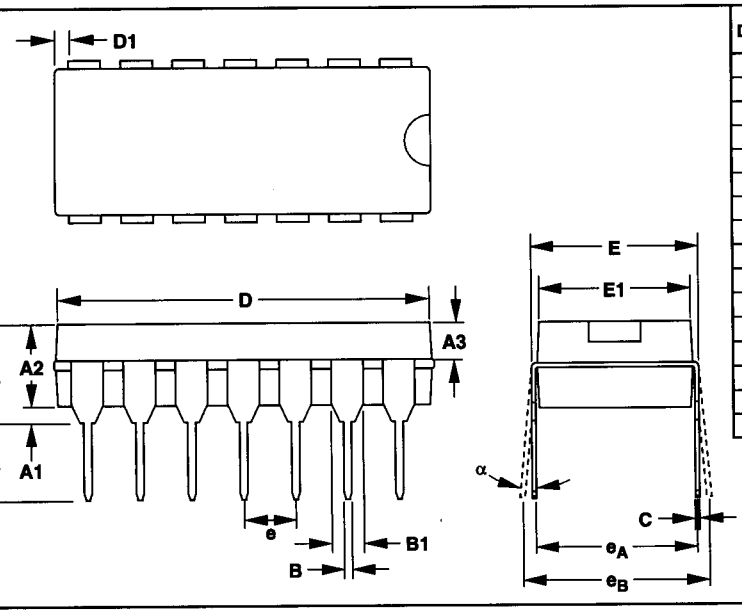
Chopper Stabilized Operational Amplifier



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.348	0.390	8.84	9.91
D1	0.005	0.035	0.13	0.89
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-324A

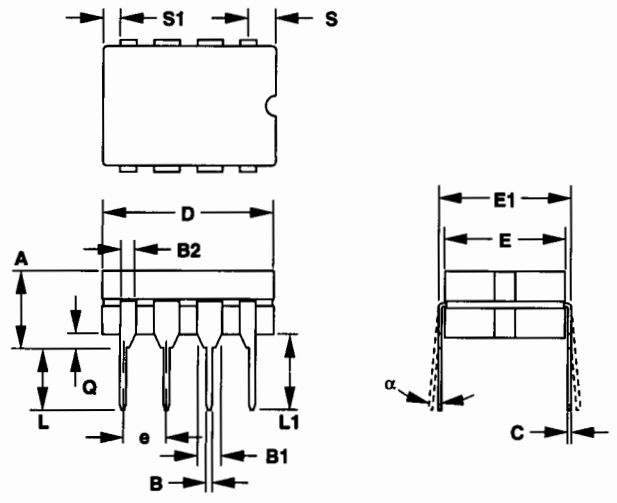
8-PIN PLASTIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.735	0.765	18.67	19.43
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-330A

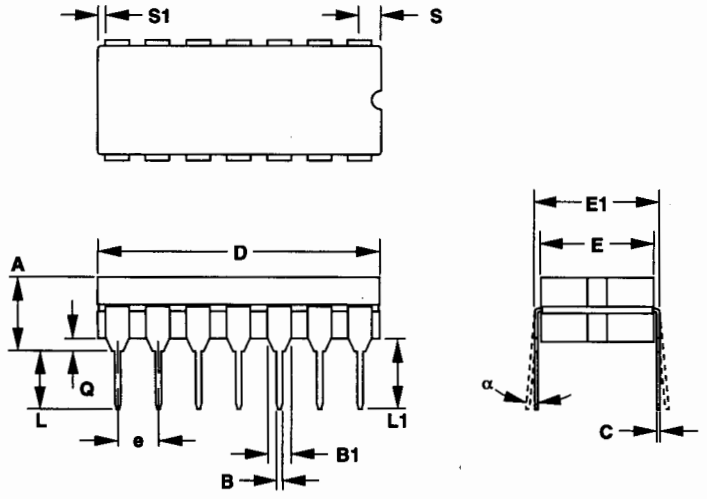
14-PIN PLASTIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
B2	0.023	0.045	0.58	1.14
C	0.008	0.015	0.20	0.38
D	–	0.405	–	10.29
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.055	–	1.40
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-326D

8-PIN CERAMIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	0.785	–	19.94
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-332C

14-PIN CERAMIC DUAL-IN-LINE PACKAGE