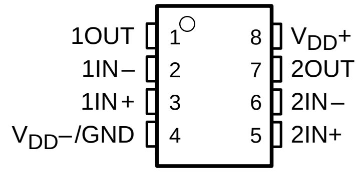
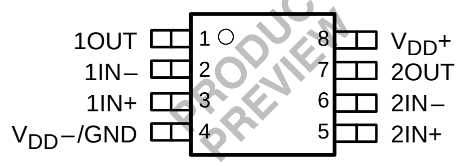
- **High Slew Rate . . . 10.5 V/μs Typ**
- **High-Gain Bandwidth . . . 5.1 MHz Typ**
- **Supply Voltage Range 2.7 V to 5 V**
- **Rail-to-Rail Output**
- **360 μV Input Offset Voltage**
- **Low Distortion Driving 600-Ω 0.005% THD+N**
- **1 mA Supply Current (Per Channel)**
- **17 nV/√Hz Input Noise Voltage**
- **2 pA Input Bias Current**
- **Characterized from T_A = –40°C to 125°C**
- **Available in MSOP (DGK) Package**

**D OR P PACKAGE
(TOP VIEW)**



**DGK PACKAGE
(TOP VIEW)**



description

The TLV2772 dual CMOS operational amplifier combines high slew rate and bandwidth, rail-to-rail output swing, high output drive and excellent dc precision. The device provides 10.5 V/μs of slew rate and 5.1 MHz of bandwidth while only consuming 1 mA of supply current per channel. This ac performance is much higher than current competitive CMOS amplifiers. The rail-to-rail output swing and high output drive makes this device a good choice for driving the analog input or reference of analog-to-digital converters. The device also has low distortion while driving a 600-Ω load for use in telecom systems.

The amplifier has a 360 μV input offset voltage, a 17 nV√Hz input noise voltage, and a 2 pA input bias current for measurement, medical, and industrial applications. The TLV2772 is also specified across an extended temperature range (–40°C to 125°C) making it useful for automotive systems.

The device operates from a 2.2 V to 5.5 V single supply voltage and is characterized at 2.7 V and 5 V. The single supply operation and low power consumption make this device a good solution for portable applications. It is available in an 8-pin PDIP, SOIC and ultra-low profile MSOP package.

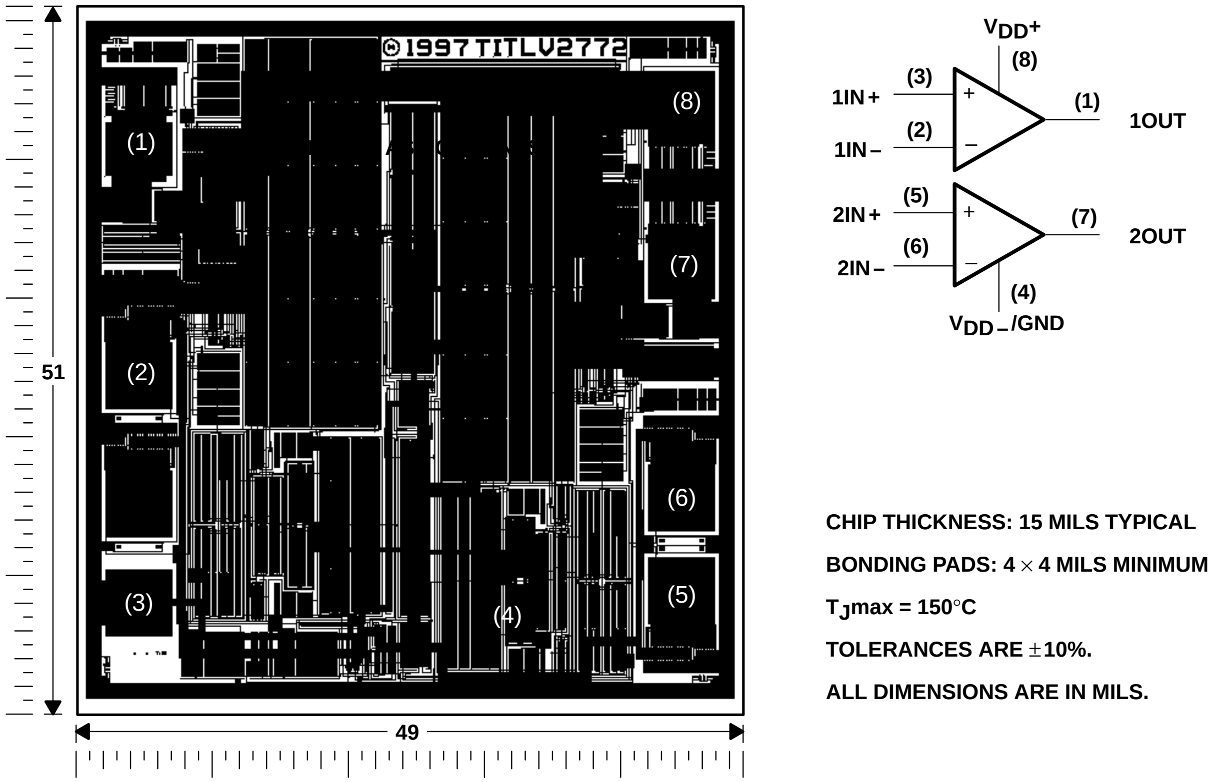
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	MSOP (DGK)	PLASTIC DIP (P)	
0°C to 70°C	2.5	TLV2772CD	TLV2772CDGK	TLV2772CP	TLV2772Y
–40°C to 125°C	2.5 1.6	TLV2772ID TLV2772AID	TLV2772IDGK TLV2772AIDGK	TLV2772IP TLV2772AIP	

† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLV2772CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2772Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2772. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . –0.3 V to V_{DD}
Input current, I_I (any input) . . . ±4 mA
Output current, I_O . . . ±50 mA
Total current into V_{DD+} . . . ±50 mA
Total current out of V_{DD-} . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . unlimited
Continuous total power dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . 0°C to 70°C
I suffix . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DGK	n/a	n/a	n/a	n/a	n/a
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.2	5.5	2.2	5.5	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.3	V_{DD-}	V_{DD+} –1.3	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.3	V_{DD-}	V_{DD+} –1.3	V
Operating free-air temperature, T_A	0	70	–40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2772C MIN	TLV2772C TYP	TLV2772C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		0.44	2.5	mV
			Full range		0.47	2.7	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2		µV/°C
I_{IO}	Input offset current		25°C		1		pA
			–40°C to 85°C		2	100	
I_{IB}	Input bias current		25°C		2		pA
			–40°C to 85°C		6	100	
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB, R_S = 50 Ω	25°C	0 to 1.4	–0.3 to 1.7		V
			Full range	0 to 1.4	–0.3 to 1.7		
V_{OH}	High-level output voltage	I_{OH} = –0.675 mA	25°C		2.6		V
			Full range	2.5			
		I_{OH} = –2.2 mA	25°C		2.4		
			Full range	2.1			
V_{OL}	Low-level output voltage	V_{IC} = 1.35 V, I_{OL} = 0.675 mA	25°C		0.1		V
			Full range			0.2	
		V_{IC} = 1.35 V, I_{OL} = 2.2 mA	25°C		0.21		
			Full range			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.35 V, R_L = 10 kΩ, V_O = 0.6 V to 2.1 V	25°C	20	380		V/mV
			Full range	13			
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.5 V, V_O = 1.5 V, R_S = 50 Ω	25°C	70	84		dB
			Full range	70	82		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	70	89		dB
			Full range	70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load	25°C		1	2	mA
			Full range			2	

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772C MIN	TLV2772C TYP	TLV2772C MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 100 pF,	25°C	5	9		V/μs
				Full range	4.7	6		
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		147		nV/√Hz
		f = 1 kHz		25°C		21		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33		μV
		f = 0.1 Hz to 10 Hz				0.86		
I_n	Equivalent input noise current	f = 100 Hz		25°C		1.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%		
			A_V = 10			0.025%		
			A_V = 100			0.12%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		4.8		MHz
t_s	Settling time	A_V = –1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186		μs
			0.01%	25°C		3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω,	C_L = 100 pF	25°C		46°		
	Gain margin			25°C		12		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2772I			TLV2772AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		0.44	2.5		0.44	1.6	mV
			Full range		0.47	2.7		0.47	1.9	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current		25°C		1			1		pA
			−40°C to 85°C		2	100		2	100	
I_{IB}	Input bias current		25°C		2			2		pA
			−40°C to 85°C		6	100		6	100	
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB, R_S = 50 Ω	25°C	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		V
			Full range	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		
V_{OH}	High-level output voltage	I_{OH} = −0.675 mA	25°C		2.6			2.6		V
			Full range	2.5			2.5			
		I_{OH} = −2.2 mA	25°C		2.4			2.4		
			Full range	2.1			2.1			
V_{OL}	Low-level output voltage	V_{IC} = 1.35 V, I_{OL} = 0.675 mA	25°C		0.1			0.1		V
			Full range			0.2			0.2	
		V_{IC} = 1.35 V, I_{OL} = 2.2 mA	25°C		0.21			0.21		
			Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.35 V, V_O = 0.6 V to 2.1 V, R_L = 10 kΩ	25°C	20	380		20	380		V/mV
			Full range	13			13			
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		25			25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.5 V, V_O = 1.5 V, R_S = 50 Ω	25°C	70	84		70	84		dB
			Full range	70	82		70	82		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	70	89		70	89		dB
			Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load	25°C		1	2		1	2	mA
			Full range			2			2	

† Full range is – 40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772I			TLV2772AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	9		5	9		V/µs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		147			147		nV/√Hz
		f = 1 kHz		25°C		21			21		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		1.5			1.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%			0.0085%		
			A_V = 10			0.025%			0.025%		
			A_V = 100			0.12%			0.12%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		4.8			4.8		MHz
t_s	Settling time	A_V = –1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186			0.186		µs
			0.01%	25°C		3.92			3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is –40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		0.36	2.5	mV
				Full range		0.4	2.7	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2		µV/°C
I_{IO}	Input offset current			25°C		1		pA
				–40°C to 85°C		2	100	
I_{IB}	Input bias current			25°C		2		pA
				–40°C to 85°C		6	100	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω	25°C	0 to 3.7	–0.3 to 3.8		V
				Full range	0 to 3.7	–0.3 to 3.8		
V_{OH}	High-level output voltage	I_{OH} = –1.3 mA		25°C		4.9		V
				Full range	4.8			
		I_{OH} = –4.2 mA		25°C		4.7		
				Full range	4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 1.3 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 4.2 mA	25°C		0.21		
				Full range			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,	25°C	20	450		V/mV
				Full range	13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3.7 V, R_S = 50 Ω	V_O = 3.7 V,	25°C	60	96		dB
				Full range	60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		dB
				Full range	70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		1	2	mA
				Full range			2	

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		V/µs
				Full range	4.7	6		
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		147		nV/√Hz
		f = 1 kHz		25°C		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33		µV
		f = 0.1 Hz to 10 Hz				0.86		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.2		pA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%		
			A_V = 10			0.016%		
			A_V = 100			0.095%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		5.1		MHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134		µs
			0.01%	25°C		1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°		
	Gain margin			25°C		12		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772I			TLV2772AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		0.36	2.5		0.36	1.6	mV
				Full range		0.4	2.7		0.4	1.9	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1			1		pA
				−40°C to 85°C		2	100		2	100	
I_{IB}	Input bias current			25°C		2			2		pA
				−40°C to 85°C		6	100		6	100	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω	25°C	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		V
				Full range	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		
V_{OH}	High-level output voltage	I_{OH} = −1.3 mA		25°C		4.9			4.9		V
				Full range	4.8			4.8			
		I_{OH} = −4.2 mA		25°C		4.7			4.7		
				Full range	4.4			4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 1.3 mA	25°C		0.1			0.1		V
				Full range			0.2			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 4.2 mA	25°C		0.21			0.21		
				Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ	25°C	20	450		20	450		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		20			20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3.7 V, R_S = 50 Ω	V_O = 3.7 V,	25°C	60	96		60	96		dB
				Full range	60	93		60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		1	2		1	2	mA
				Full range			2			2	

† Full range is – 40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772I MIN	TLV2772I TYP	TLV2772I MAX	TLV2772AI MIN	TLV2772AI TYP	TLV2772AI MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		5	10.5		V/µs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		147			147		nV/√Hz
		f = 1 kHz		25°C		17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.2			0.2		pA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%			0.005%		
			A_V = 10			0.016%			0.016%		
			A_V = 100			0.095%			0.095%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		5.1			5.1		MHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134			0.134		µs
			0.01%	25°C		1.97			1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is –40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2772Y MIN	TLV2772Y TYP	TLV2772Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		0.44		mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				2		pA
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB,	R_S = 50 Ω		−0.3 to 1.7		V
V_{OH}	High-level output voltage	I_{OH} = −0.675 mA			2.6		V
		I_{OH} = −2.2 mA			2.4		
V_{OL}	Low-level output voltage	V_{IC} = 1.35 V,	I_{OL} = 0.675 mA		0.1		V
		V_{IC} = 1.35 V,	I_{OL} = 2.2 mA		0.21		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.35 V, V_O = 0.6 V to 2.1 V	R_L = 10 kΩ,		380		V/mV
$r_{i(d)}$	Differential input resistance				10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10		25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.5 V, R_S = 50 Ω	V_O = 1.5 V,		84		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,		89		dB
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load		1		mA

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2772Y MIN	TLV2772Y TYP	TLV2772Y MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 100 pF,		9		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			147		nV/√Hz
		f = 1 kHz			21		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.33		µV
		f = 0.1 Hz to 10 Hz			0.86		
I_n	Equivalent input noise current	f = 100 Hz			1.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1		0.0085%		
			A_V = 10		0.025%		
			A_V = 100		0.12%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,		4.8		MHz
t_s	Settling time	A_V = −1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%		0.186		µs
			0.01%		3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω,	C_L = 100 pF		46°		
	Gain margin				12		dB

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2772Y MIN	TLV2772Y TYP	TLV2772Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		0.36		mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				2		pA
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω		–0.3 to 3.8		V
V_{OH}	High-level output voltage	I_{OH} = –1.3 mA			4.9		V
		I_{OH} = –4.2 mA			4.7		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 1.3 mA		0.1		V
		V_{IC} = 2.5 V,	I_{OL} = 4.2 mA		0.21		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,		450		V/mV
$r_{i(d)}$	Differential input resistance				10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10		20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3.7 V, R_S = 50 Ω	V_O = 3.7 V,		96		dB
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,		89		dB
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load		1		mA

operating characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2772Y MIN	TLV2772Y TYP	TLV2772Y MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, R_L = 10 kΩ	C_L = 100 pF,		10.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			147		nV/√Hz
		f = 1 kHz			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.33		µV
		f = 0.1 Hz to 10 Hz			0.86		
I_n	Equivalent input noise current	f = 100 Hz			0.2		pA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1		0.005%		
			A_V = 10		0.016%		
			A_V = 100		0.095%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,		5.1		MHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%		0.134		µs
			0.01%		1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω,	C_L = 100 pF		46°		
	Gain margin				12		dB

TYPICAL CHARACTERISTICS

Table of Graphs

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ϕ_m	Phase margin	vs Load capacitance	46
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TYPICAL CHARACTERISTICS

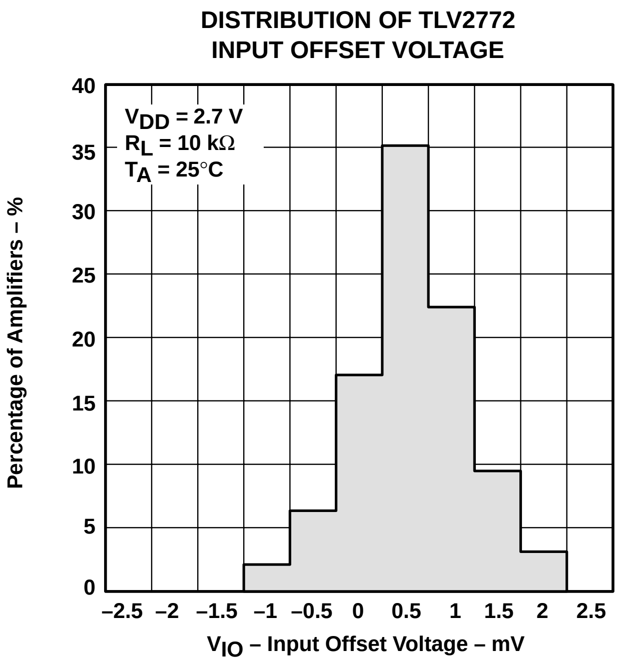

Figure 1

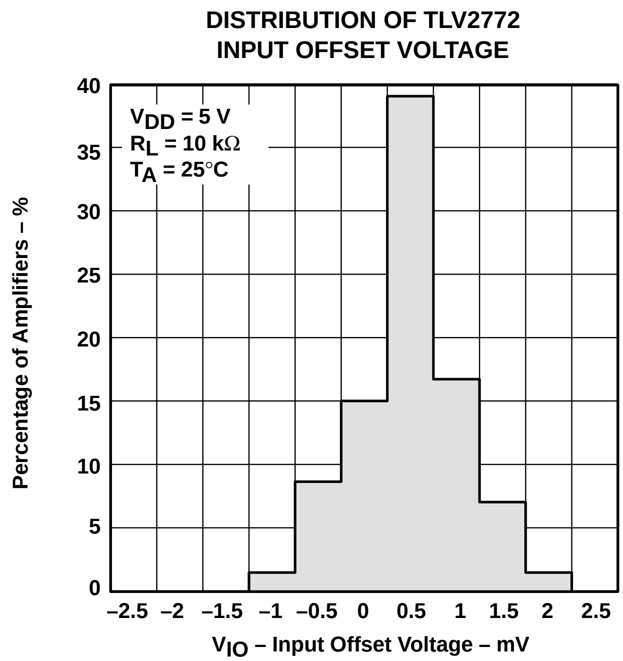

Figure 2

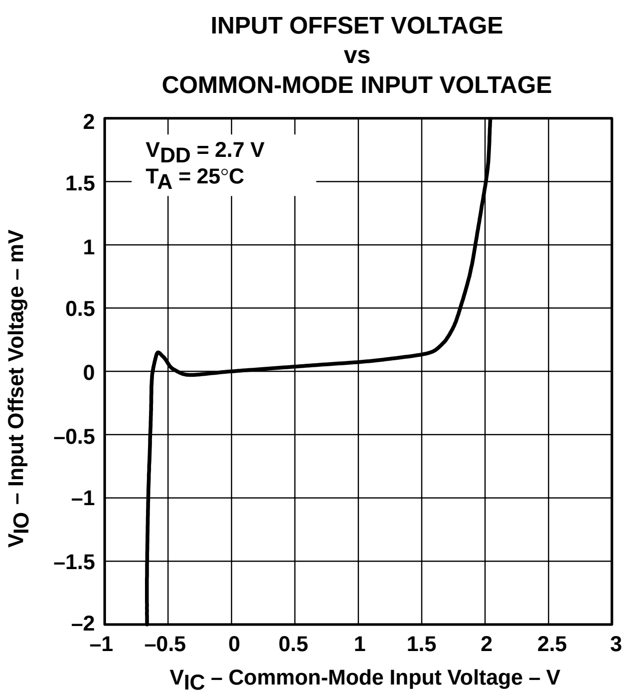

Figure 3

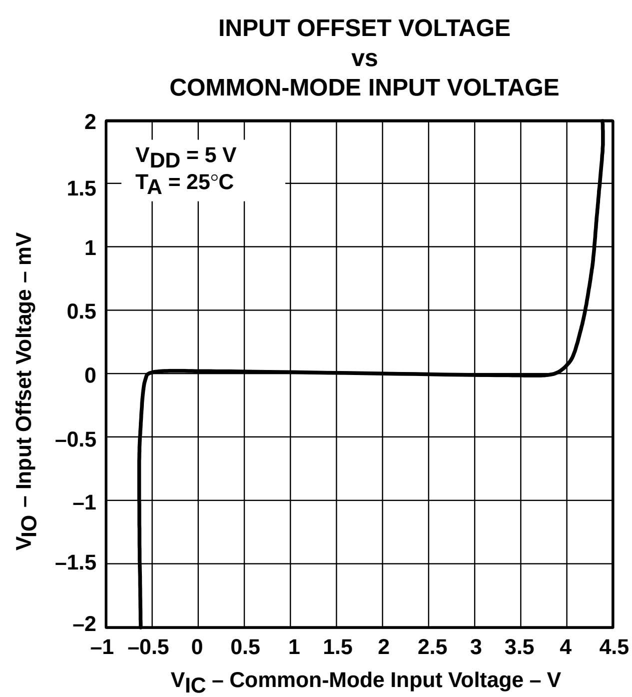

Figure 4

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE

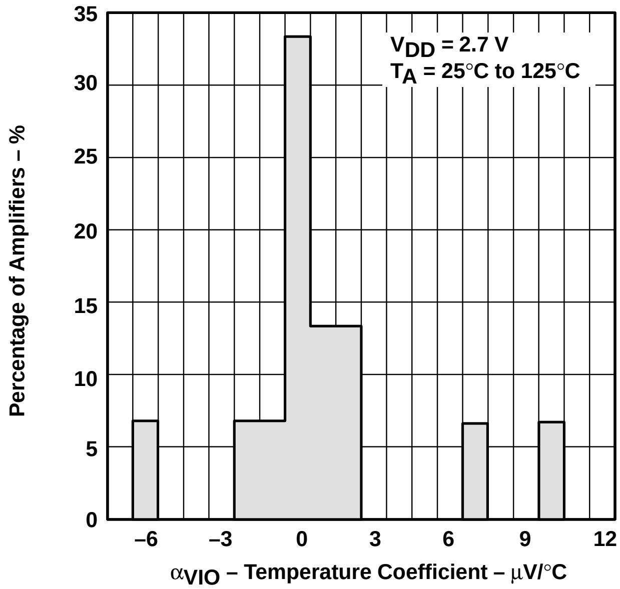

Figure 5

DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE

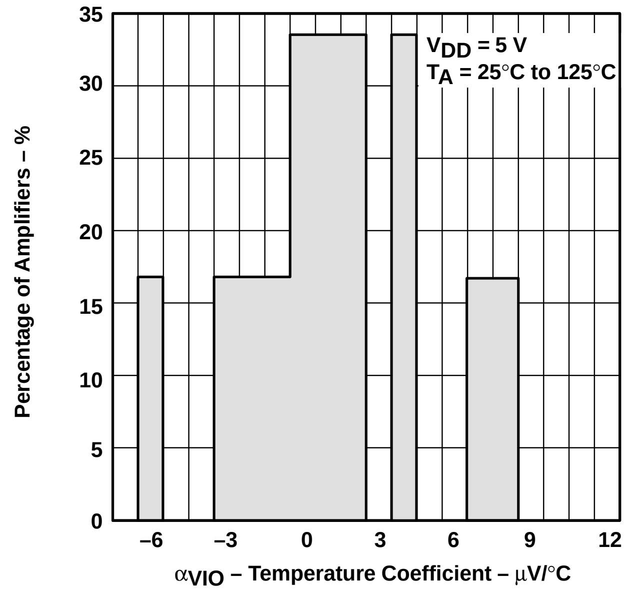

Figure 6

INPUT BIAS AND OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

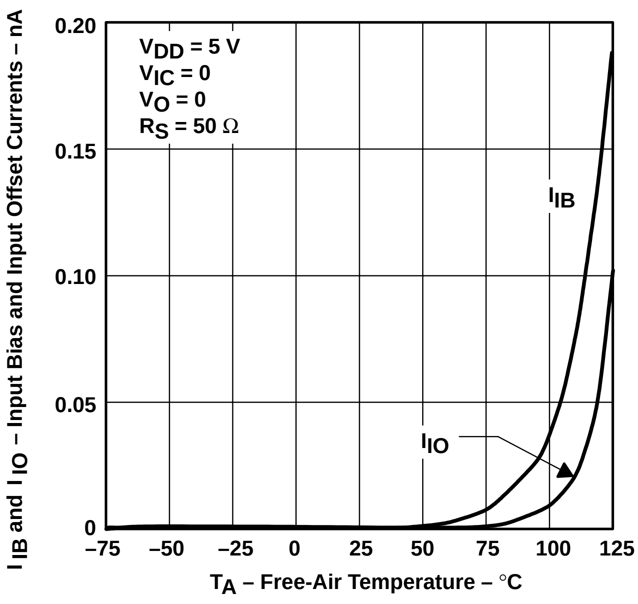

Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

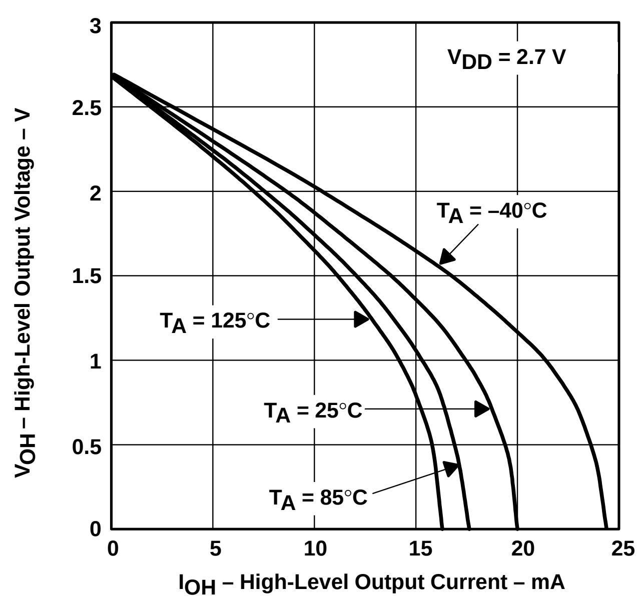

Figure 8

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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

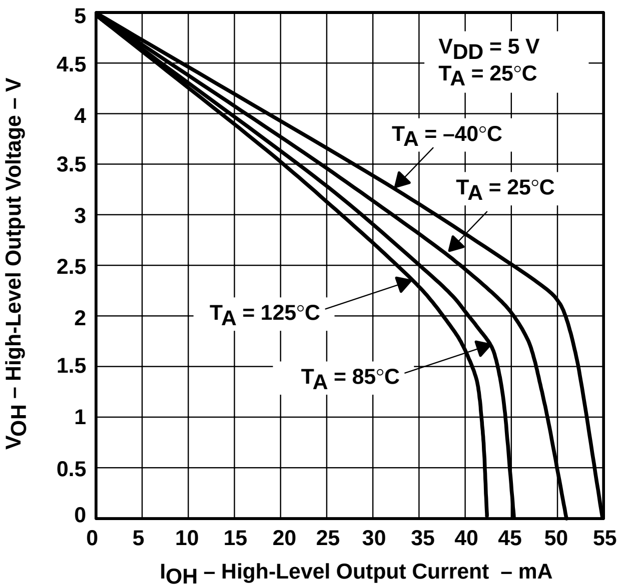


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

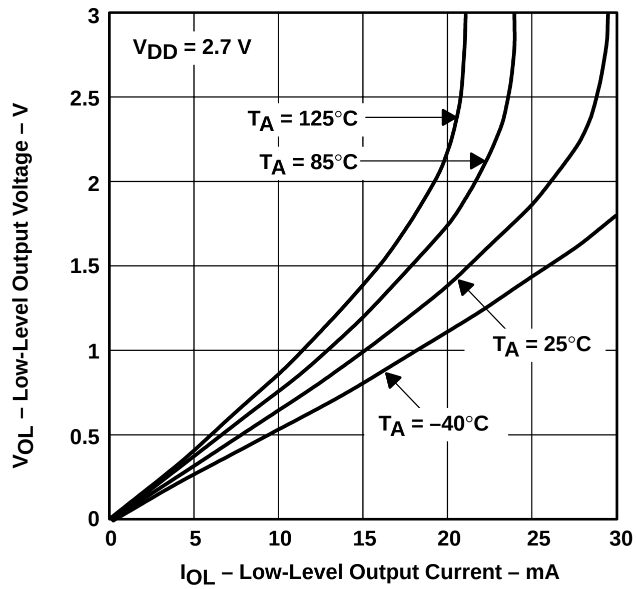


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

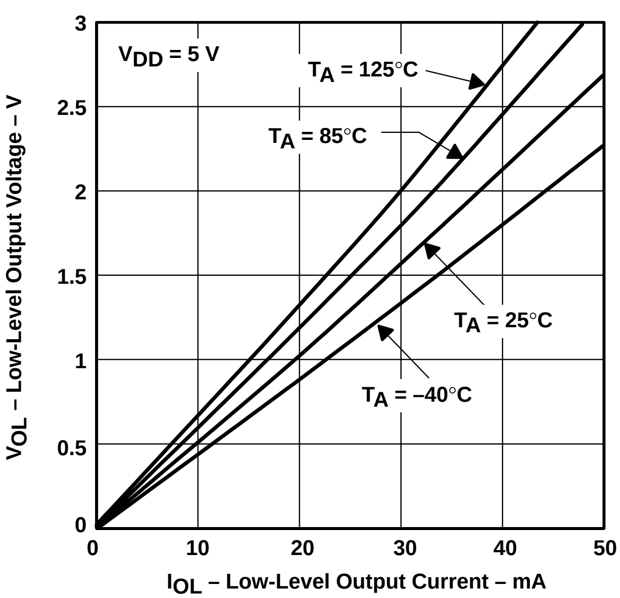


Figure 11

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

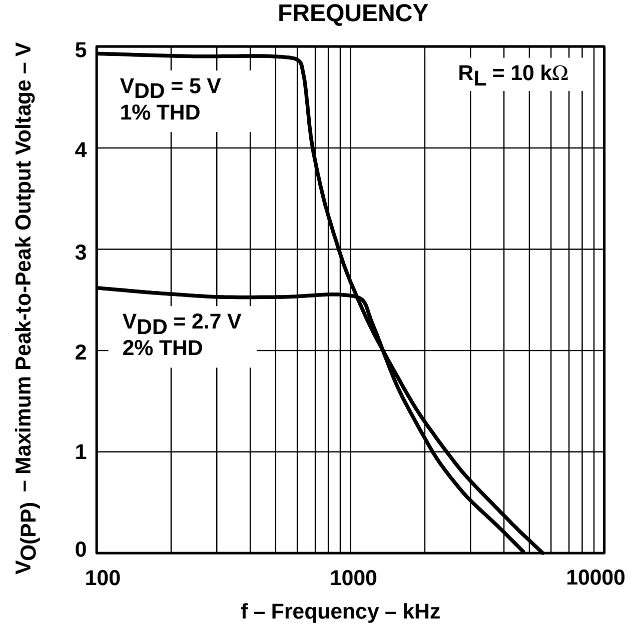


Figure 12

TYPICAL CHARACTERISTICS

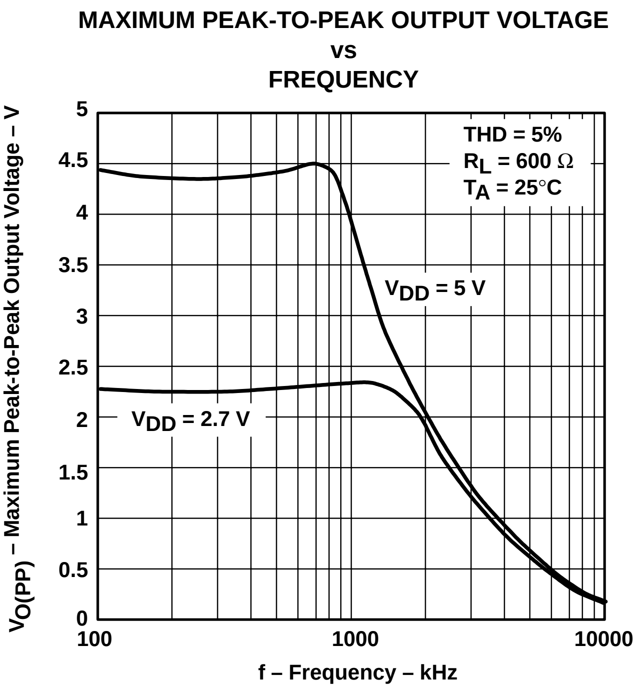


Figure 13

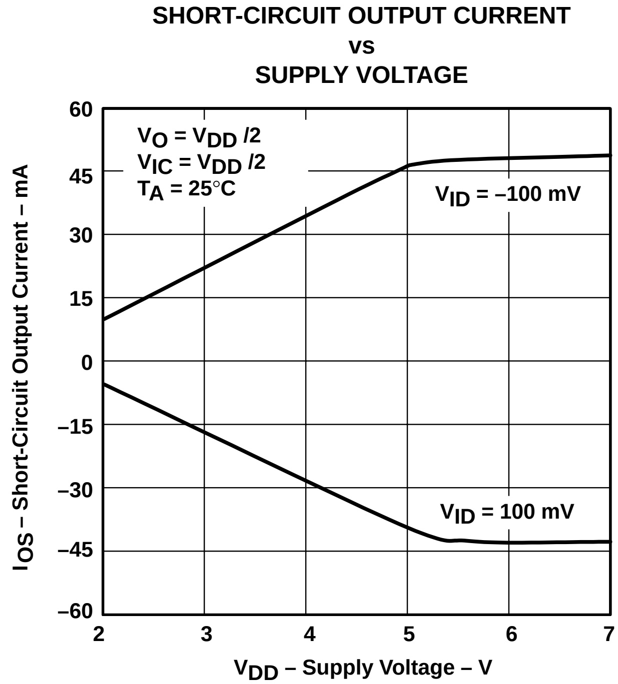


Figure 14

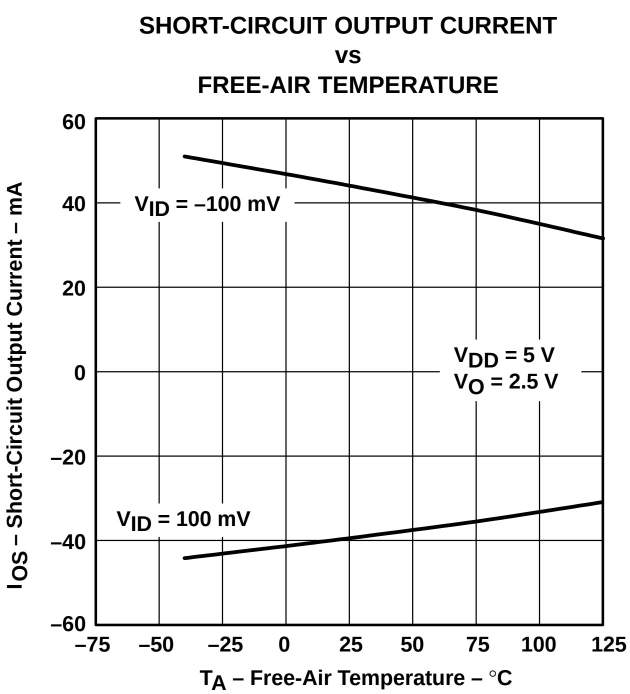


Figure 15

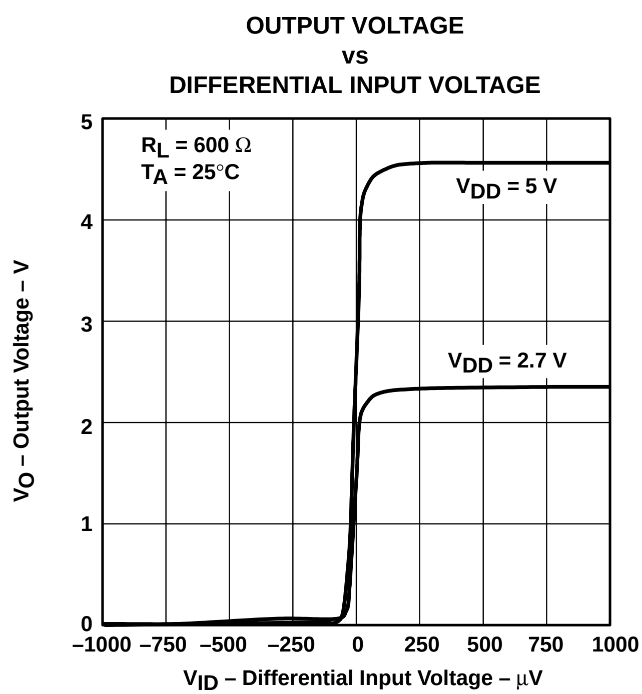


Figure 16

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

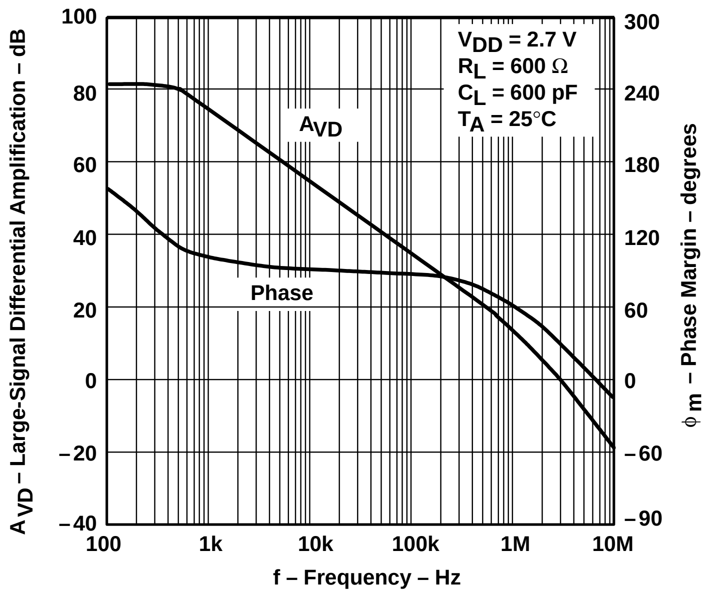


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

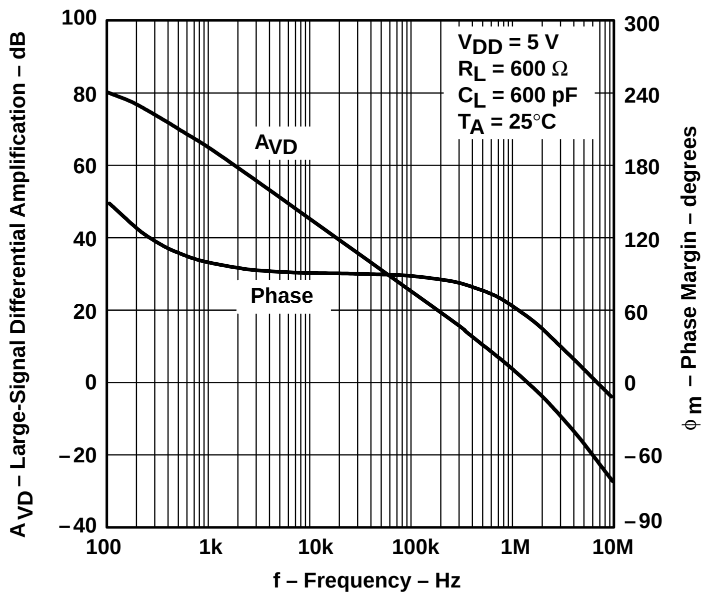


Figure 18

TYPICAL CHARACTERISTICS

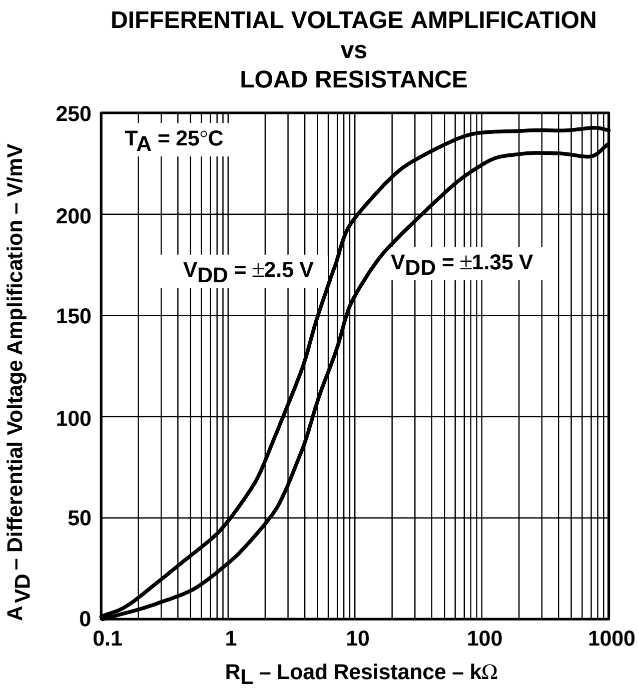


Figure 19

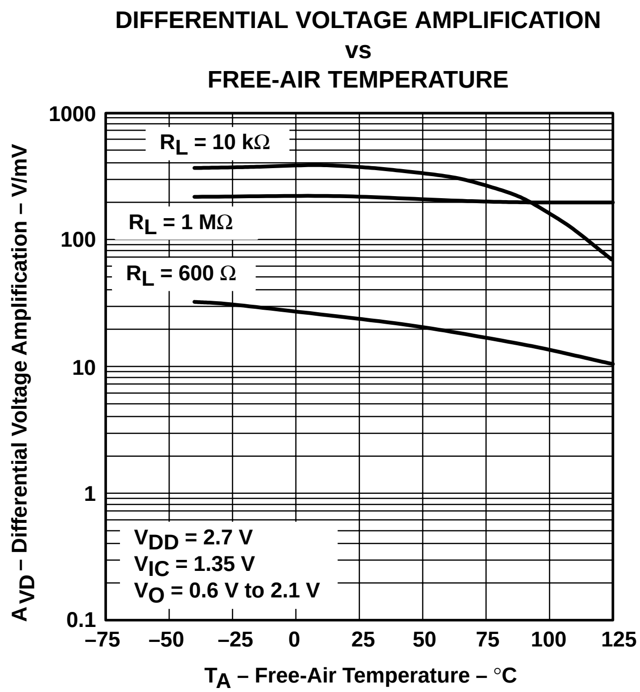


Figure 20

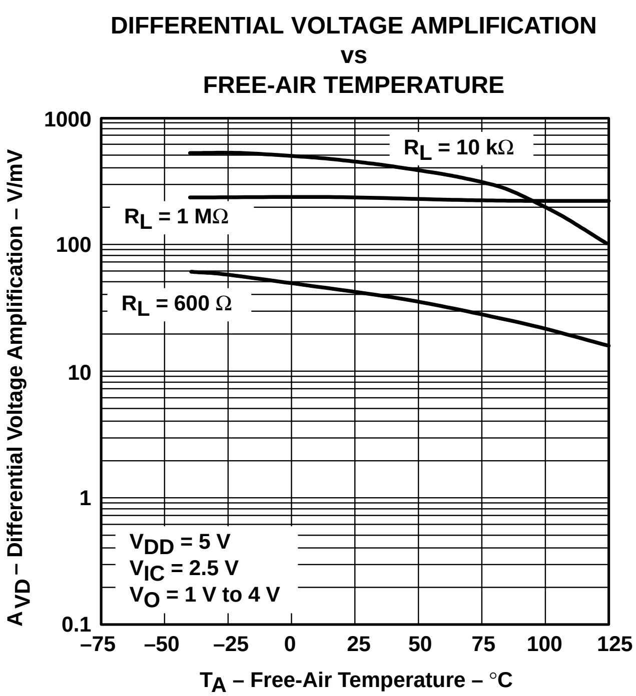


Figure 21

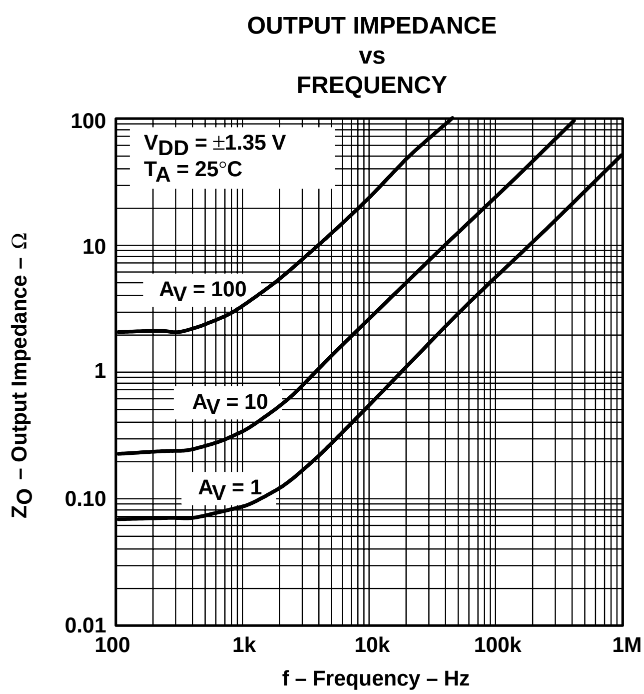


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

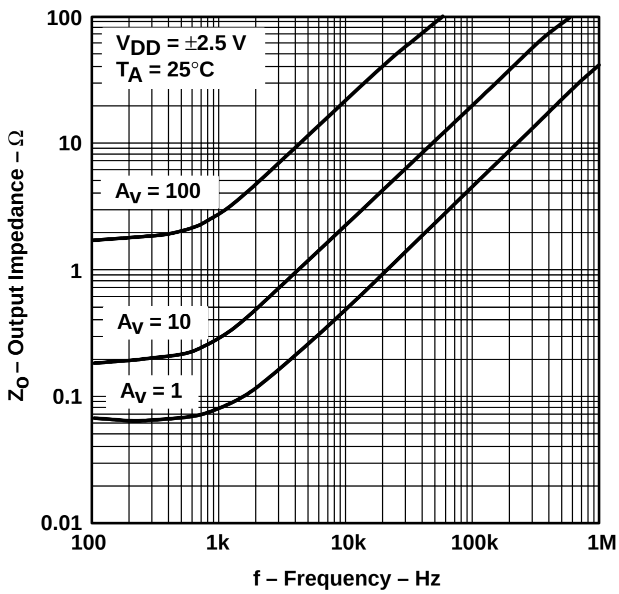


Figure 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

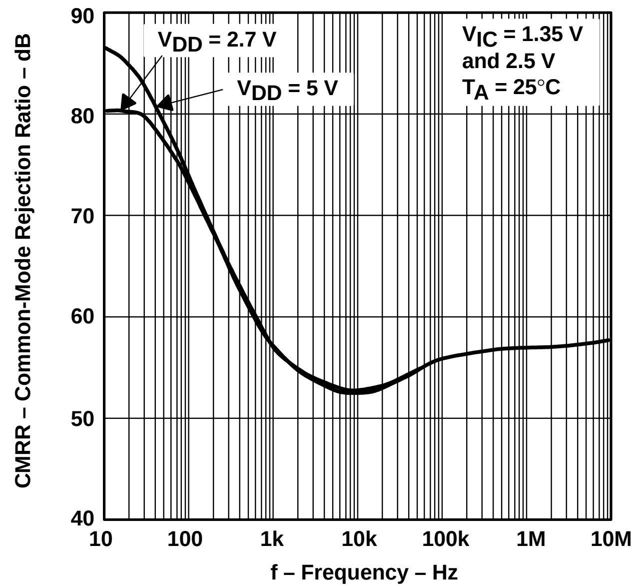


Figure 24

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

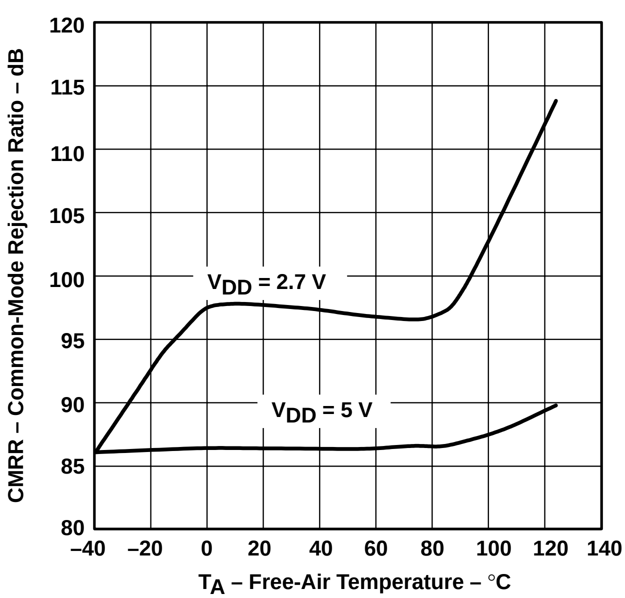


Figure 25

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

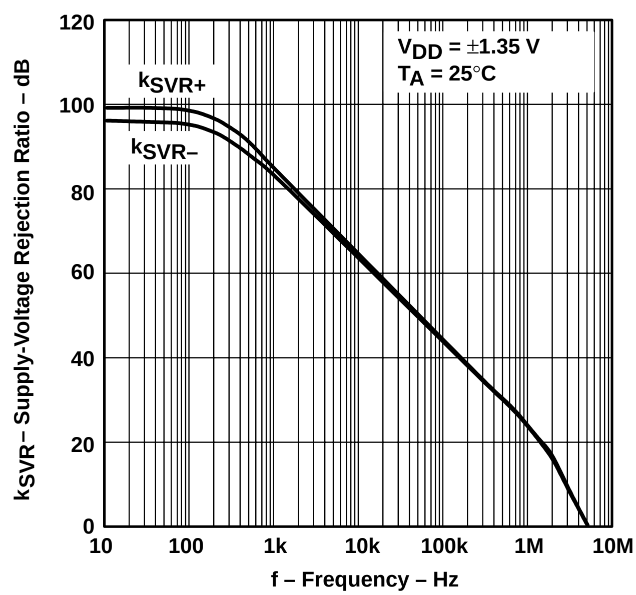


Figure 26

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

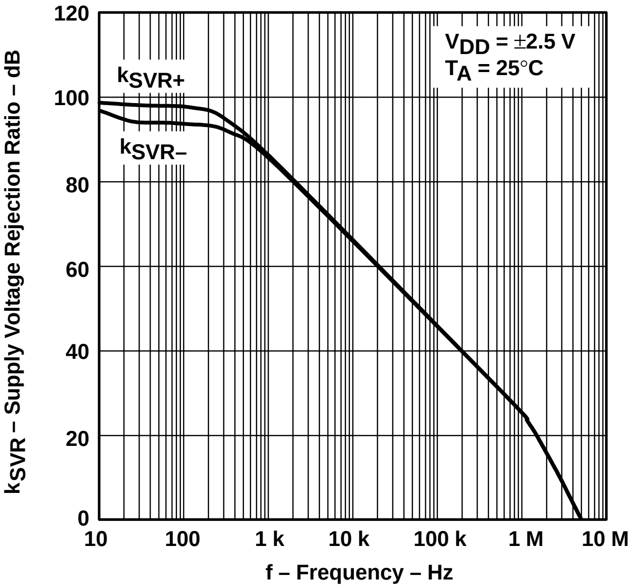


Figure 27

SUPPLY CURRENT (PER CHANNEL) vs SUPPLY VOLTAGE

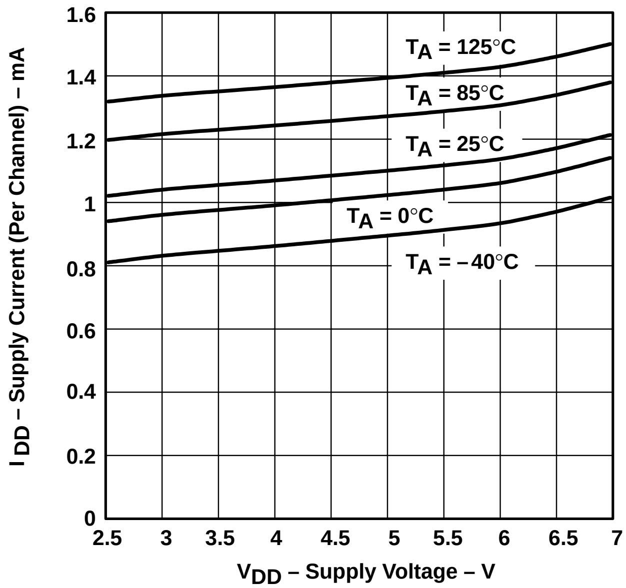


Figure 28

SLEW RATE vs LOAD CAPACITANCE

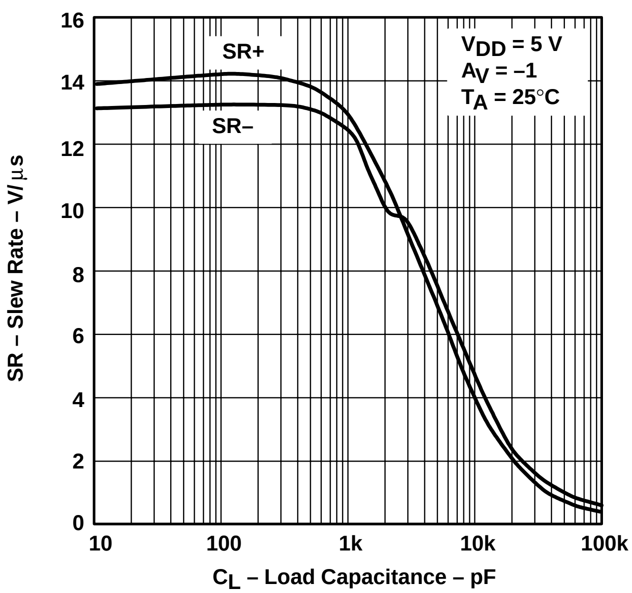


Figure 29

SLEW RATE vs FREE-AIR TEMPERATURE

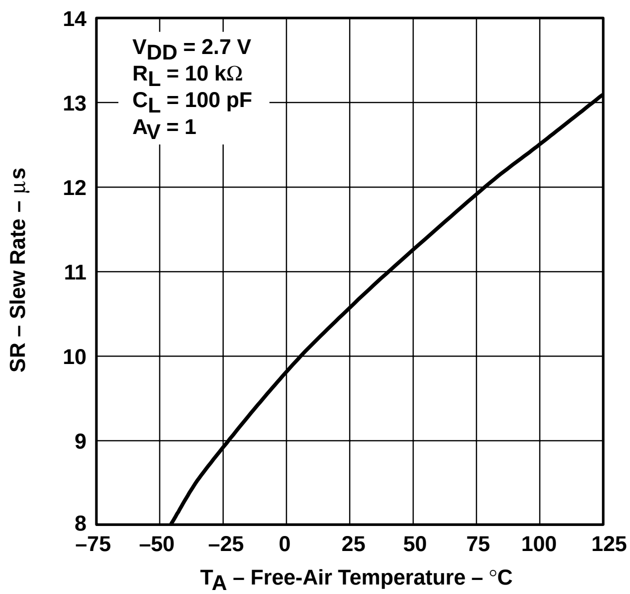


Figure 30

TYPICAL CHARACTERISTICS

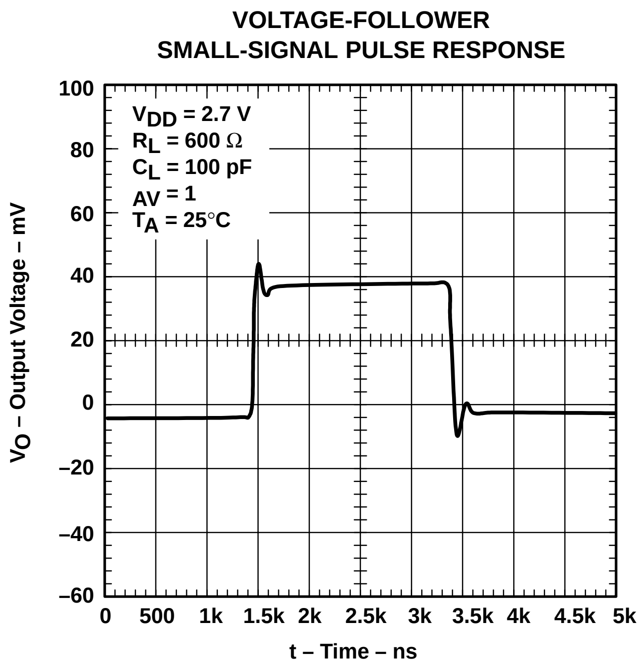


Figure 31

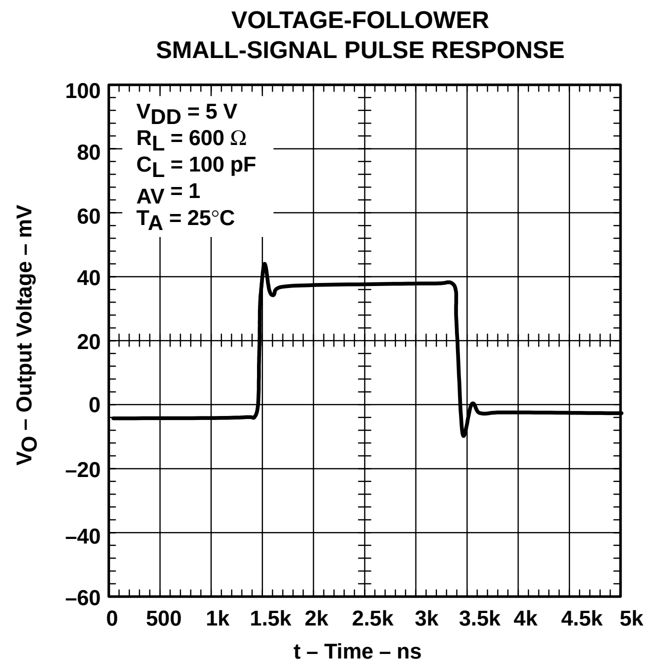


Figure 32

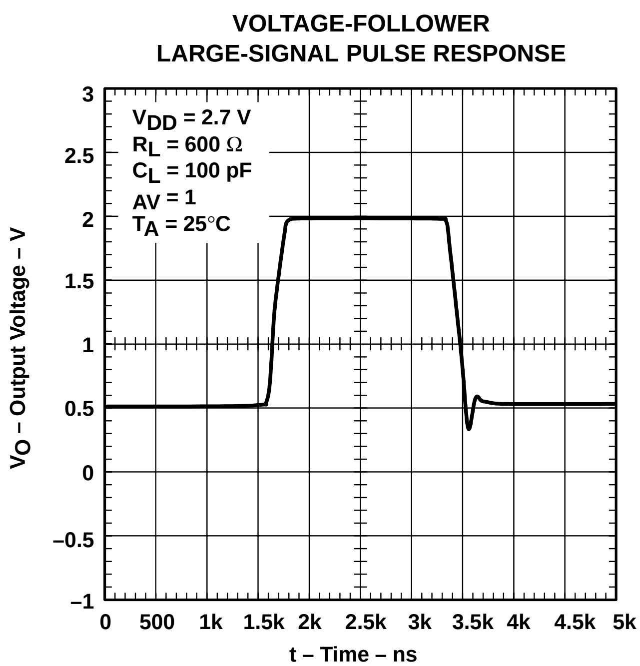


Figure 33

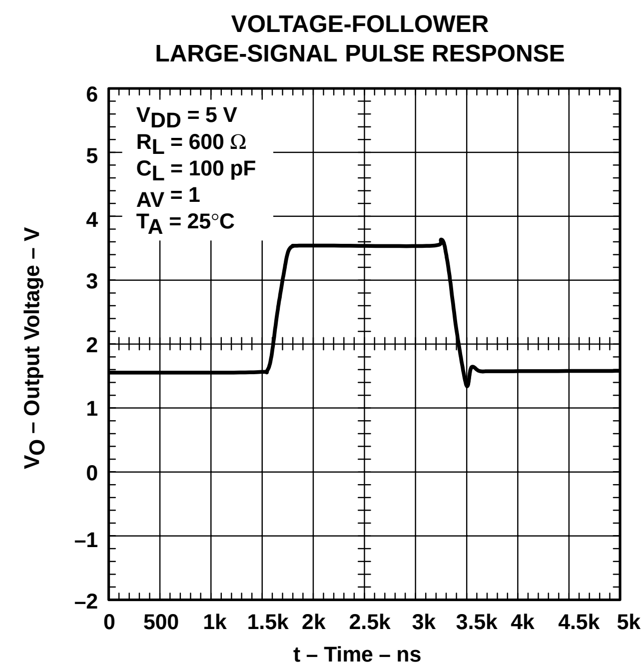


Figure 34

TYPICAL CHARACTERISTICS

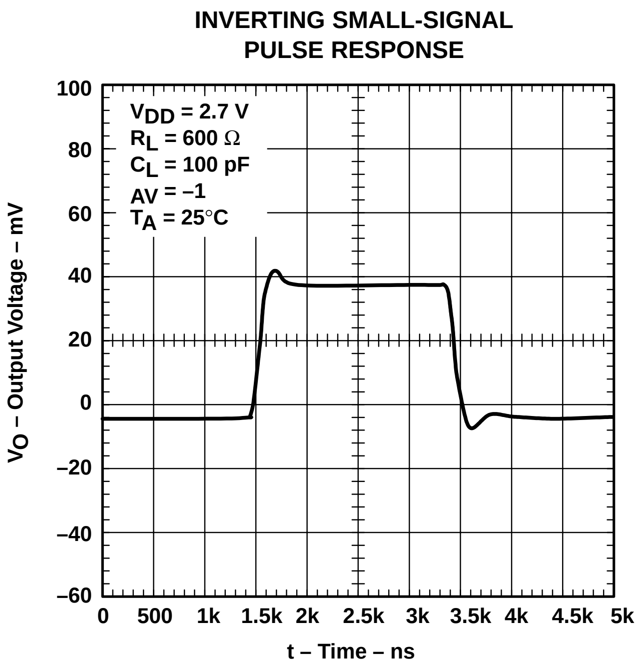


Figure 35

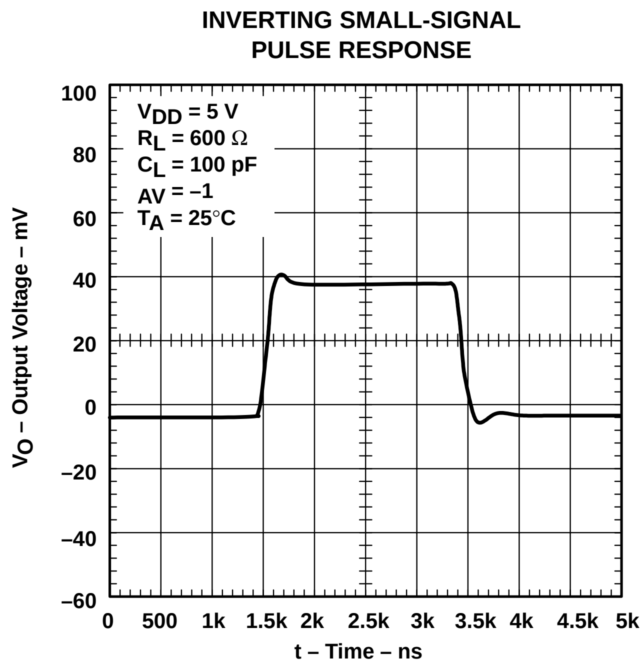


Figure 36

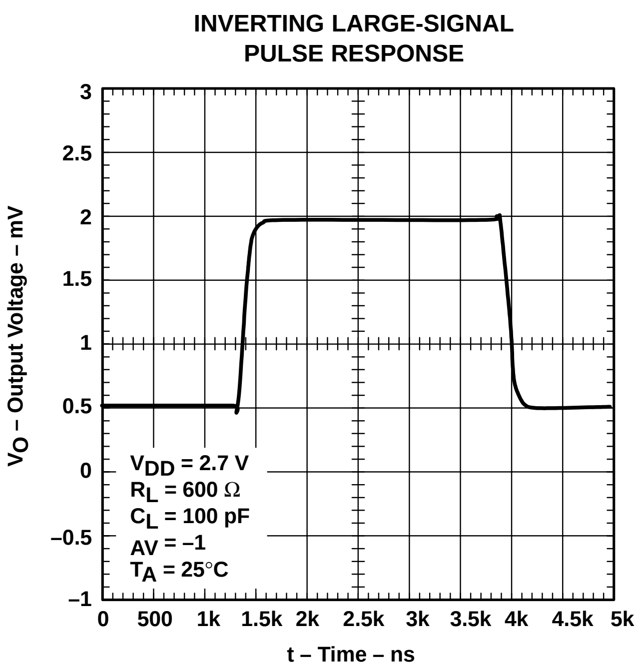


Figure 37

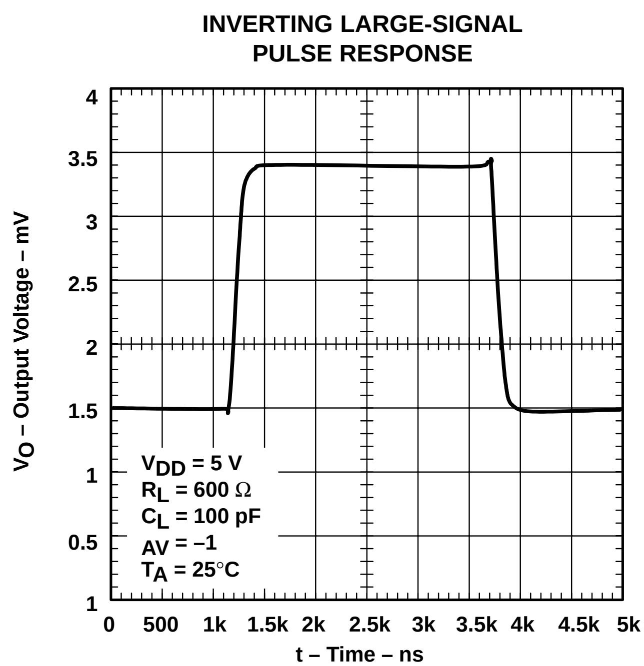


Figure 38

TYPICAL CHARACTERISTICS

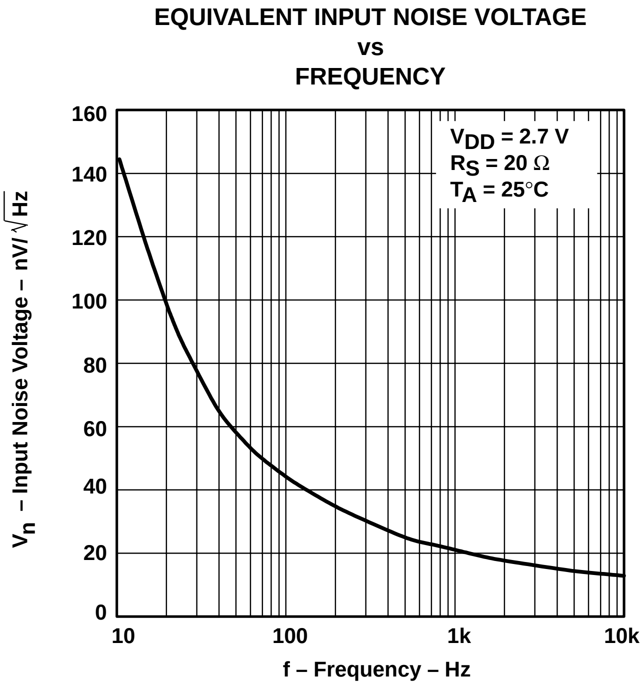


Figure 39

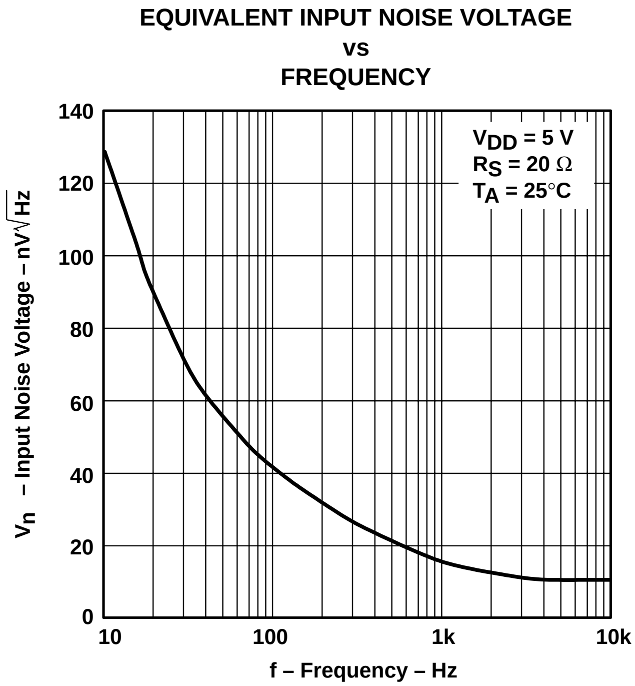


Figure 40

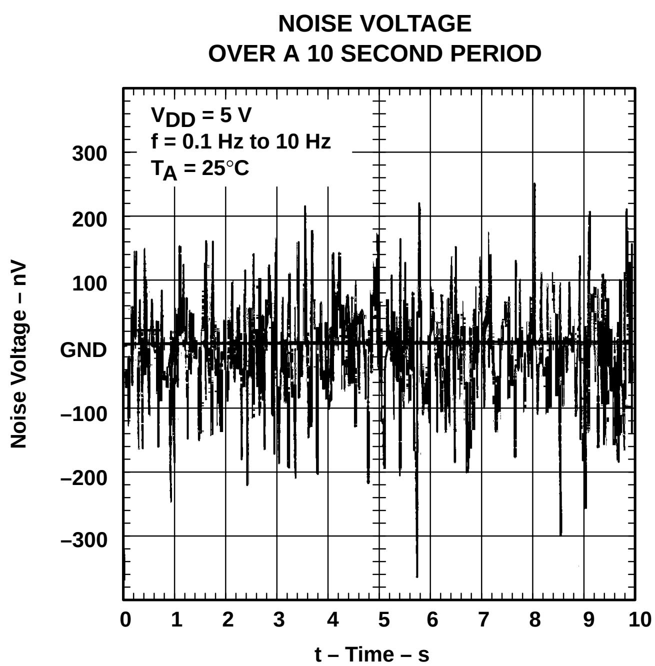


Figure 41

TYPICAL CHARACTERISTICS

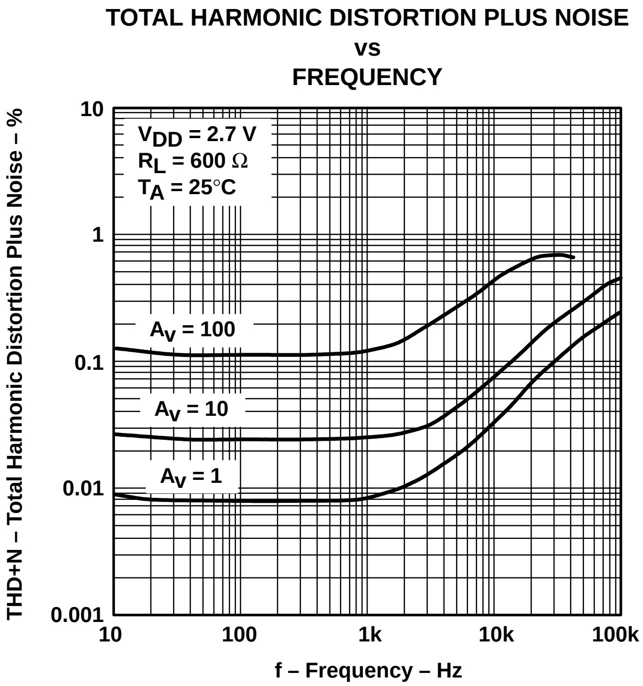


Figure 42

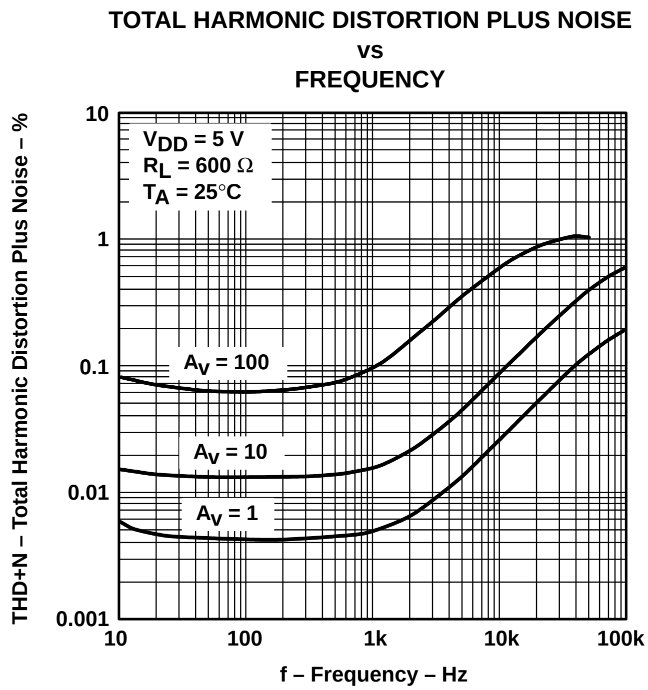


Figure 43

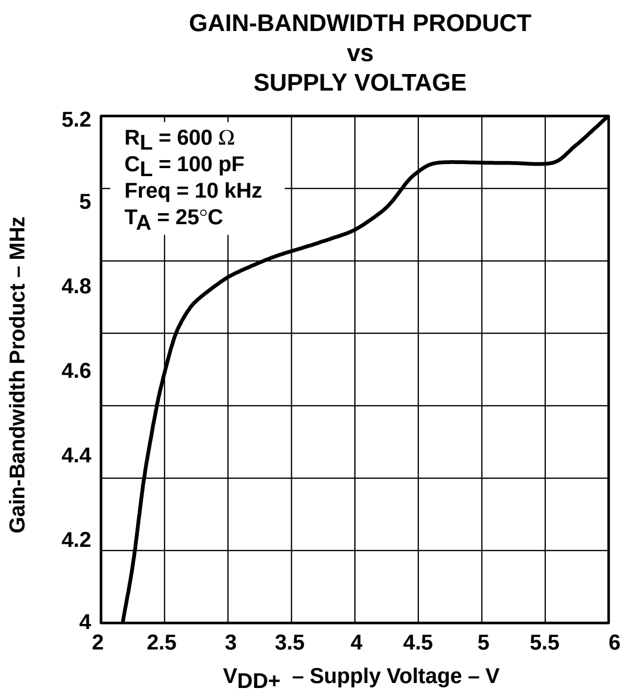


Figure 44

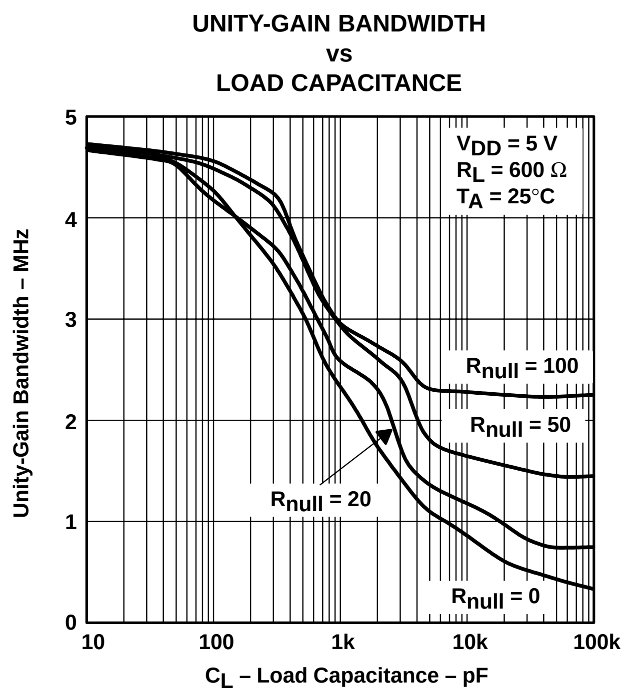


Figure 45

TYPICAL CHARACTERISTICS

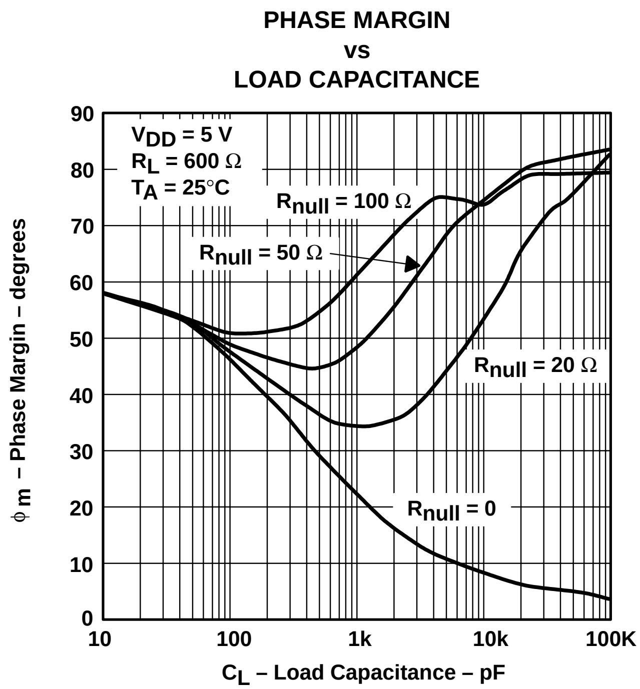


Figure 46

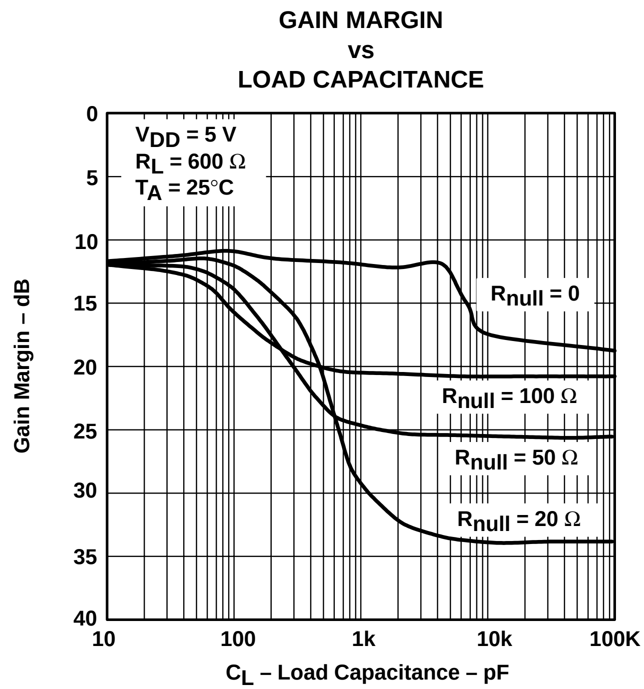


Figure 47

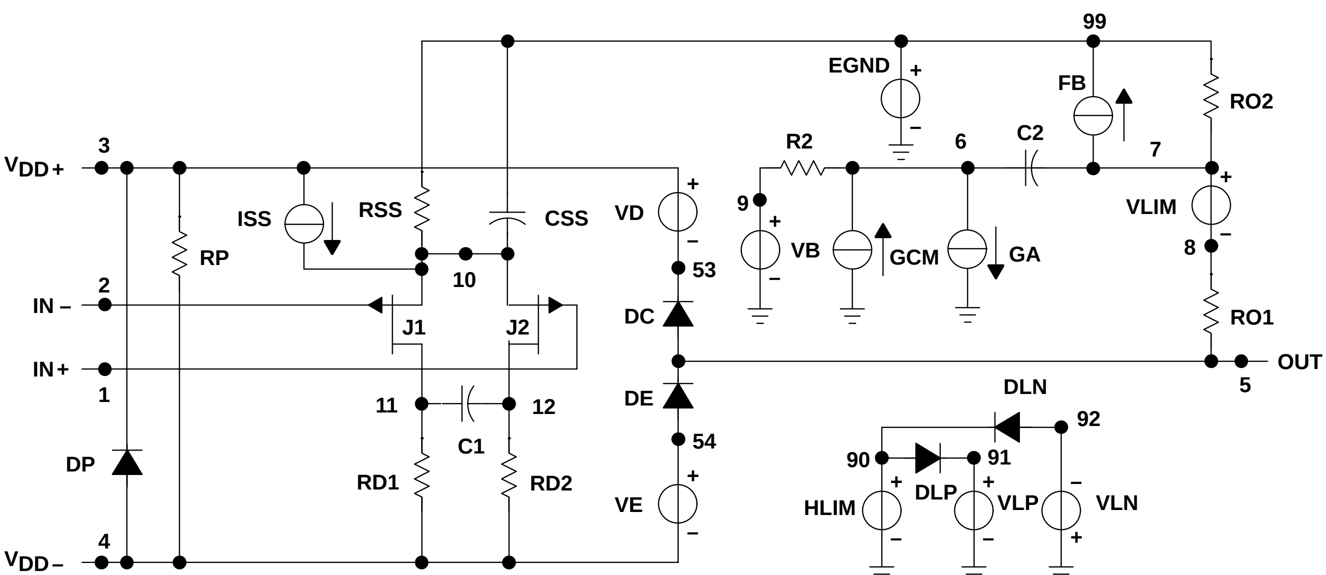
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 4) and subcircuit in Figure 48 are generated using the TLV2772 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Intergrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV2772–X 1 2 3 4 5
        C1      11      12      2.3094E–12
        C2      6       7       8.0000E–12
        CSS     10      99      2.1042E–12
        DC      5       53      DY
        DE      54      5       DY
        DLP     90      91      DX
        DLN     92      90      DX
        DP      4       3       DX
        EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7       99      POLY (5) VB VC VE VLP
        + VLN 0 19.391E6 –1E3 1E3 19E6 –19E6
        GA      6       0       11      12 150.80E–6
        GCM     0       6       10      99 7.5576E–9
        ISS     3       10      DC 116.40E–6
        HLIM    90      0       VLIM 1K
        J1      11      2       10 JX1
        J2      12      1       10 JX2
        R2      6       9       100.00E3
RD1     4       11      6.6315E3
RD2     4       12      6.6315E3
R01     8       5       17.140
R02     7       99      17.140
RP      3       4       4.5455E3
RSS     10      99      1.7182E6
VB      9       0       DC 0
VC      3       53      DC .1
VE      54      4       DC .1
VLIM    7       8       DC 0
VLP     91      0       DC 47
VLN     0       92      DC 47
.MODEL DX D (IS=800.0E–18)
.MODEL DY D (IS=800.0E–18 Rs = 1m Cjo=10p)
.MODEL JX1 PJF (IS=2.2500E–12 BETA=195.36E–6
+ VTO=–1)
.MODEL JX2 PJF (IS=1.7500E–12 BETA=195.36E–6
+ VTO=–1)
.ENDS
```

Figure 48. Boyle Macromodel and Subcircuit

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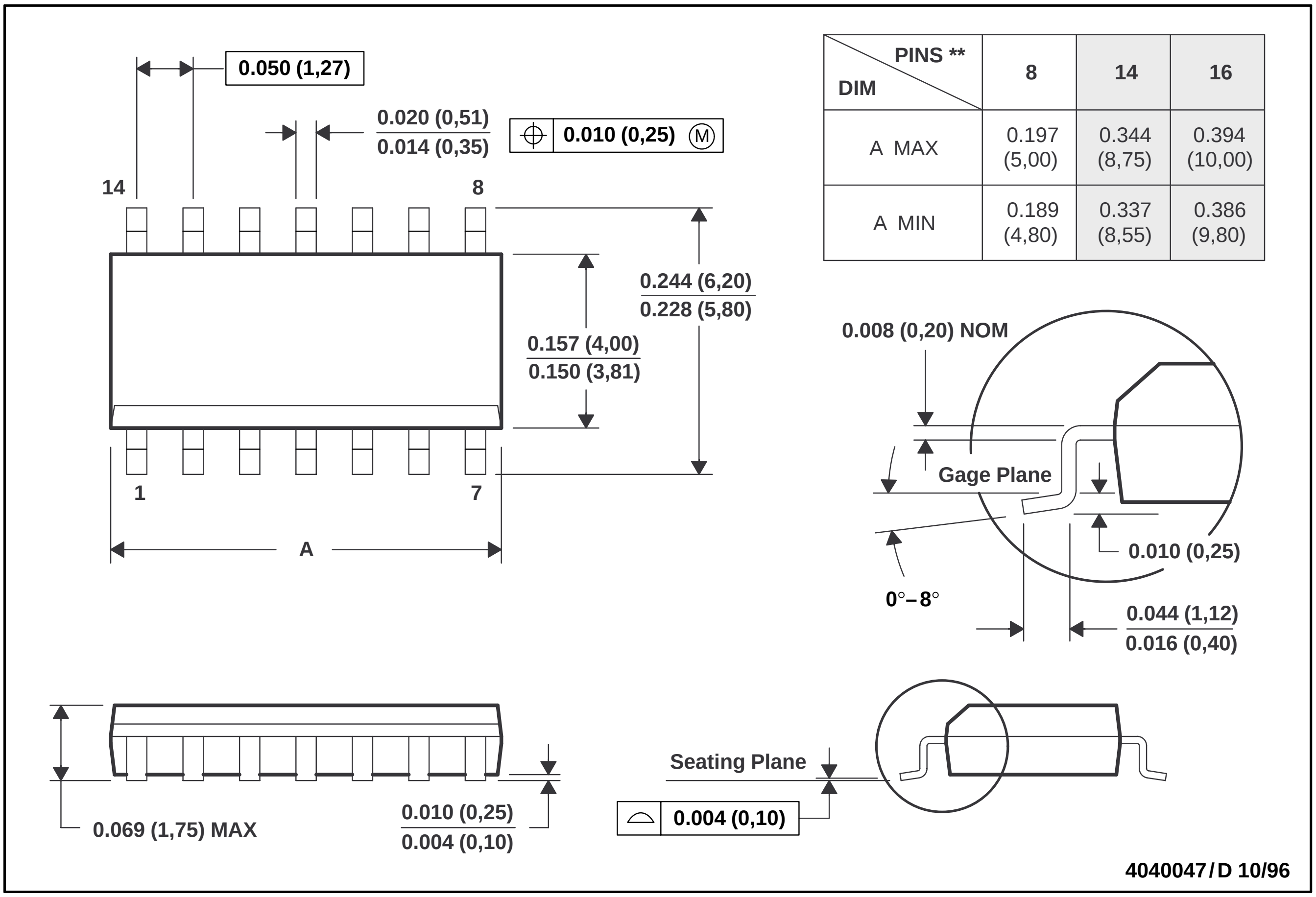
MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

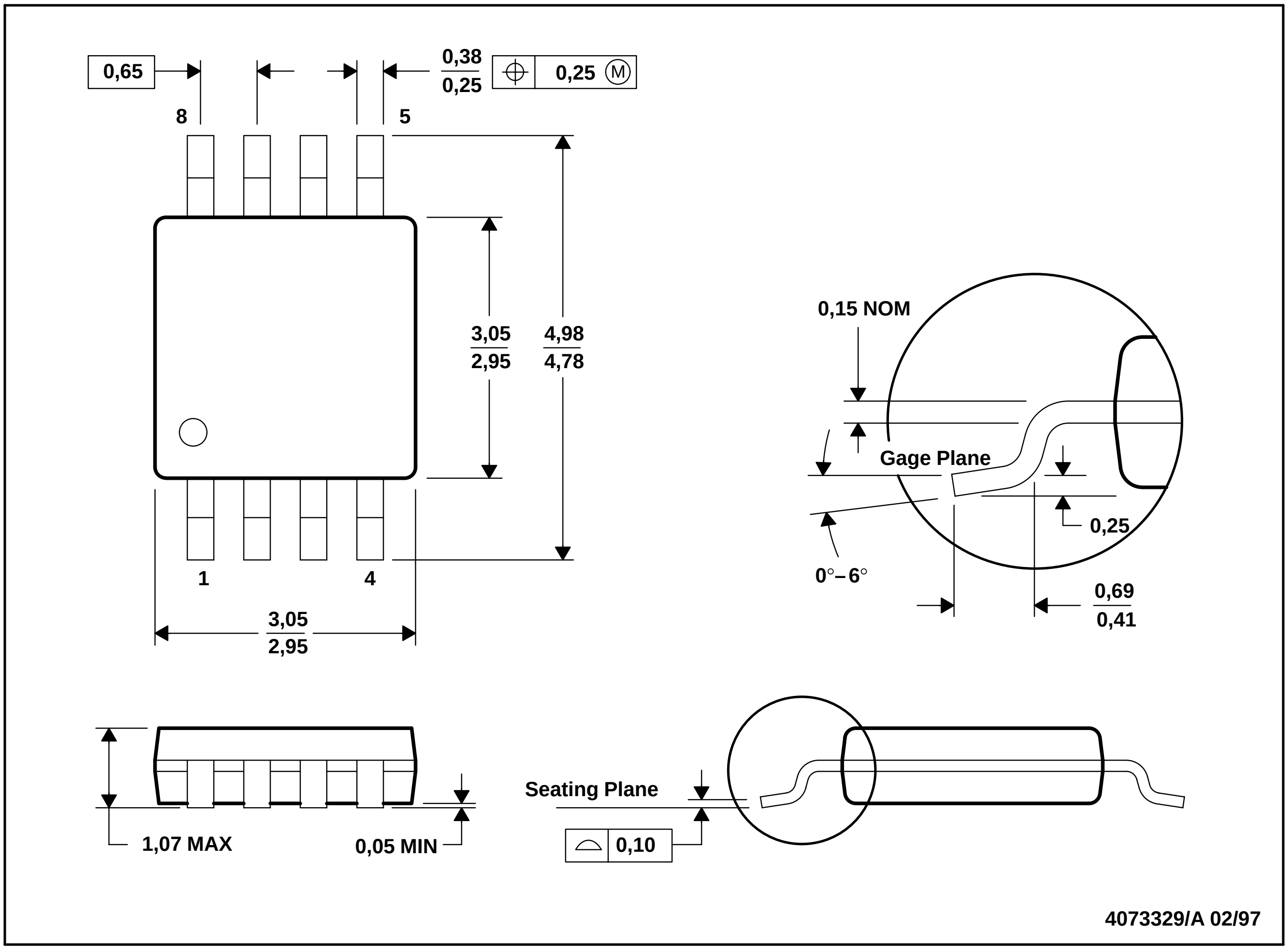


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

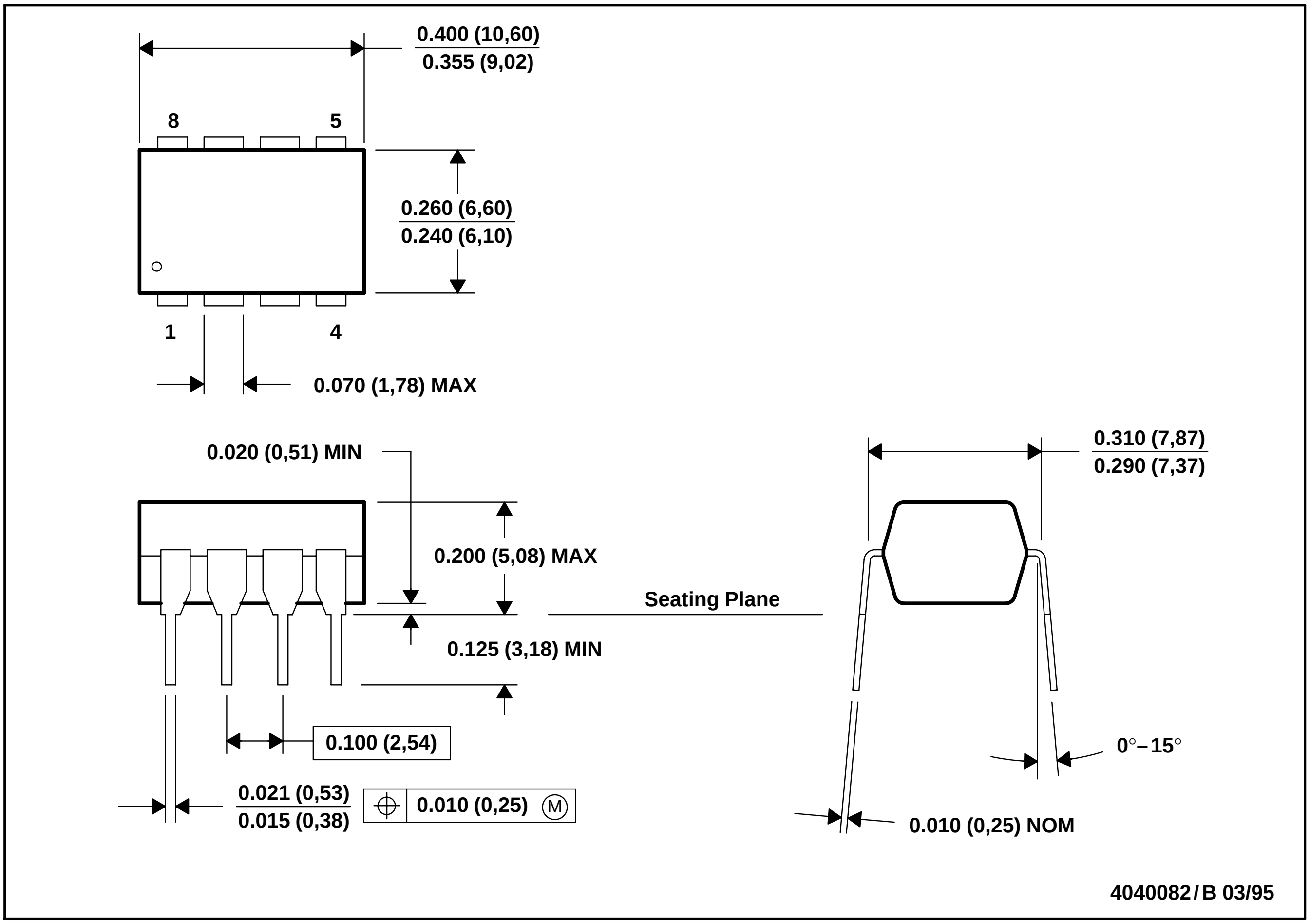
DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001