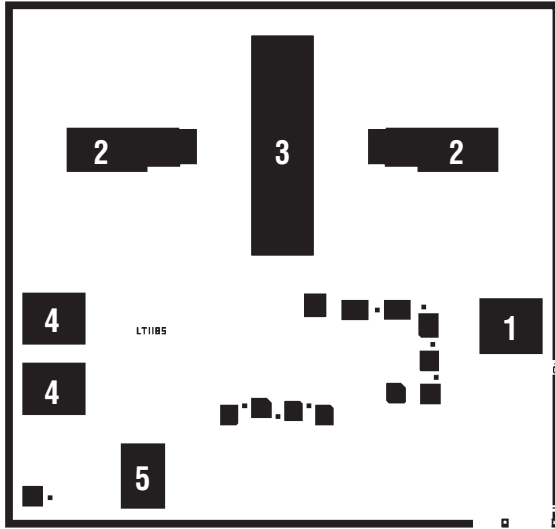


RH1185AMK

Negative Regulator with Adjustable Current Limit



110mils × 116mils
Backside metal: Alloyed Gold Layer
Backside Potential: V_{IN} Pads 2

PAD FUNCTION

1. REF
2. V_{IN}
3. V_{OUT}
4. GND
5. FB

DIE CROSS REFERENCE

LTC Finished Part Number	Order Part Number
RH1185AMK RH1185AMK	RH1185AMK DICE RH1185AMK DWF*

Please refer to LTC standard product data sheet for other applicable product information.

*DWF = DICE in wafer form.

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DICE/DWF ELECTRICAL TEST LIMITS $V_{IN} = 7.4V$, $V_{OUT} = 5V$, $I_{OUT} = 1mA$, $R_{LIM} = 4.02k$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage (at FB Pin, Note 2)	$V_{IN} - V_{OUT} = 5V$, $V_{OUT} = V_{REF}$	-2.344	-2.37	-2.396	V
Feedback Pin Bias Current	$V_{OUT} = V_{REF}$			2	μA
Dropout Voltage (Note 3)	$I_{OUT} = 0.5A$, $V_{OUT} = 5V$			0.4	V
	$I_{OUT} = 3A$, $V_{OUT} = 5V$			1.05	V
Line Regulation (Note 6)	$V_{IN} - V_{OUT} = 1V$ to $20V$, $V_{OUT} = 5V$			0.01	%/V
Minimum Input Voltage (Note 4)	$I_{OUT} = 1A$, $V_{OUT} = V_{REF}$			4.5	V
Internal Current Limit (Note 8)	$V_{IN} - V_{OUT} = 1.5V$	3.3		4.2	A
	$V_{IN} - V_{OUT} = 20V$	1		2.6	A
	$V_{IN} - V_{OUT} = 30V$	0.2		1	A
External Current Limit (Note 7)	$R_{LIM} = 5k$, $V_{OUT} = 1V$	2.7		3.3	A
	$R_{LIM} = 15k$, $V_{OUT} = 1V$	0.9		1.1	A
Quiescent Supply Current (Note 5)	$I_{OUT} = 5mA$, $V_{OUT} = V_{REF}$, $4V \leq V_{IN} \leq 25V$			3.5	mA

Note 1: Dice are probe tested at 25°C to the limits shown except for high current tests. Dice are tested under low current conditions which assure full load current specifications when assembled in packaging systems approved by Linear Technology. For absolute maximum ratings, typical specifications, performance curves and finished product specifications, please refer to the standard product RH data sheet.

Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications in the LT1185 data sheet for output changes due to heating effects.

DICE/DWF SPECIFICATION

RH1185AMK

DICE/DWF ELECTRICAL TEST LIMITS $V_{IN} = 7.4V$, $V_{OUT} = 5V$, $I_{OUT} = 1mA$, $R_{LIM} = 4.02k$, unless otherwise noted.

Note 3: Dropout voltage is tested by reducing input voltage until the output drops 1% below its nominal value. Tests are done at 0.5A and 3A. The power transistor looks basically like a pure resistance in this range so that minimum differential at any intermediate current can be calculated by interpolation; $V_{DROPOUT} = 0.25V + 0.25\Omega \cdot I_{OUT}$. For load current other than 0.5A and 3.0A, see the graph in the LT1185 data sheet.

Note 4: Minimum input voltage is limited by base emitter voltage drive of the power transistor section, not saturation as measured in Note 3. For output voltages below 4V, minimum input voltage specification may limit dropout voltage before transistor saturation limit.

Note 5: Supply current is measured on the ground pin, and does not include load current, R_{LIM} , or output divider current.

Note 6: Line regulation is measured on a pulse basis with a pulse width of $\approx 2ms$ to minimize heating. DC regulation will be affected by thermal regulation and temperature coefficient of the reference. See the Applications Information section of the LT1185 data sheet for details.

Note 7: External current limit is programmed with a resistor from REF pin to GND pin. The value is $15K \cdot A/I_{LIMIT}$.

Note 8: For $V_{IN} - V_{OUT} = 1.5V$, $V_{IN} = 5V$ and $V_{OUT} = 3.5V$. For all other current limit tests $V_{OUT} = 1V$.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-1185AMK