DATA SHEET

# GPCH8501A

## 8-Channel Sound Controller

DEC. 02, 2008

Version 1.4

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# 8-CHANNEL SOUND CONTROLLER

## 1.GENERAL DESCRIPTION

The GPCH8501A embedded with an 8-bit processor, 512K bytes OTP ROM chip, 512 bytes working SRAM, 3 sets of 12-bit timers, 24 general I/Os, and 1 set of 12-bit DAC. The microprocessor can implement software based on audio processing, functional control and others. For audio processing, melody and speech can be mixed into one output. The GPCH8501A implement a high performance SPU voice engine to achieve 8 channel voices with ADPCM/PCM. It operates over a wide voltage range of 2.4V - 5.5V and it includes Low Voltage Reset function to assure system operating appropriately under low voltage condition. In addition, GPCH8501A provide sleep mode for power savings. It can be awaken from sleep mode by interrupt source or by IOA's state change.

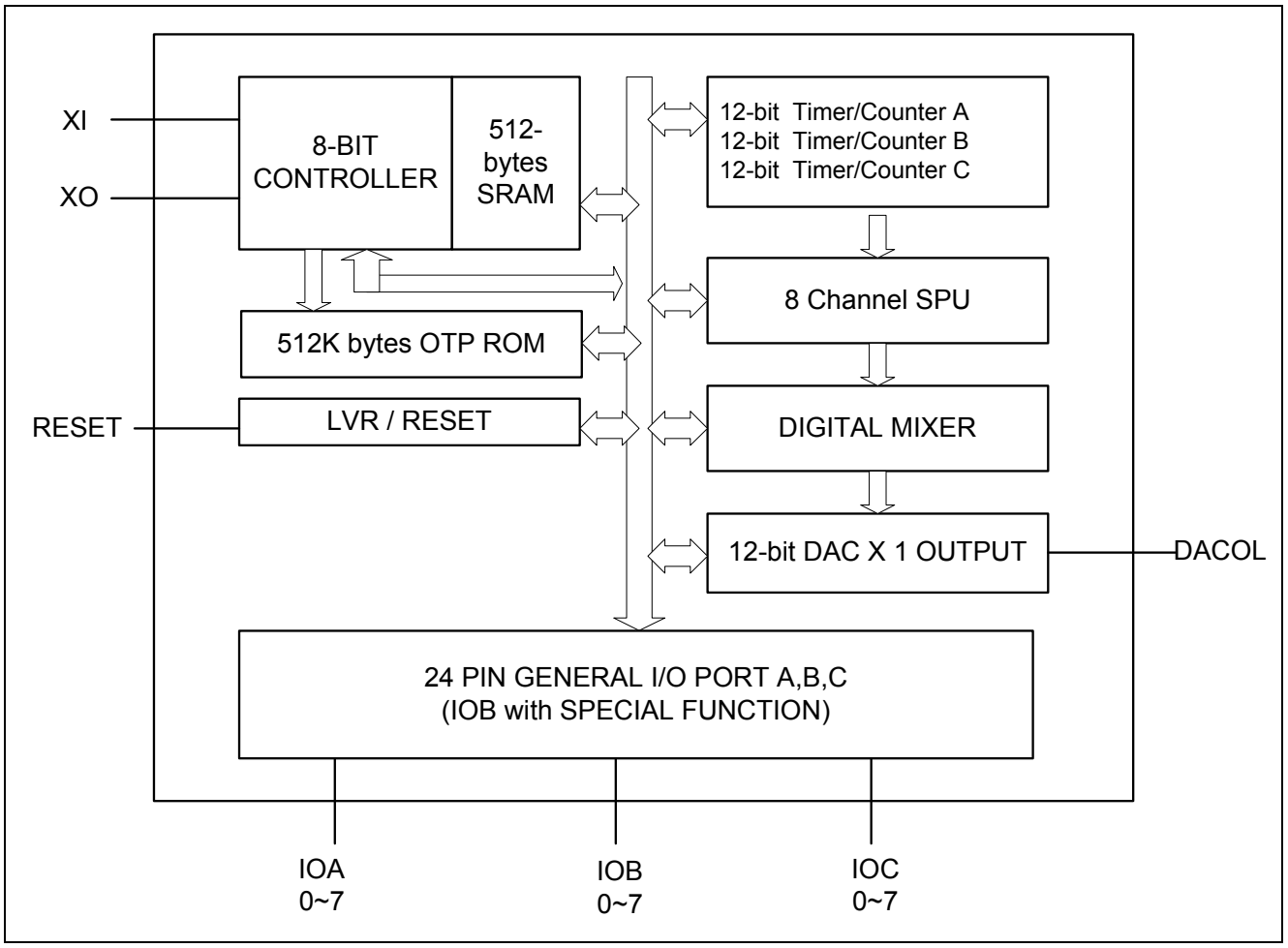
## 2.FEATURES

- Working Voltage: 2.4V - 5.5V
- CPU Speed: 7.159MHz.
- $F_{OSC}$ = 14.318MHz (2 x CPU clock)
- ROM Size: 512K bytes OTP ROM
- RAM Size: 512 bytes (Programmable RAM 384 bytes)
- Three 12-bit timers/counters, TMA/TMB/TMC (Programmable and Auto Reload)
- Sleep mode to reduce power
- Key change wake up function
- 10 IRQs & 6 NMI Interrupts
- Watchdog Function
- Low Voltage Reset: 2.2V
- 24 general I/Os, including 8 general/special I/Os (All bit programmable)
- 8-bit I/O with high sink current(20mA) for LED application
- IOA with 1M pull low function to prevent current leakage from error key touch
- One 12-bit DAC outputs (D/A output: 4mA/channel)
- SPU(Sound Processing Unit) engine can output audio data of 15-bit resolution with 12-bit DAC to perform high quality sound
- IR PWM Output
- 8-channel SPU engine with ADPCM/PCM wave table
- Tone color (Speech) with ADPCM algorithm to save memory usage

## 3.APPLICATION FIELD

- Talking Instrument Controller
- General Music Synthesizer
- Industrial Controller
- High End Toy Controller
- Intelligent Education Toys
- and more

## 4.BLOCK DIAGRAM

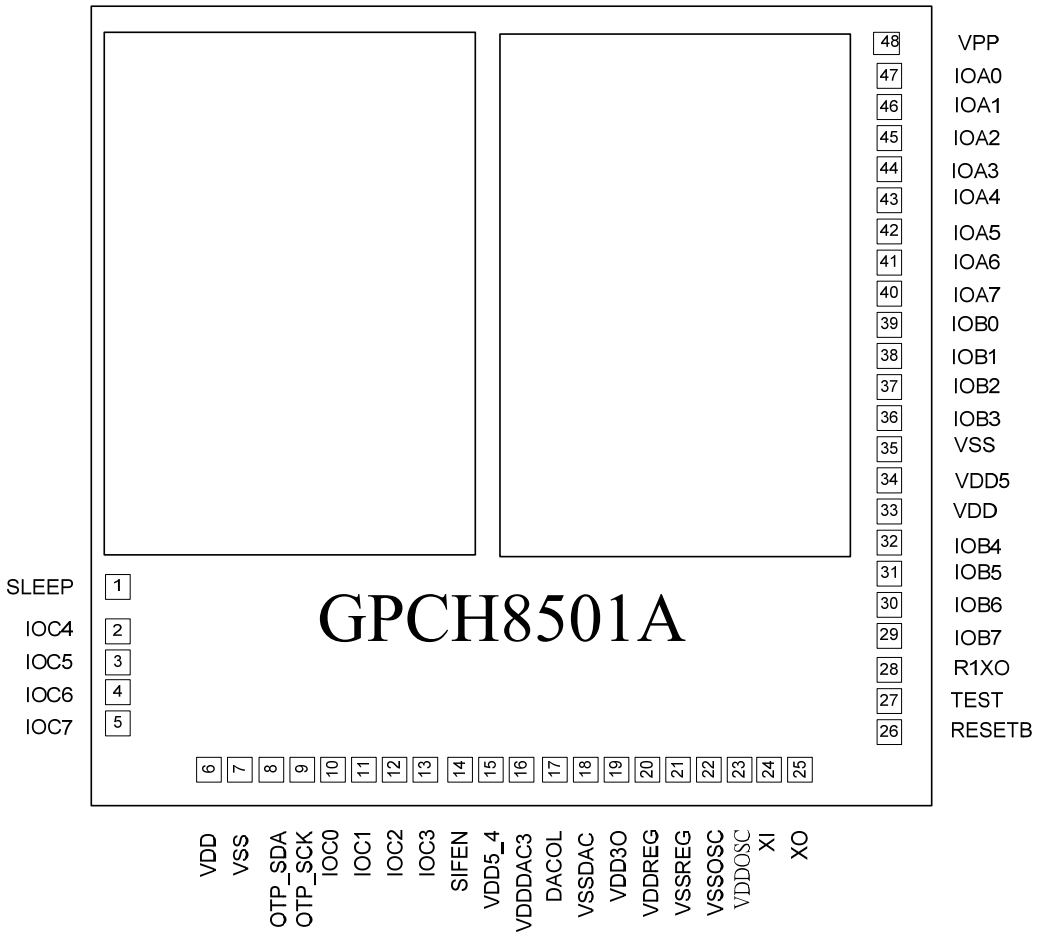


## 5. SIGNAL DESCRIPTIONS

| Name | PIN No. | LQFP128 PIN No. | LQFP44 PIN No. | Type | Description | Pull hi/low/float |
|---|---|---|---|---|---|---|
| IO PORT | | | | | | |
| IOA0~IOA7 | 47-40 | 90-83 | 34-31, - | I/O | Bi-directional IO ports, can be wakeup pins | - |
| IOB0~IOB7 | 39-36, 32-29 | 82-79, 75-72 | 30-29, - | I/O | Bi-directional IO ports | - |
| IOC0~IOC7 | 10-13, 2-5 | 41-44, 23-26 | 6-9, - | I/O | Bi-directional IO ports | - |
| OTP Related | | | | | | |
| OTP_SCK | 9 | 40 | 11 | I | Serial clock for 512K byte OTP | Pull-low |
| OTP_SDA | 8 | 39 | 10 | I/O | Serial data bus for 512K byte OTP | - |
| SIFEN | 14 | 46 | - | I | Internal OTP controller enable (with serial interface) | Pull-hi |
| Clock Related | | | | | | |
| XO | 25 | 58 | 22 | O | Oscillator Crystal output | - |
| XI | 24 | 57 | 21 | I | Oscillator crystal input./ROSC input | Pull-low |
| R1XO | 28 | 67 | 25 | I | ROSC mode(1) or Crystal mode(0) | Floating |
| Power Pad | | | | | | |
| VDD | 6, 33 | 36, 76 | 26 | I | Positive supply for logic (from VDD3O) | - |
| VSS | 7, 35 | 37, 78 | 28 | I | Ground reference for logic and I/O pins | - |
| VDD5_4,VDD5 | 15, 34 | 47, 77 | 12, 27 | I | Positive supply for I/O pins(2.4~5.5 V) | - |
| VDDDAC3 | 16 | 48 | 13 | I | Positive supply for DAC | - |
| VSSDAC | 18 | 51 | 15 | I | Ground reference for DAC | - |
| VDDREG | 20 | 53 | 17 | I | Positive supply for REGULATOR(2.4~5.5 V) | - |
| VSSREG | 21 | 54 | 18 | I | Ground reference for regulator | - |
| VDD3O | 19 | 52 | 16 | O | 3V power output from regulator | - |
| VDDOSC | 23 | 56 | 20 | I | Positive supply for oscillator | - |
| VSSOSC | 22 | 55 | 19 | I | Ground reference for oscillator | - |
| VPP | 48 | 107 | 35 | I | OTP high voltage source for program | - |
| Others | | | | | | |
| RESETB | 26 | 65 | 23 | I | External reset pin(active low) | Pull-hi |
| TEST | 27 | 66 | 24 | I | Test mode | Pull-low |
| DACOL | 17 | 50 | 14 | O | Left DAC output | - |
| SLEEP | 1 | 20 | 5 | O | Sleep indicator | - |

I.e. Total 48 pads.

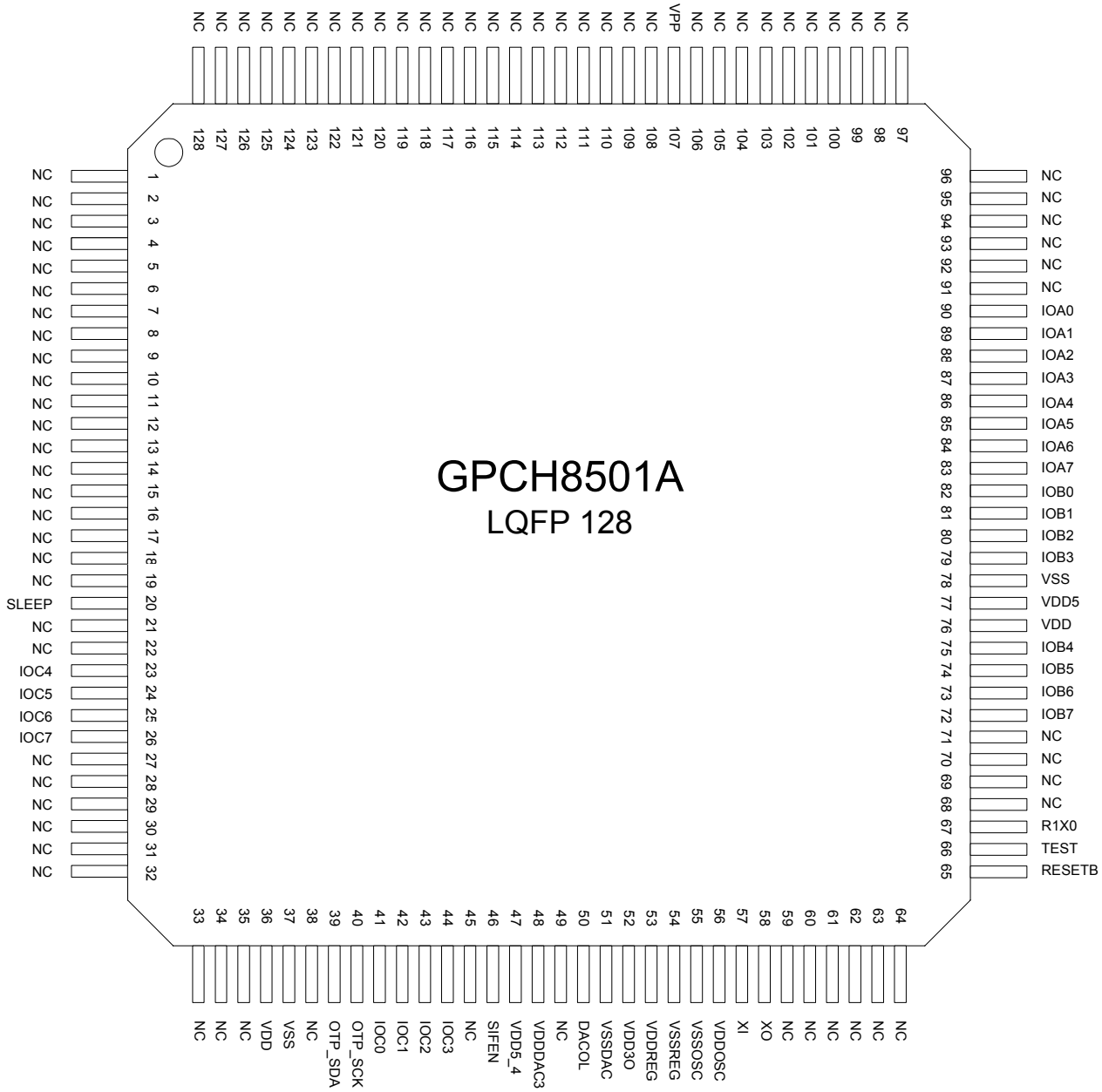
### 5.1. PAD Assignment



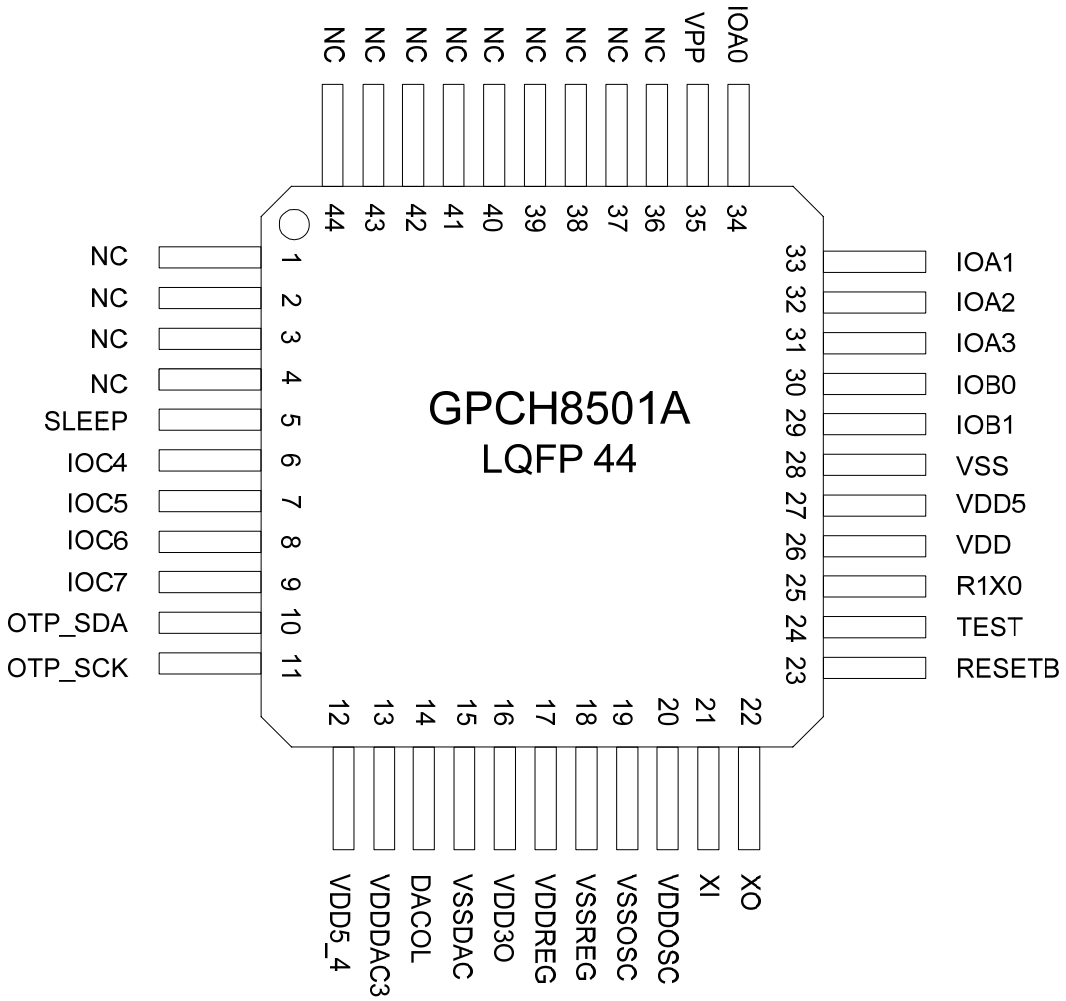

This IC substrate should be connected to VSS

**Note1:** To ensure that the IC functions properly, please bond all of VDD and VSS pins.
**Note2:** The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

### 5.2. Pin Map - LQFP 128



### 5.3. Pin Map - LQFP 44



## 6. FUNCTIONAL DESCRIPTIONS

### 6.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000~$0002FF.

### 6.2. ROM

GPCH8501A can be selected to use internal OTP ROM with 512k bytes.

### 6.3. Low Voltage Reset

The GPCH8501A provides another important feature, Low Voltage Reset (LVR). Without LVR, CPU may become unstable and malfunctioning when operating voltage drops below 2.2V. It will reset all functions to the initial operational (stable) states when the voltage drops below 2.2V by LVR.

### 6.4. Interrupt

The GPCH8501A has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls 10 IRQs and 6 NMIs. A NMI cannot be interrupted by any other IRQs. An IRQ can be interrupted by a NMI and by a high priority IRQ.

| Interrupt Source | Interrupt Name | Priority |
|---|---|---|
| Timer A | NMI_TIMER_A | NMI |
| Timer B | NMI_TIMER_B | NMI |
| Timer C | NMI_TIMER_C | NMI |
| CPU_CLOCK/1024 | NMI_D1024 | NMI |
| KEY | NMI_KEY | NMI |
| EXT | NMI_EXT | NMI |
| TIMER A | IRQ_TIMER_A | IRQ1 |
| TIMER B | IRQ_TIMER_B | IRQ2 |
| TIMER C | IRQ_TIMER_C | IRQ3 |
| CPU_CLOCK/1024 | IRQ_D1024 | IRQ4 |
| CPU_CLOCK/4096 | IRQ_D4096 | IRQ5 |
| CPU_CLOCK/262144 | IRQ_D262144 | IRQ6 |
| CPU_CLOCK/2097152 | IRQ_D2097152 | IRQ7 |
| KEY | IRQ_KEY | IRQ8 |
| EXT | IRQ_EXT | IRQ9 |
| SPU | IRQ_SPU | IRQ10 |

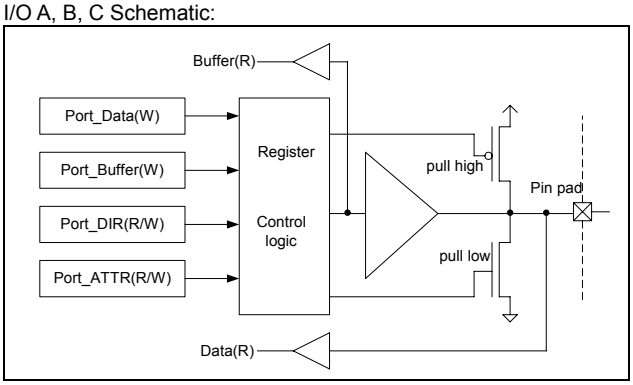
### 6.5. I/O

The purpose of input and output ports is to communicate with other devices. Four programmable I/O ports are built-in, including Port A, B, and C. The PortA is a general I/O with programmable wake-up capability. In addition to general I/O function, PortB also offers some special functions in certain pins. Refer to **Special Function in PortB**. PortC0~7 provides large sink current (20mA) for LED application.

#### 6.5.1. I/O configuration

The following diagram represents the I/O schematic.

I/O A, B, C Schematic:



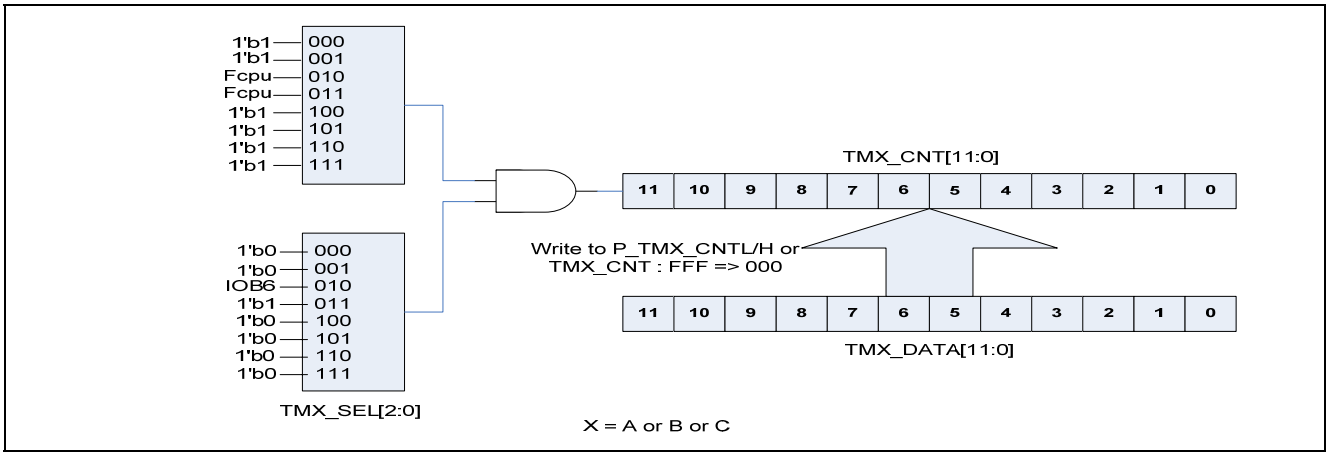

Port_Data and Port_Buffer are written into the same register but read from different node. The IOA [7:0] is the key wakeup port. To activate key wakeup function, first latch data on IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from first latched data. In addition to a general I/O port, PortB can be assigned to some special functions. A summary of PortB special functions is listed as follows.

**Special Function in PortB**

| PortB | Special Function | Function Description | Note |
|---|---|---|---|
| IOB5 | PWMO IR | IR carrier frequency output | Refer to Timer/Counter section |
| IOB6 | EXT | External interrupt source | Negative edge trigger INT(default) |
| | Feedback Output | Works with IOB7 by adding a RC circuit between them to get an OSC to EXT interrupt | - |
| IOB7 | Feedback Input | Schmitt Inverter Input | - |

### 6.6. Timer/Counter (Timer A/Timer B/Timer C)

Three timers are embedded in GPCH8501A, timer A, B and C. All three timers have the same behavior which includes 12-bit up counter and a preload register and programmable clock source. Timer A can also be the clock source of the software channel. The clock source of each timer can be set individually. Two clock sources including CPU clock and external clock can be selected individually or combined together for timer's clock source.




| Select | Input 1 | Input 2 | Function | Comment |
|---|---|---|---|---|
| 000 | '1' | '0' | Disable | Disable |
| 001 | '1' | '0' | Disable | Disable |
| 010 | $F_{CPU}$ | IOB6 | Duration count by $F_{CPU}$ | Duration count by $F_{CPU}$ |
| 011 | $F_{CPU}$ | '1' | Timer by $F_{CPU}$ | Timer by $F_{CPU}$ |
| 100 | '1' | '0' | Disable | Disable |
| 101 | '1' | '0' | Disable | Disable |
| 110 | '1' | '0' | Disable | Disable |
| 111 | '1' | '0' | Disable | Disable |

### 6.7. Sleep, Wakeup and Watchdog

#### 6.7.1. Sleep and Wakeup

Sleep mode is to save power by stopping clock running while device is not in use. When sleep acts, the device runs from operating mode to standby mode. Wake-up from sleep mode will turn back to operating mode.

1). Sleep: After power on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter sleep mode.

2). Wake-up: While an IRQ/NMI interrupt signal is generated, GPCH8501A is waking up from sleep mode. While wake-up completed, program counter will continue to execute the next command.

#### 6.7.2. Watchdog

The purpose of watchdog is to monitor system's operation normally. Within a certain period, watchdog must be cleared; otherwise, CPU assumes the program has been running in an abnormal condition and therefore, CPU will reset the system to the initial state and start running the program from program's beginning. It protects the system from incorrect code execution by generating a system reset when the watchdog timer overflows as a result of failure of software to clear the timer within 0.75 seconds. Watchdog function can be removed by option.

### 6.8. Speech and DAC

The GPCH8501A uses a high performance SPU voice engine to archive 8-channel voice with ADPCM/PCM. The SPU also supports automatic zero-crossing concatenating function. A hardware multiplier is also embedded in this SPU for software usage. The fixed address of RAM area $0000 - $007F is designed as address pointers and a data buffer for the 8 channel speech/melody generation. There is one 12-bit D/A with 4mA driving current for audio output.

## 7. ELECTRICAL SPECIFICATIONS

### 7.1. Absolute Maximum Ratings

| Characteristics | Symbol | Ratings |
|---|---|---|
| DC Supply Voltage | $V_+$ | < 7.0V |
| Input Voltage Range | $V_{IN}$ | -0.5V to $V_+$ + 0.5V |
| Operating Temperature | $T_A$ | 0℃ to +60℃ |
| Storage Temperature | $T_{STO}$ | -50℃ to +150℃ |

**Note:** Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see DC Electrical Characteristics.

### 7.2. DC Characteristics (VDD5/VDD5_4 = 3.0V, $T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 2.4 | - | 3.6 | V | For 2-battery |
| Operating Current | $I_{OP}$ | - | 9 | - | mA | $F_{CPU}$ = 7.0MHz, no load, midi playing with inner OTP Rom, DAC enabled |
| Standby Current | $I_{STB}$ | - | - | 4.0 | μA | VDD5/VDD5_4 = 3.0V |
| OSC Frequency | $F_{OSC}$ | - | - | 15 | MHz | VDD5/VDD5_4 = 3.0V |
| Input High Level | $V_{IH}$ | 0.7 VDD | - | VDD | V | - |
| Input Low Level | $V_{IL}$ | VSS | - | 0.3VDD | V | - |
| Audio Output Current | $I_{AUD}$ | - | -1.9 | - | mA | - |
| Output High Current | $I_{OH}$ | -2.6 | - | - | mA | VDD5/VDD5_4 = 3.0V, $V_{OH}$ = 2.7V |
| Output Low Current (IOA7:0, IOB7:0) | $I_{OL1}$ | 2.7 | - | - | mA | VDD5/VDD5_4 = 3.0V, $V_{OL}$ = 0.3V |
| Output Low Current (IOC7:0) | $I_{OL2}$ | 12 | - | - | mA | VDD5/VDD5_4 = 3.0V, $V_{OL}$ = 0.3V |
| Input Pull-Low Resister (PA7:0) | $R_{PL}$ | - | 1900 | - | KΩ | $V_{IN}$ = VDD5/VDD5_4 |
| Input Pull-High Resister (PA7:0, PB7:0, PC7:0) | $R_{PH}$ | - | 180 | - | KΩ | $V_{IN}$ = VSS |

### 7.3. DC Characteristics (VDD5/VDD5_4 = 5.0V, $T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 3.6 | - | 5.5 | V | For 3-battery |
| Operating Current | $I_{OP}$ | - | 13 | - | mA | $F_{CPU}$ = 7.0MHz, no load, midi playing with inner OTP Rom, DAC enabled |
| Standby Current | $I_{STB}$ | - | - | 5.0 | μA | VDD5/VDD5_4 = 5.0V |
| OSC Frequency | $F_{OSC}$ | - | - | 15 | MHz | VDD5/VDD5_4 = 5.0V |
| Input High Level | $V_{IH}$ | 0.7 VDD | - | VDD | V | - |
| Input Low Level | $V_{IL}$ | VSS | - | 0.3VDD | V | - |
| Audio Output Current | $I_{AUD}$ | - | -3.9 | - | mA | - |
| Output High Current | $I_{OH}$ | -6.0 | - | - | mA | VDD5/VDD5_4 = 5.0V, $V_{OH}$ = 4.5V |
| Output Low Current (IOA7:0, IOB7:0) | $I_{OL1}$ | 6.0 | - | - | mA | VDD5/VDD5_4 = 5.0V, $V_{OL}$ = 0.5V |

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output Low Current (IOC7:0) | $I_{OL2}$ | 27 | - | - | mA | VDD5/VDD5_4 = 5.0V, $V_{OL}$ = 0.5V |
| Input Pull-Low Resister (PA7:0) | $R_{PL}$ | - | 900 | - | KΩ | $V_{IN}$ = VDD5/VDD5_4 |
| Input Pull-High Resister (PA7:0, PB7:0, PC7:0) | $R_{PH}$ | - | 90 | - | KΩ | $V_{IN}$ = VSS |

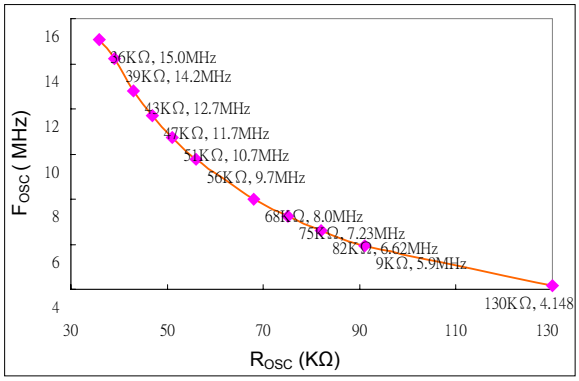
### 7.4. DAC Characteristics (VDD5 = 3.0V, $T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Resolution of DAC | RESO | - | - | 12 | bit |
| THD+N (f=1kHz) | SNR | - | 0.1 | - | % |
| Noise at no signal | - | - | -84 | - | dBr A |
| Dynamic range(-60dB) | - | - | -76.9 | - | dBr A |
| Sample Rate | $F_S$ | - | - | 400K | Hz |

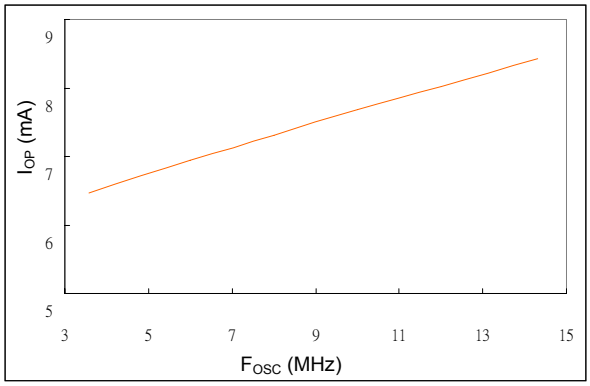
### 7.5. Regulator Characteristics ( $T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Input Voltage | VREGI | 2.4 | 4.5 | 5.5 | V |
| Maximum Current Output | IREGO | - | - | 30 | mA |
| Output Voltage | VREGO | 2.4 | 3 | 3.3 | V |
| Standby Current | IRGES | - | 3 | - | uA |

### 7.6. The Relationships between the $R_{OSC}$ and the $F_{CPU}$

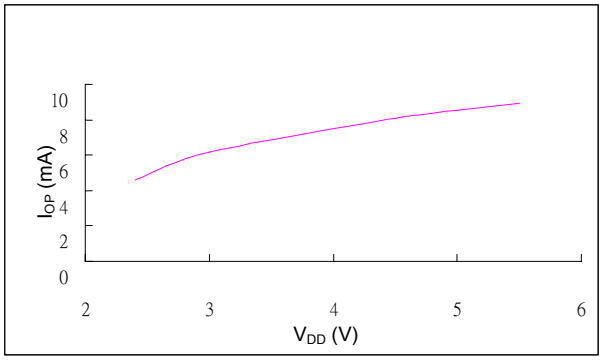



### 7.7. The Relationships between the $F_{CPU}$ and the $I_{OP}$



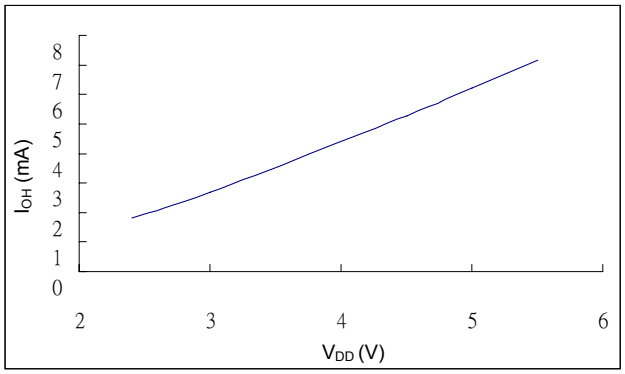
### 7.8. The Relationships between the $I_{OP}$ and the $V_{DD}$

#### 7.8.1. $F_{CPU}$ = 7.159 MHz. $V_{DD}$ = VDD5_4



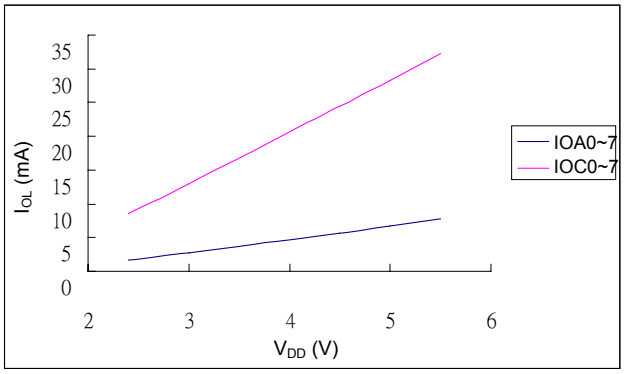

### 7.9. The Relationships between the $I_{OH}$ and the $V_{DD}$

#### 7.9.1. $V_{OH}$ = 0.9$V_{DD}$



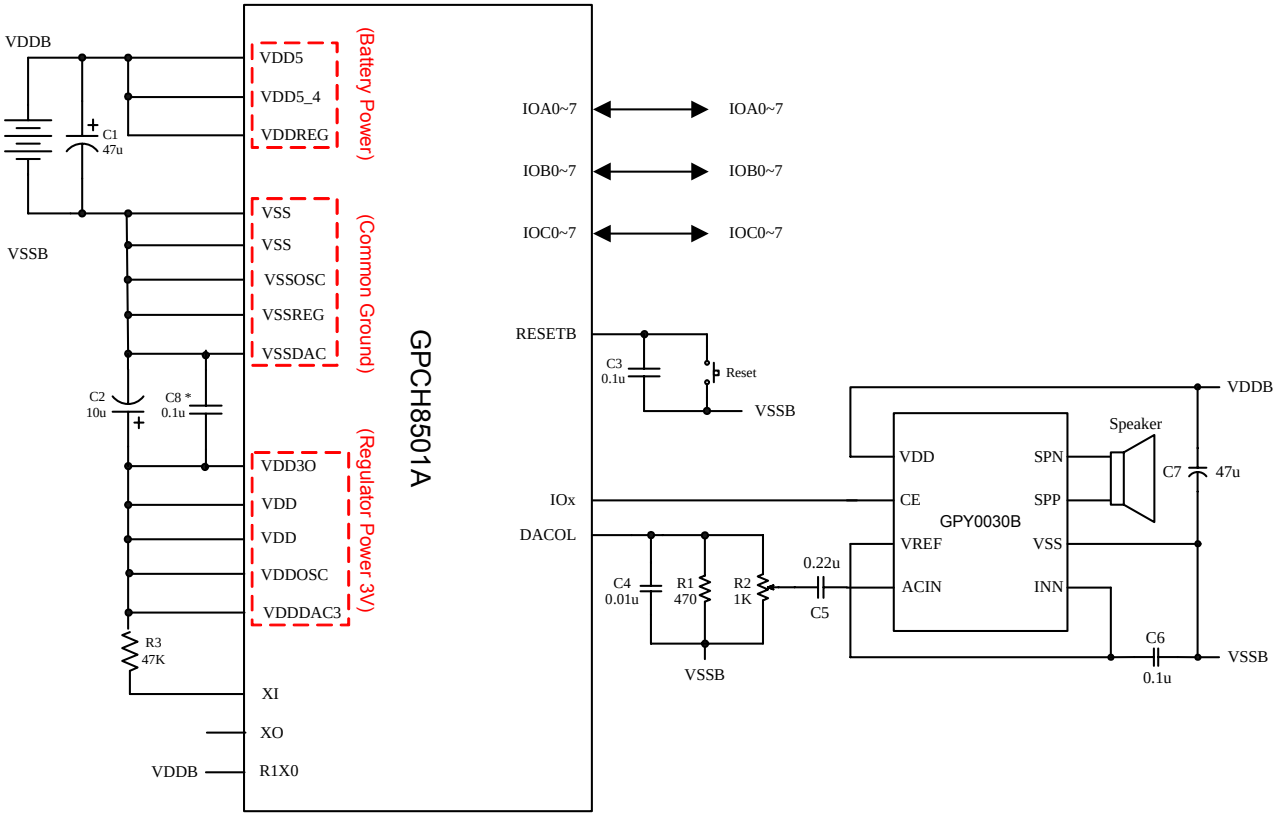

### 7.10. The Relationships between the $I_{OL}$ and the $V_{DD}$

#### 7.10.1. $V_{OL}$ = 0.1$V_{DD}$



## 8. APPLICATION CIRCUITS

### 8.1. GPCH8501A Application Circuit with $R_{OSC}$ Option




GPCH8501A application circuit with Rosc option

**Note*:** This capacitor can be removed if there is good power line layout on PCB that no harm to sound quality.

**Note:** Important note to power connection:

(a) Battery or Power supply connects to VDDB (including VDDREG, VDD5 and VDD5_4, 2.4V ~ 5.5V)

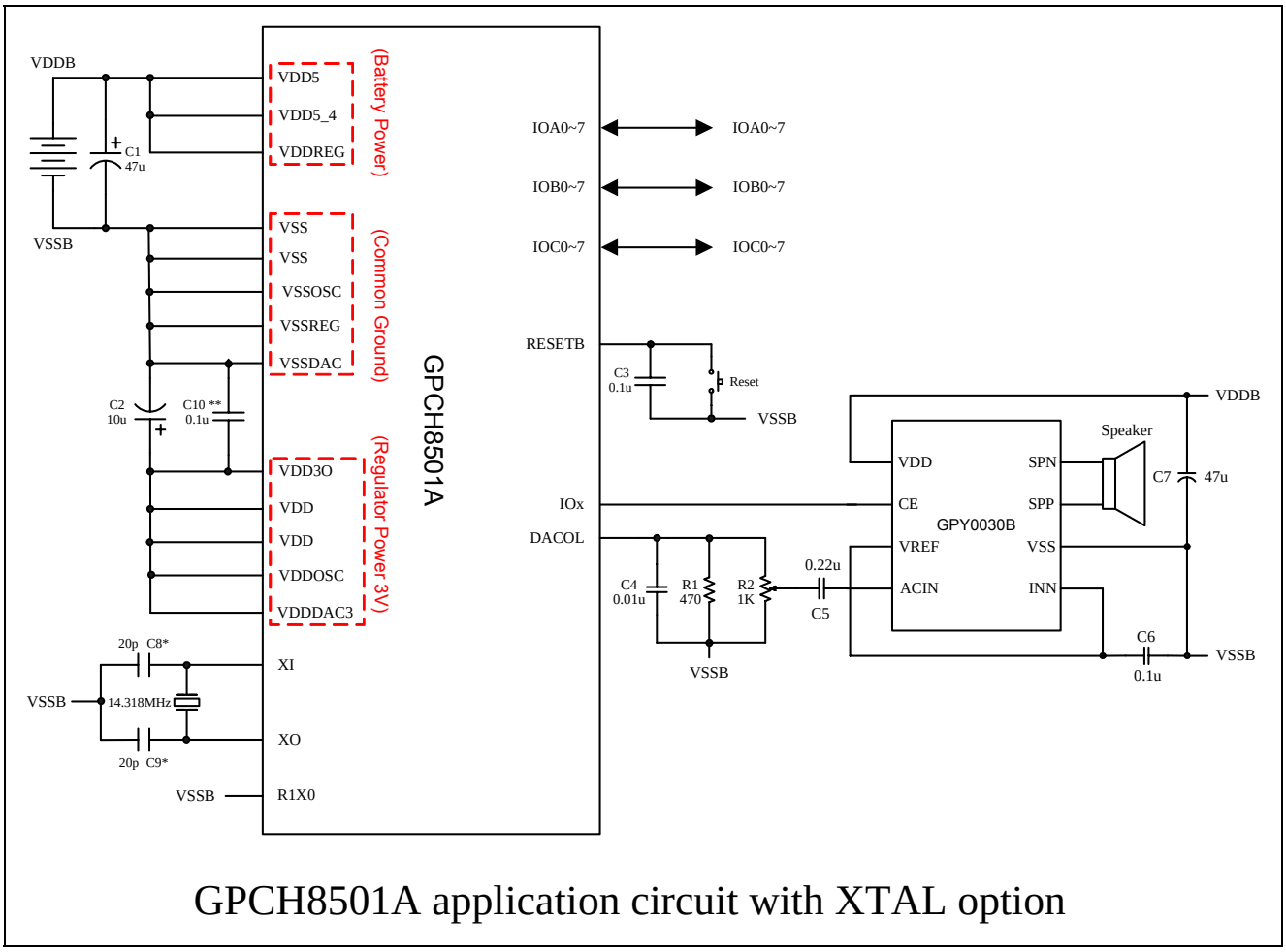
(b) VDD3O is internal regulator output that supplies power to VDD, VDDDAC3, VDDOSC, etc. Connect VDD3O, VDD, VDDDAC3 and VDDOSC all together.

(c) VDDB should NOT be connected to VDD3O, VDD, VDDDAC3, VDDOSC, etc.

(d) The built-in regulator can NOT be disabled, so user should NOT bypass this regulator.

(e) Recommended capacitor placement for power distribution on PCB: C1 close to battery, C2 close to VDD3O pad and C8 close to VDDDAC3 pad.

### 8.2. GPCH8501A Application Circuit with Crystal Option




GPCH8501A application circuit with XTAL option

**Note*:** These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

**Note**:** This capacitor can be removed if there is good power line layout on PCB that no harm to sound quality.

**Note:** Important note to power connection:

(a) Battery or Power supply connects to VDDB (including VDDREG, VDD5 and VDD5_4, 2.4V ~ 5.5V)

(b) VDD3O is internal regulator output that supplies power to VDD, VDDDAC3, VDDOSC, etc. Connect VDD3O, VDD, VDDDAC3 and VDDOSC all together.

(c) VDDB should NOT be connected to VDD3O, VDD, VDDDAC3, VDDOSC, etc.

(d) The built-in regulator can NOT be disabled, so user should NOT bypass this regulator.

(e) Recommended capacitor placement for power distribution on PCB: C1 close to battery, C2 close to VDD3O pad and C10 close to VDDDAC3 pad.

### 8.3. Current Mode DAC Speaker Driver

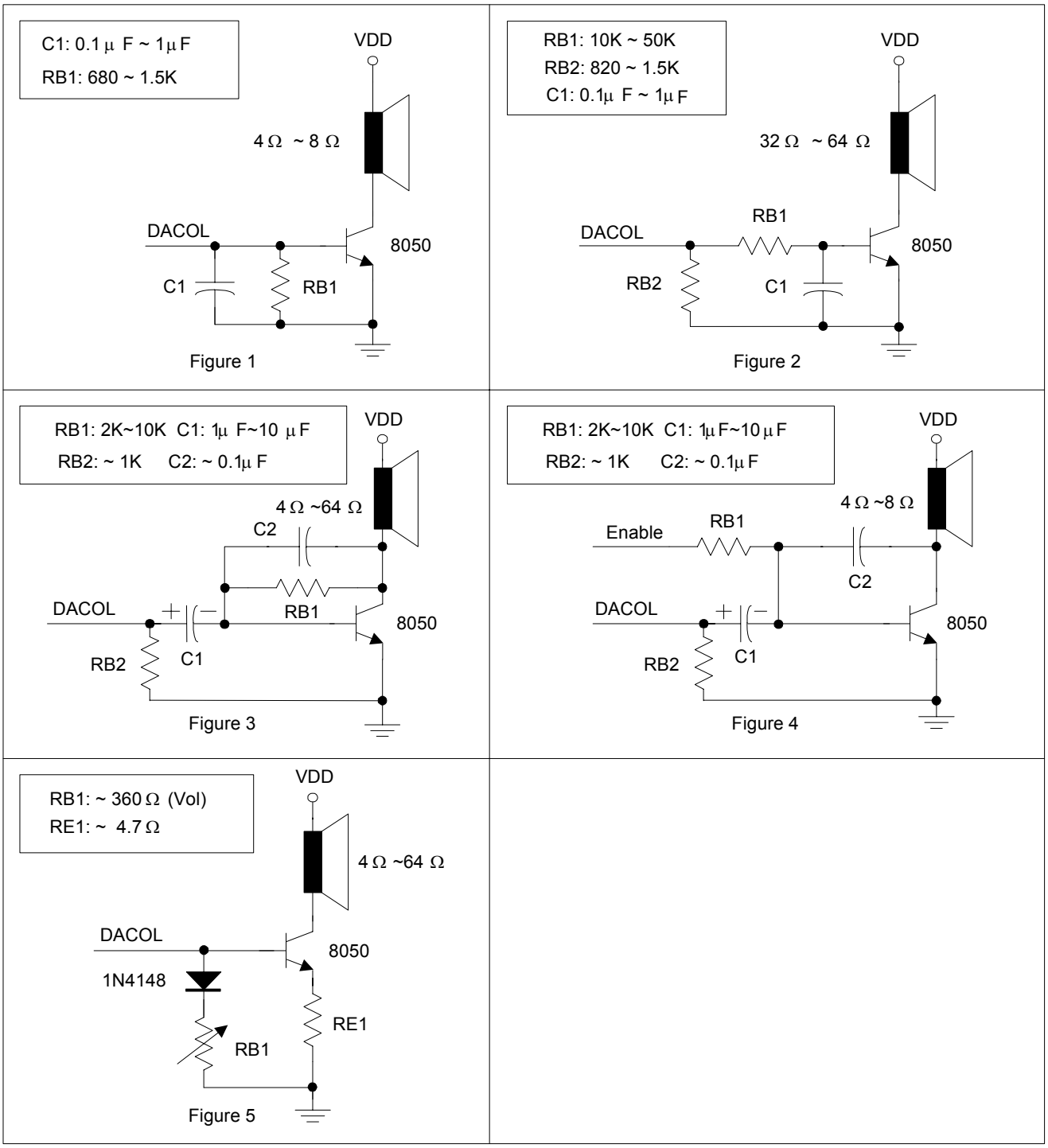



**Figure 1**: The simplest CKT uses with low impedance speaker. It has high operation current, but the cost is the cheapest.

**Figure 2**: It is the same as Figure 1 but a high impedance speaker is used.

**Figure 3**: The CKT has low pass filter. It can provide higher speech quality, but it always takes high operation current.

**Figure 4**: Improved version of Figure 3. The standby current can be controlled by enable pin.

**Figure 5**: The current mirror mode. It is able to control the volume. In addition, it has more stable and lower operation current than Figure 1-3.

## 9.PACKAGE/ORDERING INFORMATION

### 9.1. Ordering Information

| Product Number | Package Type |
|---|---|
| GPCH8501A-NnnV-C | Chip form |
| GPCH8501A-NnnV-QL09x | Halogen Free Package |
| GPCH8501A-NnnV-QL01x | Halogen Free Package |

**Note1:** Code number is assigned for customer.

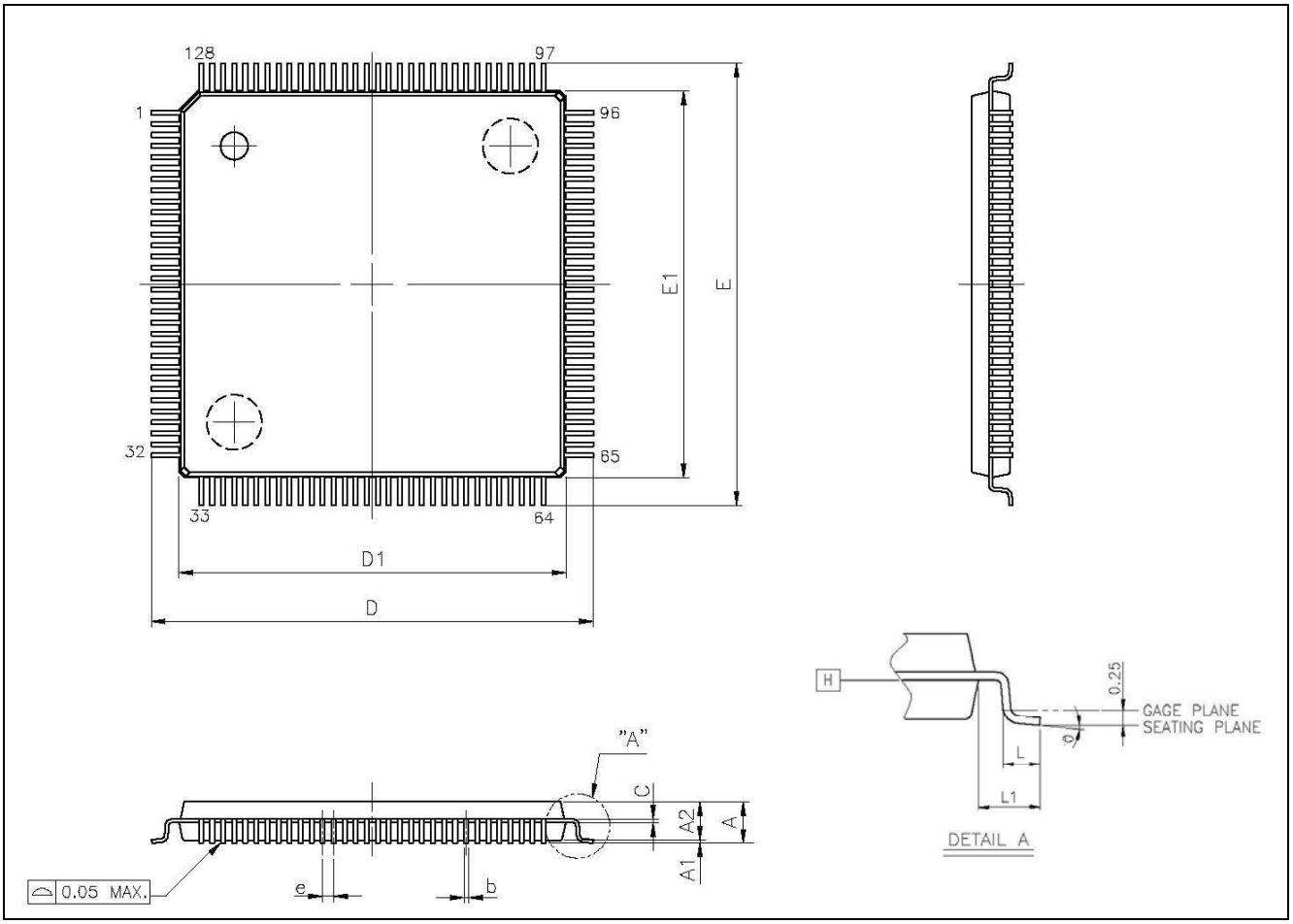
**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

**Note3:** Package form number (x = 1 - 9, serial number).

**Note4:** LQFP44 only bonds 10 IO pads, so IR carrier/External interrupt/RC Feedback function is not supported.

### 9.2. Package Information

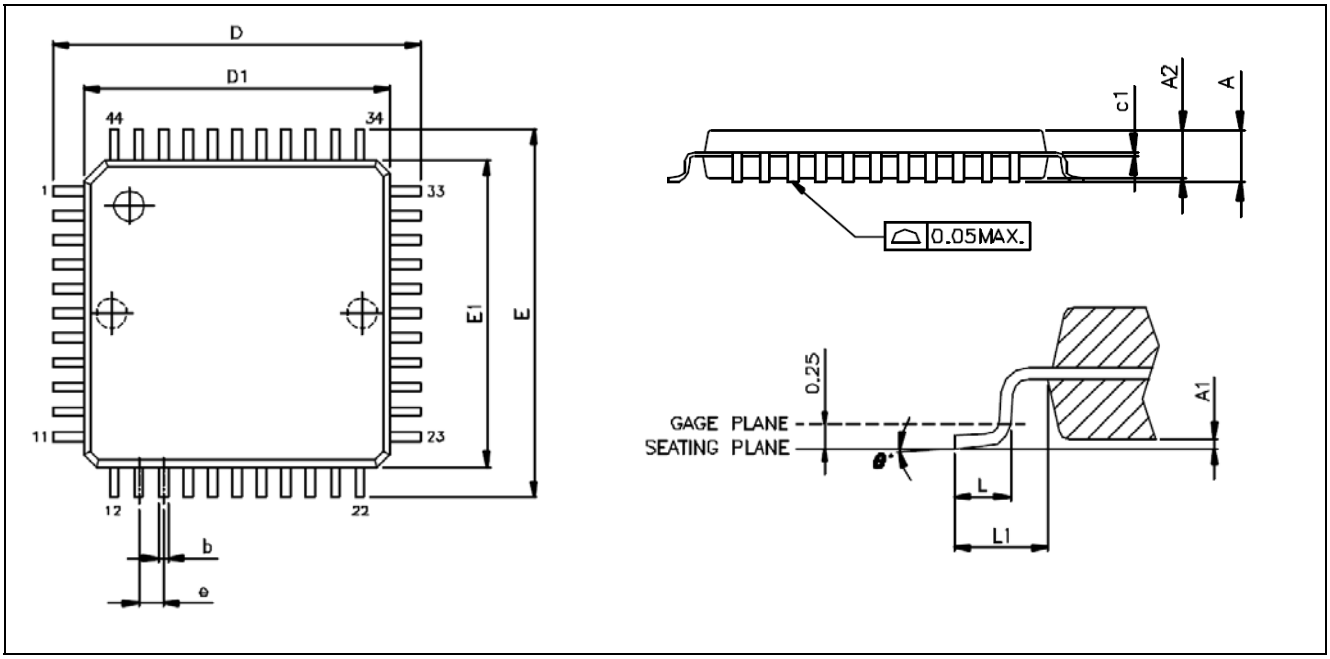
#### 9.2.1. LQFP 128-QL09




| Symbol | Dimension in Millimeter | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.13 | 0.16 | 0.23 |
| c | 0.09 | - | 0.20 |
| D | 16.00 BSC. | | |

| Symbol | Dimension in Millimeter | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| D1 | 14.00 BSC. | | |
| E | 16.00 BSC. | | |
| E1 | 14.00 BSC. | | |
| e | 0.40 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| $\theta$ | 0° | 3.5° | 7° |

### 9.2.2. LQFP 44-QL01




| Symbol | Dimension in Millimeter | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| c1 | 0.09 | - | 0.16 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| e | 0.80 BSC | | |
| b | 0.30 | 0.37 | 0.45 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| $\theta$° | 0° | 3.5° | 7° |

## 10. DISCLAIMER

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## 11. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| DEC. 02, 2008 | 1.4 | 1. Modify section 4. BLOCK DIAGRAM.<br>2. Modify 6.3 Low voltage reset.<br>3. Modify 7.4 DAC Characteristics.<br>4. Add 7.5 Regulator Characteristics.<br>5. Add note in section 8.1 Application circuits.<br>6. Add note in section 8.2 Application circuits.<br>7. Modify section 8.3 Current Mode DAC Speaker Driver. | 4<br>9<br>12<br>12<br>14<br>15<br>16 |
| AUG. 21, 2008 | 1.3 | 1. Modify section 5. SIGNAL DESCRIPTIONS.<br>2. Modify section 7.2 DC Characteristics (VDD5/VDD5_4 = 3.0V, TA = 25℃).<br>3. Modify section 7.3 DC Characteristics (VDD5/VDD5_4 = 5.0V, TA = 25℃).<br>4. Modify section 8.1 and 8.2 Application circuits. | 4<br>11<br>11<br>14, 15 |
| MAY. 13, 2008 | 1.2. | 1. Modify section 1. GENERAL DESCRIPTION.<br>2. Modify section 2. FEATURES.<br>3. Modify section 6.6 Timer/Counter (Timer A/Timer B/Timer C).<br>4. Modify section 8.1 and 8.2 Application circuits.<br>5. Modify section 8.4 Current Mode DAC Speaker Driver. | 3<br>3<br>10<br>15,16<br>18 |
| JAN. 29, 2008 | 1.1 | 1. Modify “DAC Characteristics” in section 7.4. | 12 |
| NOV. 05, 2007 | 1.0 | 1. Modify the “SIGNAL DESCRIPTIONS” in section 5.<br>2. Modify the “PACKAGE/ORDERING INFORMATION” in section 9. | 4-7<br>18-20 |
| AUG 27, 2007 | 0.1 | Original | 18 |