TPS7A84 High-Current (3 A), High-Accuracy (1%), Low-Noise (4.4 μV_{RMS}), LDO Voltage Regulator

1 Features

- Low Dropout: 180 mV (max) at 3 A
- 1% (max) Accuracy Over Line, Load, and Temperature
- Output Voltage Noise:
  - 4.4 μV_{RMS} at 0.8-V Output
  - 7.7 μV_{RMS} at 5.0-V Output
- Input Voltage Range:
  - Without BIAS: 1.4 V to 6.5 V
  - With BIAS: 1.1 V to 6.5 V
- ANY-OUT™ Operation:
  - Output Voltage Range: 0.8 V to 3.95 V
- Adjustable Operation:
  - Output Voltage Range: 0.8 V to 5.0 V
- Power-Supply Ripple Rejection:
  - 40 dB at 500 kHz
- Excellent Load Transient Response
- Adjustable Soft-Start In-Rush Control
- Open-Drain Power-Good (PG) Output
- Stable with a 47-µF or Larger Ceramic Output Capacitor
- 3.5-mm × 3.5-mm, 20-Pin VQFN

2 Applications

- Digital Loads: SerDes, FPGAs, and DSPs
- Instrumentation, Medical, and Audio
- High-Speed Analog Circuits:
  - VCO, ADC, DAC, and LVDS
- Imaging: CMOS Sensors and Video ASICs
- Test and Measurement

3 Description

The TPS7A84 is a low-noise (4.4 μV_{RMS}), low-dropout linear regulator (LDO) capable of sourcing 3 A with only 180 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 V to 3.95 V and adjustable from 0.8 V to 5.0 V using an external resistor divider.

The combination of low-noise (4.4 μV_{RMS}), high-PSRR, and high output current capability makes the TPS7A84 ideal to power noise-sensitive components such as those found in high-speed communications, video, medical, or test and measurement applications. The high performance of the TPS7A84 limits power-supply-generated phase noise and clock jitter, making this device ideal for powering high-performance serializer and deserializer (SerDes), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. Specifically, RF amplifiers benefit from the high-performance and 5.0-V output capability of the device.

For digital loads [such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs)] requiring low-input voltage, low-output (LILO) voltage operation, the exceptional accuracy (0.75% over load and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7A84 ensure optimal system performance.

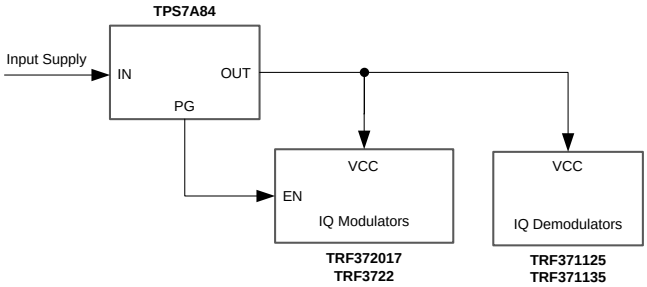
The versatility of the TPS7A84 makes the device a component of choice for many demanding applications.

Device Information(1)

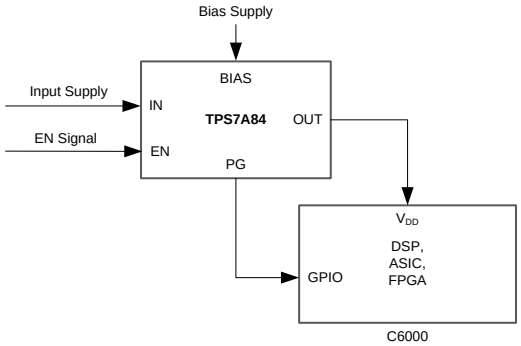
PART NUMBER	PACKAGE	BODY SIZE (nom)
TPS7A84	VQFN (20)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Powering RF Components



Powering Digital Loads



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configurations and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 7
7 Detailed Description ... 14
7.1 Overview ... 14
7.2 Functional Block Diagram ... 15
7.3 Feature Description ... 16
7.4 Device Functional Modes ... 18
8 Application and Implementation ... 19
8.1 Application Information ... 19
8.2 Typical Applications ... 30
9 Power-Supply Recommendations ... 33
10 Layout ... 33
10.1 Layout Guidelines ... 33
10.2 Layout Example ... 34
11 Device and Documentation Support ... 35
11.1 Device Support ... 35
11.2 Documentation Support ... 35
11.3 Community Resources ... 35
11.4 Trademarks ... 35
11.5 Electrostatic Discharge Caution ... 36
11.6 Glossary ... 36
12 Mechanical, Packaging, and Orderable Information ... 36

4 Revision History

Changes from Original (January 2016) to Revision A	Page
• Released to production	1

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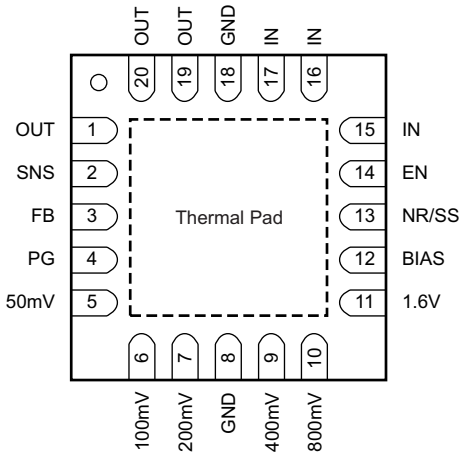
5 Pin Configurations and Functions

RGR Package
3.5-mm × 3.5-mm, 20-Pin VQFN
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
50mV	5	I	ANY-OUT voltage setting pins. Connect these pins to ground, SNS, or leave floating. Connecting these pins to ground increases the output voltage, whereas connecting these pins to SNS increases the resolution of the ANY-OUT network but decreases the range of the network; multiple pins can be simultaneously connected to GND or SNS to select the desired output voltage. Leave these pins floating (open) when not in use. See the *ANY-OUT Programmable Output Voltage* section for additional details.
100mV	6		
200mV	7		
400mV	9		
800mV	10		
1.6V	11		
BIAS	12	I	BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILO) voltage conditions (that is, V_{IN} = 1.2 V, V_{OUT} = 1 V) to reduce power dissipation across the die. The use of a BIAS voltage improves dc and ac performance for V_{IN} ≤ 2.2 V. A 10-µF capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
EN	14	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN. If enable functionality is required, V_{EN} must always be high after V_{IN} is established when a BIAS supply is used. See the *Sequencing Requirements* section for more details.
FB	3	I	Feedback pin connected to the error amplifier. Although not required, a 10-nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended to maximize ac performance. The use of a feed-forward capacitor can disrupt PG (power good) functionality. See the *ANY-OUT Programmable Output Voltage* and *Adjustable Operation* sections for more details.
GND	8, 18	—	Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection.
IN	15-17	I	Input supply voltage pin. A 47-µF or larger ceramic capacitor (25 µF or greater of capacitance) from IN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible. See the *Input and Output Capacitor Requirements* section for more details.
NR/SS	13	—	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a 10-nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance. See the *Noise-Reduction and Soft-Start Capacitor* section for more details.
OUT	1, 19, 20	O	Regulated output pin. A 47-µF or larger ceramic capacitor (25 µF or greater of capacitance) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load. See the *Input and Output Capacitor Requirements* section for more details.
PG	4	O	Active-high, power-good pin. An open-drain output indicates when the output voltage reaches 89.3% of the target. The use of a feed-forward capacitor can disrupt PG (power good) functionality. See the *Power-Good Function* section for more details.
SNS	2	I	Output voltage sense input pin. This pin connects the internal R_1 resistor to the output. Connect this pin to the load side of the output trace only if the ANY-OUT feature is used. If the ANY-OUT feature is not used, leave this pin floating. See the *ANY-OUT Programmable Output Voltage* and *Adjustable Operation* sections for more details.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	IN, BIAS, PG, EN	–0.3	7.0	V
	IN, BIAS, PG, EN (5% duty cycle, pulse duration = 200 µs)	–0.3	7.5	V
	SNS, OUT	–0.3	V_{IN} + 0.3[2]	V
	NR/SS, FB	–0.3	3.6	V
	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	–0.3	V_{OUT} + 0.3	V
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.1		6.5	V
V_{BIAS}	Bias supply voltage range[1]	3.0		6.5	V
V_{OUT}	Output voltage range[2]	0.8		5	V
V_{EN}	Enable voltage range	0		V_{IN}	V
I_{OUT}	Output current	0		3	A
C_{IN}	Input capacitor	10	47		µF
C_{OUT}	Output capacitor	47	47 || 10 || 10[3]		µF
R_{PG}	Power-good pullup resistance	10		100	kΩ
$C_{NR/SS}$	NR/SS capacitor		10		nF
C_{FF}	Feed-forward capacitor		10		nF
R_1	Top resistor value in feedback network for adjustable operation		12.1[4]		kΩ
R_2	Bottom resistor value in feedback network for adjustable operation			160[5]	kΩ
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is required when the V_{IN} supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for $V_{IN} \leq 2.2$ V.
(2) This output voltage range does not include device accuracy or accuracy of the feedback resistors.
(3) The recommended output capacitors are selected to optimize PSRR for the frequency range of 400 kHz to 700 kHz. This frequency range is a typical value for dc-dc supplies.
(4) The 12.1-kΩ resistor is selected to optimize PSRR and noise by matching the internal R_1 value.
(5) The upper limit for the R_2 resistor is to ensure accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS7A84 RGR (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.8 V[1], OUT connected to 50 Ω to GND[2], V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ without C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range[3]			1.1		6.5	V
V_{BIAS}	Bias supply voltage range[3]		V_{IN} = 1.1 V	3.0		6.5	V
V_{FB}	Feedback voltage				0.8		V
$V_{NR/SS}$	NR/SS pin voltage				0.8		V
$V_{UVLO1(IN)}$	Input supply UVLO with BIAS		V_{IN} rising with V_{BIAS} = 3.0 V		1.02	1.085	V
$V_{HYS1(IN)}$	$V_{UVLO1(IN)}$ hysteresis		V_{BIAS} = 3.0 V		320		mV
$V_{UVLO2(IN)}$	Input supply UVLO without BIAS		V_{IN} rising		1.31	1.39	V
$V_{HYS2(IN)}$	$V_{UVLO2(IN)}$ hysteresis				253		mV
$V_{UVLO(BIAS)}$	Bias supply UVLO		V_{BIAS} rising, V_{IN} = 1.1 V		2.83	2.9	V
$V_{HYS(BIAS)}$	$V_{UVLO(BIAS)}$ hysteresis		V_{IN} = 1.1 V		290		mV
V_{OUT}	Output voltage	Range	Using the ANY-OUT pins	0.8 – 1.0%		3.95 + 1.0%	V
			Using external resistors[4]	0.8 – 1.0%		5.0 + 1.0%	
		Accuracy[4][5]	0.8 V ≤ V_{OUT} ≤ 5 V, 5 mA ≤ I_{OUT} ≤ 3 A, over V_{IN}	–1.0%		1.0%	
		Accuracy with BIAS	V_{IN} = 1.1 V, 5 mA ≤ I_{OUT} ≤ 3 A, 3.0 V ≤ V_{BIAS} ≤ 6.5 V	–0.75%		0.75%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation		I_{OUT} = 5 mA, 1.4 V ≤ V_{IN} ≤ 6.5 V		0.0035		mV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		5 mA ≤ I_{OUT} ≤ 3 A, 3.0 V ≤ V_{BIAS} ≤ 6.5 V, V_{IN} = 1.1 V		0.07		mV/A
			5 mA ≤ I_{OUT} ≤ 3 A		0.08		
			5 mA ≤ I_{OUT} ≤ 3 A, V_{OUT} = 5.0 V		0.4		
V_{DO}	Dropout voltage		V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%		156	250	mV
			V_{IN} = 5.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%		220	340	
			V_{IN} = 1.1 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%		110	180	
I_{LIM}	Output current limit		V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 0.4 V	3.7	4.2	4.7	A
I_{SC}	Short-circuit current limit		R_{LOAD} = 20 mΩ		1.0		A
I_{GND}	GND pin current		V_{IN} = 6.5 V, I_{OUT} = 5 mA		2.8	4	mA
			V_{IN} = 1.4 V, I_{OUT} = 3 A		4.2	5.5	
			Shutdown, PG = open, V_{IN} = 6.5 V, V_{EN} = 0.5 V			25	µA

(1) $V_{OUT(nom)}$ is the calculated V_{OUT} target value from the ANY-OUT in a fixed configuration. In an adjustable configuration, $V_{OUT(nom)}$ is the expected V_{OUT} value set by the external feedback resistors.
(2) This 50-Ω load is disconnected when the test conditions specify an I_{OUT} value.
(3) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is required when the V_{IN} supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for V_{IN} ≤ 2.2 V.
(4) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(5) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.7 V and I_{OUT} = 3 A, because the power dissipation is higher than the maximum rating of the package.

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Electrical Characteristics (continued)

Over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.8 V(1), OUT connected to 50 Ω to GND(2), V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ without C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EN}	EN pin current	V_{IN} = 6.5 V, V_{EN} = 0 V and 6.5 V		–0.1		0.1	µA
I_{BIAS}	BIAS pin current	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, $V_{OUT(nom)}$ = 0.8 V, I_{OUT} = 3 A			2.3	3.5	mA
$V_{IL(EN)}$	EN pin high-level input voltage (enable device)			0		0.5	V
$V_{IH(EN)}$	EN pin low-level input voltage (disable device)			1.1		6.5	V
$V_{IT(PG)}$	PG pin threshold	For falling V_{OUT}		82% × V_{OUT}	88.3% × V_{OUT}	93% × V_{OUT}	V
$V_{HYS(PG)}$	PG pin hysteresis	For rising V_{OUT}			1% × V_{OUT}		V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)				0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 6.5 V				1	µA
$I_{NR/SS}$	NR/SS pin charging current	$V_{NR/SS}$ = GND, V_{IN} = 6.5 V		4.0	6.2	9.0	µA
I_{FB}	FB pin leakage current	V_{IN} = 6.5 V		–100		100	nA
PSRR	Power-supply ripple rejection	V_{IN} – V_{OUT} = 0.4 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF	f = 10 kHz, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V		42		dB
			f = 500 kHz, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V		39		
			f = 10 kHz, V_{OUT} = 5.0 V		40		
			f = 500 kHz, V_{OUT} = 5.0 V		25		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF			4.4		$µV_{RMS}$
		BW = 10 Hz to 100 kHz, V_{OUT} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF			7.7		
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		
T_J	Operating junction temperature			–40		125	°C

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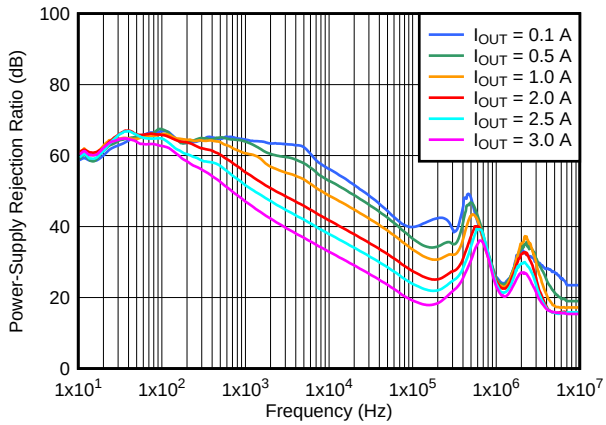
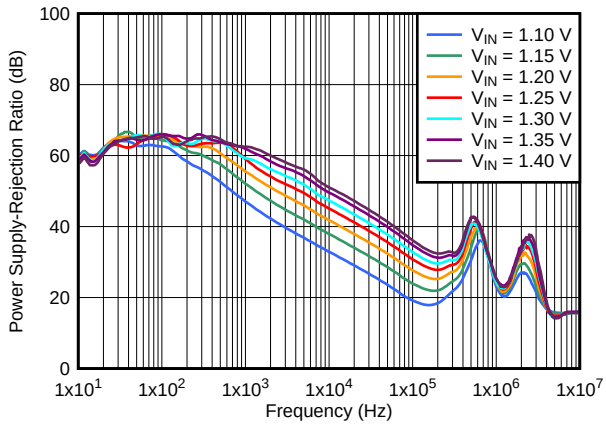
6.6 Typical Characteristics

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



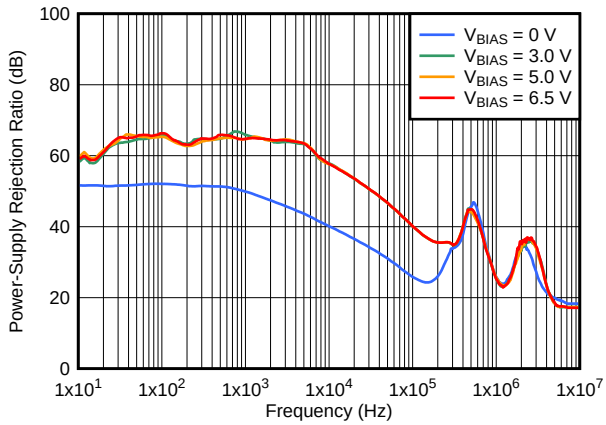
V_{IN} = 1.1 V, V_{BIAS} = 5 V,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 1. PSRR vs Frequency and I_{OUT}



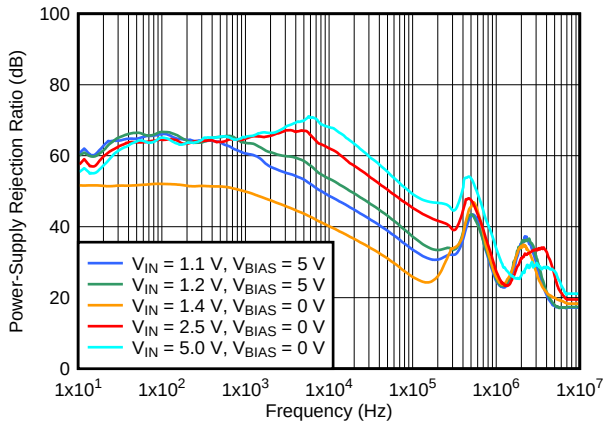
I_{OUT} = 3 A, V_{BIAS} = 5 V,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 2. PSRR vs Frequency and V_{IN} with Bias



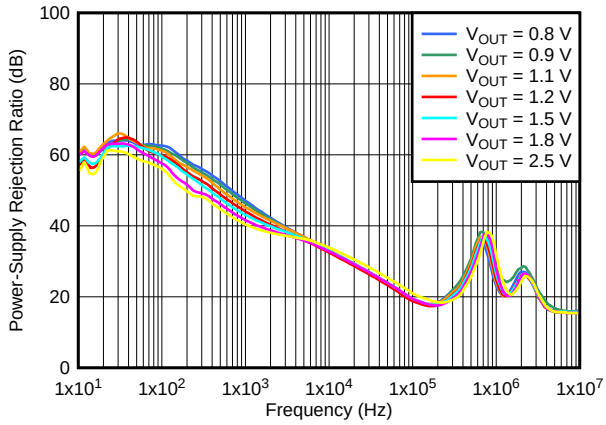
V_{IN} = 1.4 V, I_{OUT} = 1 A,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 3. PSRR vs Frequency and V_{BIAS}



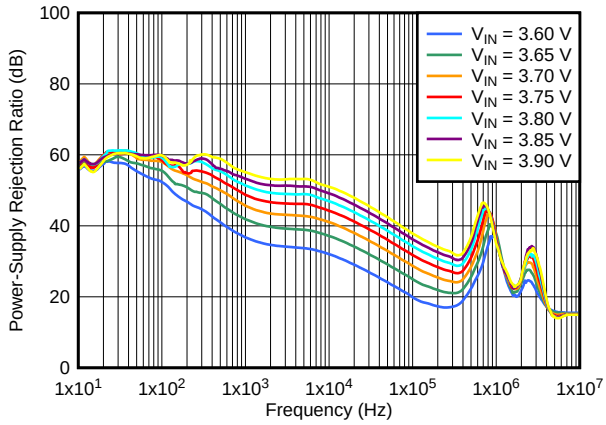
I_{OUT} = 1 A,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 4. PSRR vs Frequency and V_{IN}



V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A,
C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 5. PSRR vs Frequency and V_{OUT} with Bias

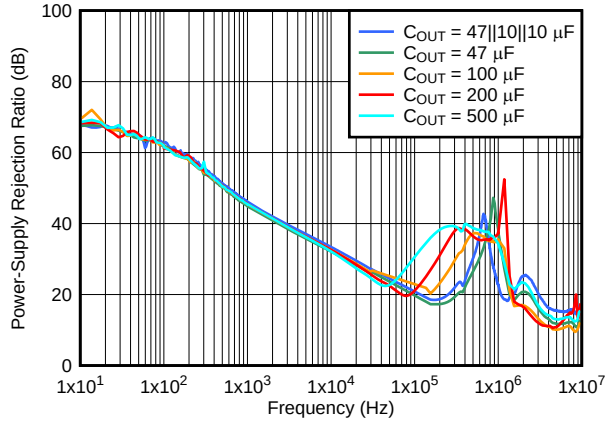


I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF,
C_{FF} = 10 nF

Figure 6. PSRR vs Frequency and V_{IN} for V_{OUT} = 3.3 V

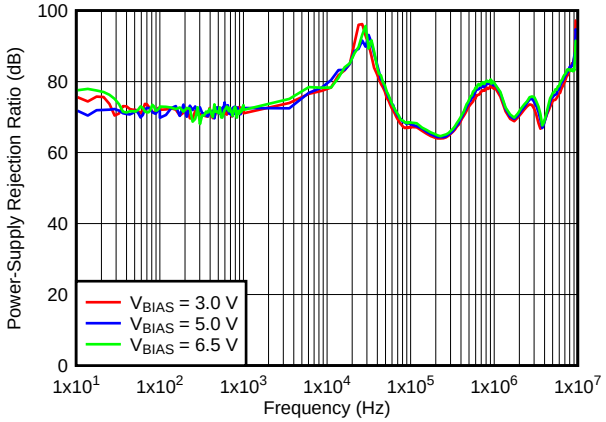
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



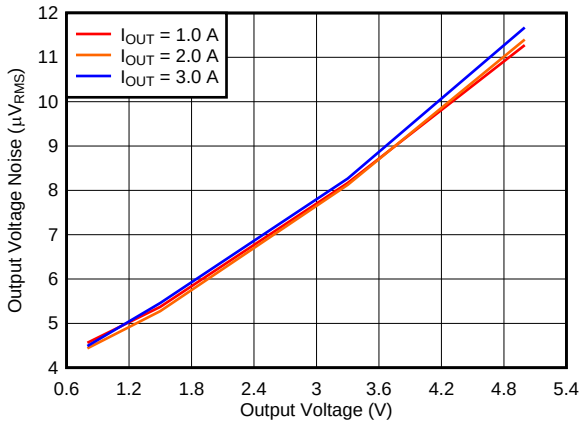
V_{IN} = V_{OUT} + 0.3 V, V_{OUT} = 1 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 7. PSRR vs Frequency and C_{OUT}



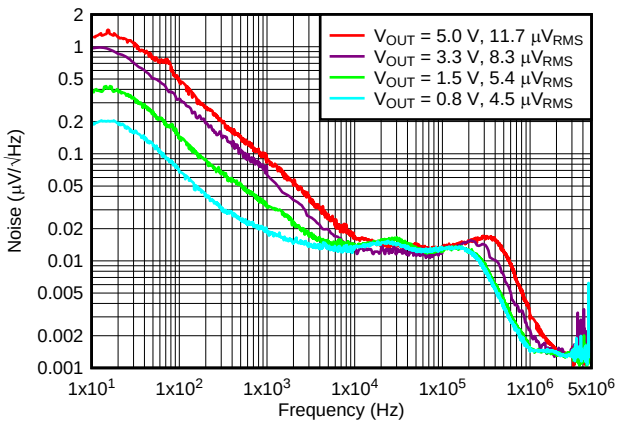
V_{IN} = V_{OUT} + 0.3 V, V_{OUT} = 1 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 8. PSRR vs Frequency and V_{BIAS}



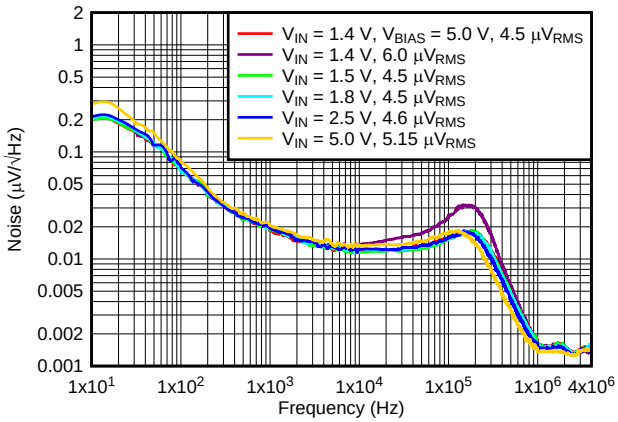
V_{IN} = V_{OUT} + 0.3 V and V_{BIAS} = 5 V for V_{OUT} ≤ 2.2 V, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 9. Output Voltage Noise vs Output Voltage



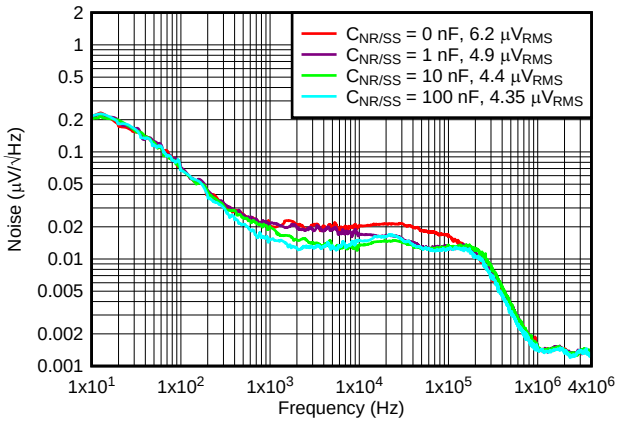
V_{IN} = V_{OUT} + 0.3 V and V_{BIAS} = 5 V for V_{OUT} ≤ 2.2 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 10. Output Noise vs Frequency and Output Voltage



I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 11. Output Noise vs Frequency and Input Voltage



V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, C_{FF} = 10 nF

Figure 12. Output Noise vs Frequency and $C_{NR/SS}$

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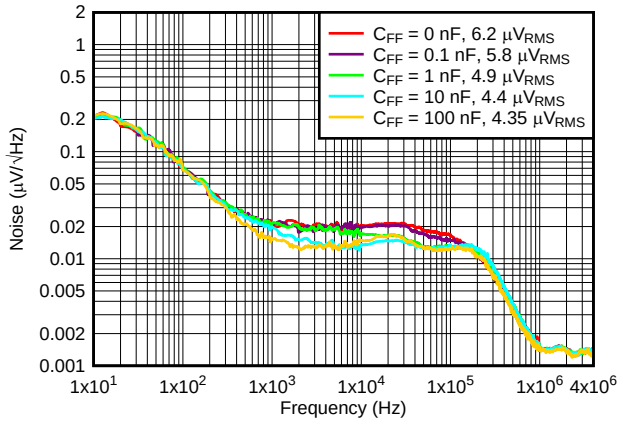
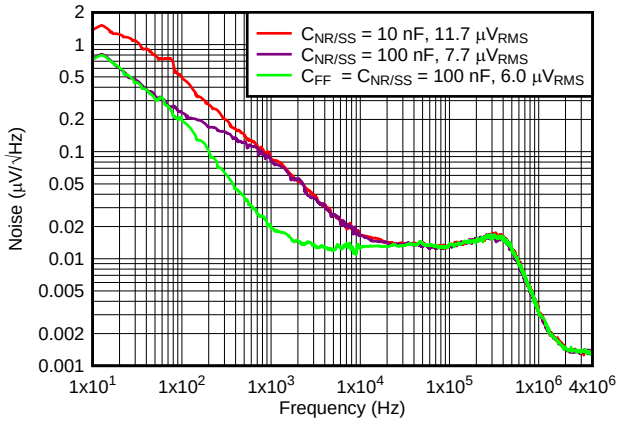
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



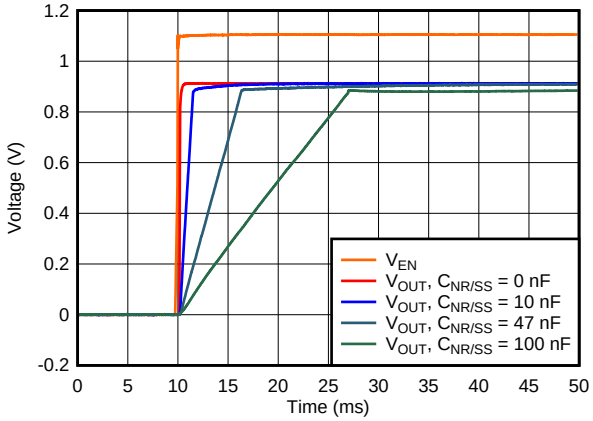
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF

Figure 13. Output Noise vs Frequency and C_{FF}



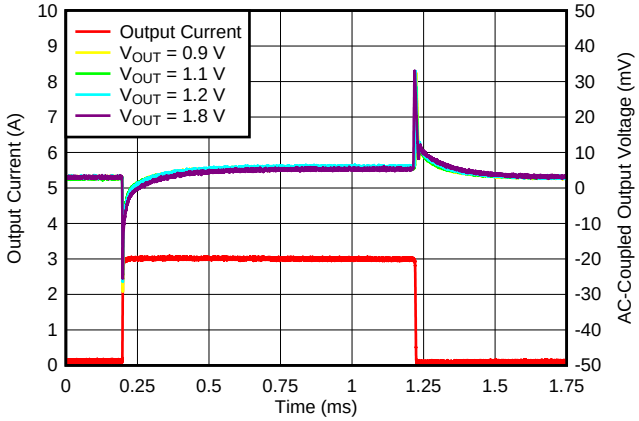
I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, C_{FF} = 10 nF

Figure 14. Output Noise at 5.0-V Output



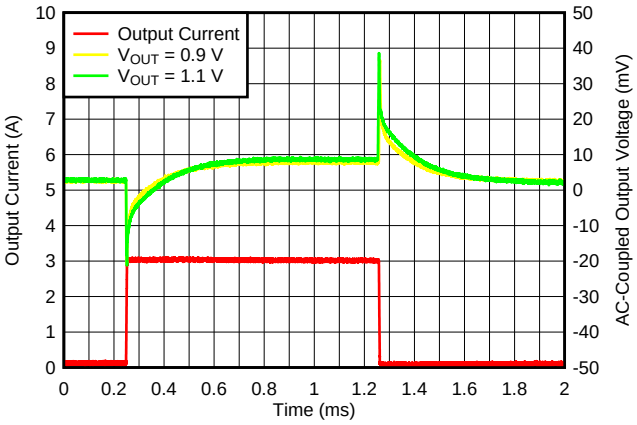
V_{IN} = 1.2 V, V_{OUT} = 0.9 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, C_{FF} = 10 nF

Figure 15. Start-Up Waveform vs Time and $C_{NR/SS}$



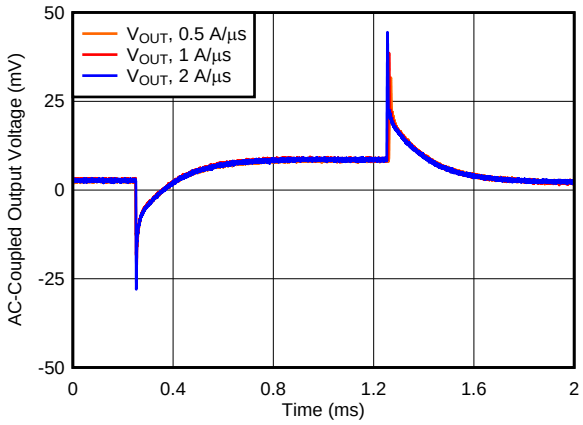
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, $I_{OUT, DC}$ = 100 mA, slew rate = 1 A/µs, $C_{NR/SS}$ = C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF

Figure 16. Load Transient vs Time and V_{OUT} with Bias



$I_{OUT, DC}$ = 100 mA, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = C_{FF} = 10 nF, slew rate = 1 A/µs

Figure 17. Load Transient vs Time and V_{OUT} without Bias

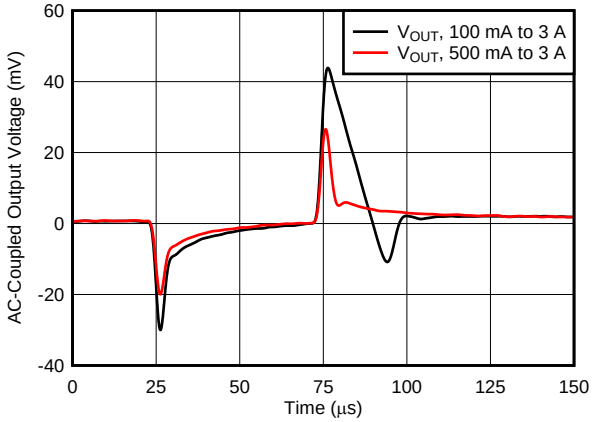


V_{OUT} = 5 V, $I_{OUT, DC}$ = 100 mA, I_{OUT} = 100 mA to 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = C_{FF} = 10 nF

Figure 18. Load Transient vs Time and Slew Rate

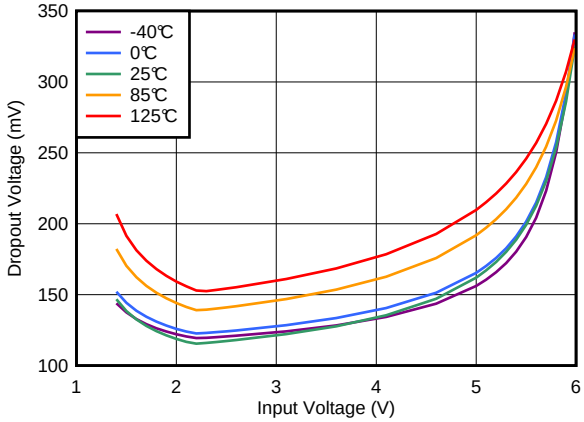
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



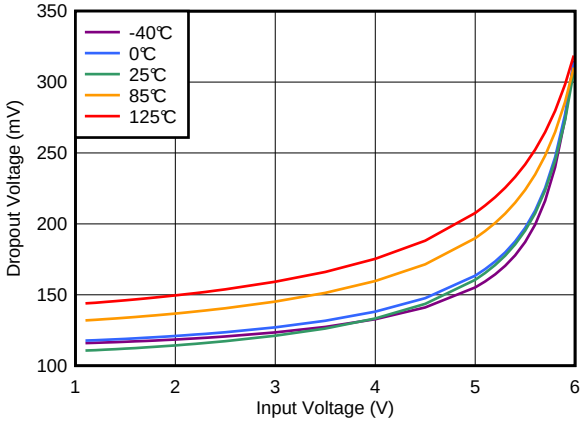
V_{IN} = 1.2 V, V_{BIAS} = 5.0 V, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = C_{FF} = 10 nF, slew rate = 1 A/µs

Figure 19. Load Transient vs Time and DC Load (V_{OUT} = 0.9 V)



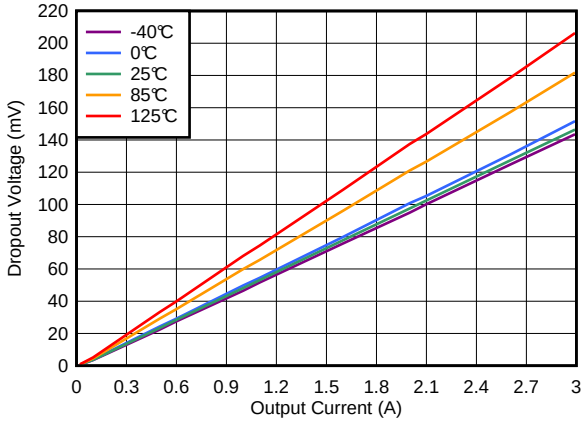
I_{OUT} = 3 A, V_{BIAS} = 0 V

Figure 20. Dropout Voltage vs Input Voltage without Bias



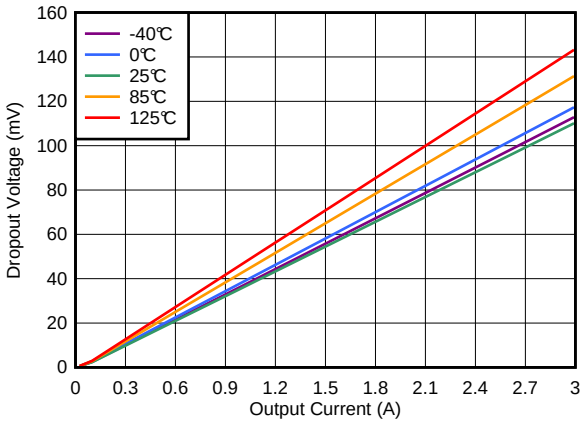
I_{OUT} = 3 A, V_{BIAS} = 6.5 V

Figure 21. Dropout Voltage vs Input Voltage with Bias



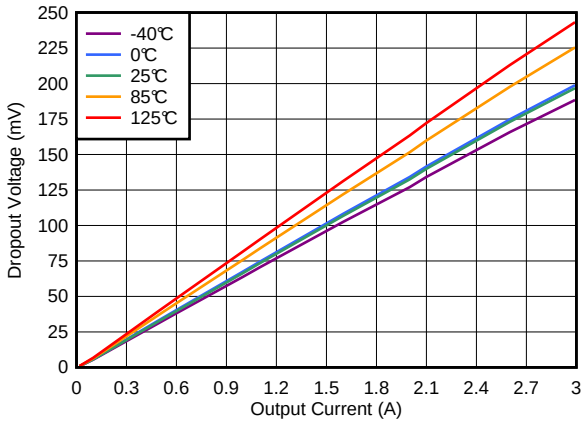
V_{IN} = 1.4 V, V_{BIAS} = 0 V

Figure 22. Dropout Voltage vs Output Current without Bias



V_{IN} = 1.1 V, V_{BIAS} = 3 V

Figure 23. Dropout Voltage vs Output Current with Bias



V_{IN} = 5.5 V

Figure 24. Dropout Voltage vs Output Current (High V_{IN})

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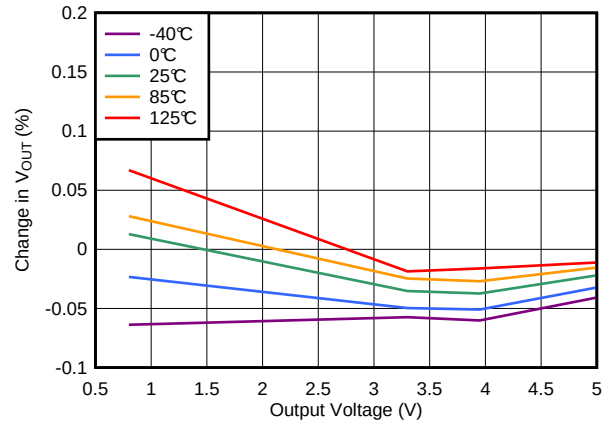
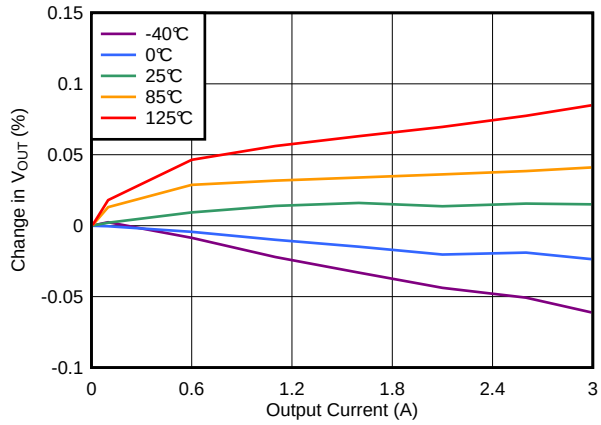
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



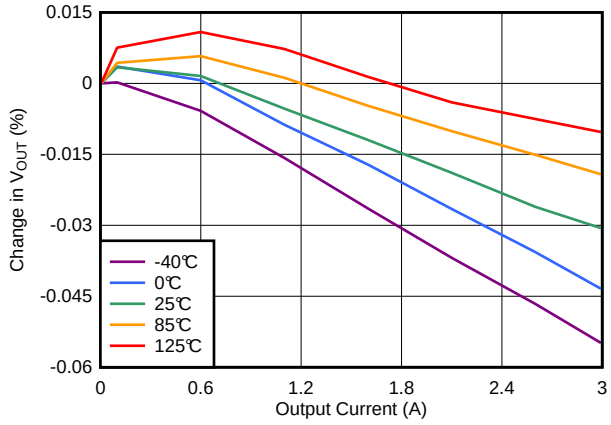
I_{OUT} = 100 mA to 3 A

Figure 25. Load Regulation vs Output Voltage



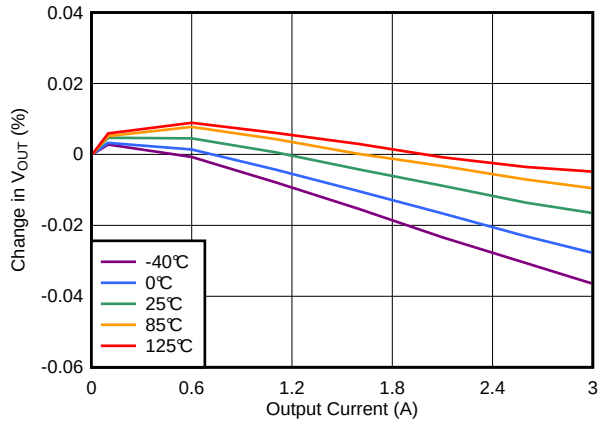
V_{IN} = 1.4 V, V_{BIAS} = 0 V

Figure 26. Load Regulation with Bias



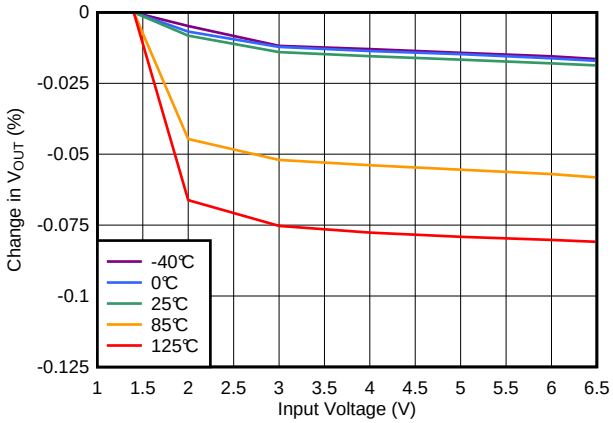
V_{IN} = 3.8 V

Figure 27. Load Regulation (3.3-V Output)



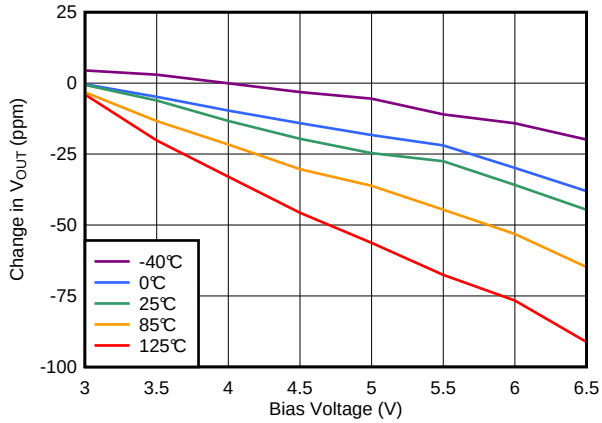
V_{IN} = 5.5 V

Figure 28. Load Regulation (5-V Output)



V_{OUT} = 0.8 V, V_{BIAS} = 0 V, I_{OUT} = 5 mA

Figure 29. Line Regulation without Bias

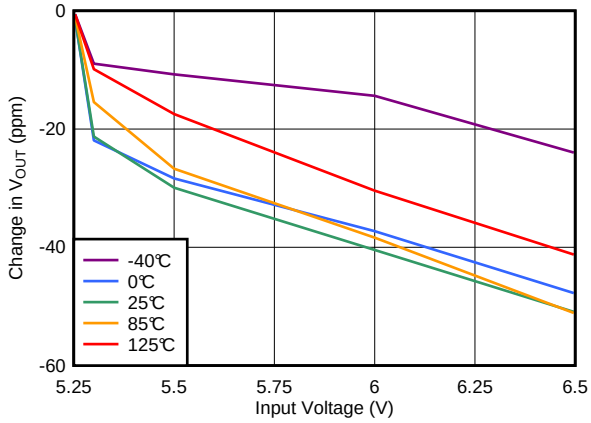


V_{OUT} = 0.8 V, V_{IN} = 1.1 V, I_{OUT} = 5 mA

Figure 30. Line Regulation without Bias

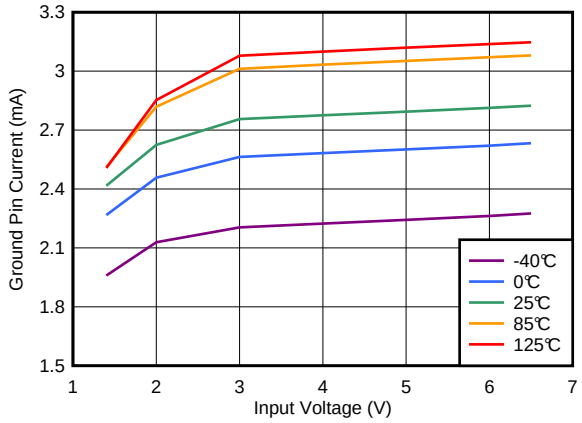
Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



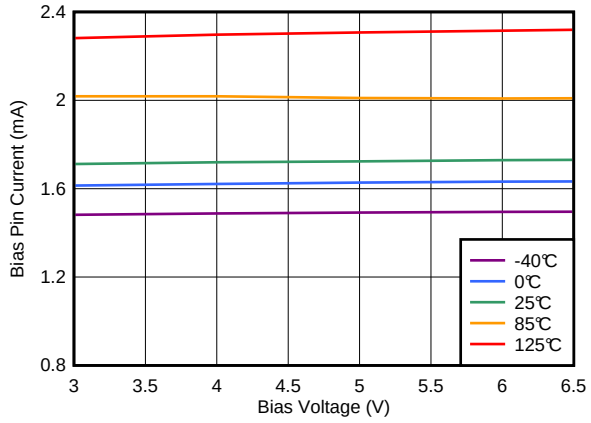
I_{OUT} = 5 mA

Figure 31. Line Regulation (5-V Output)



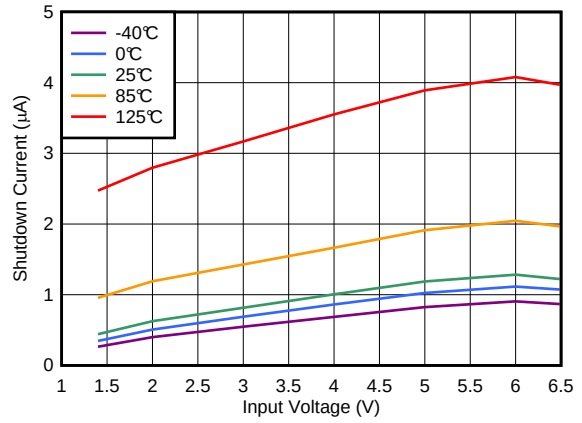
V_{BIAS} = 0 V, I_{OUT} = 5 mA

Figure 32. Quiescent Current vs Input Voltage



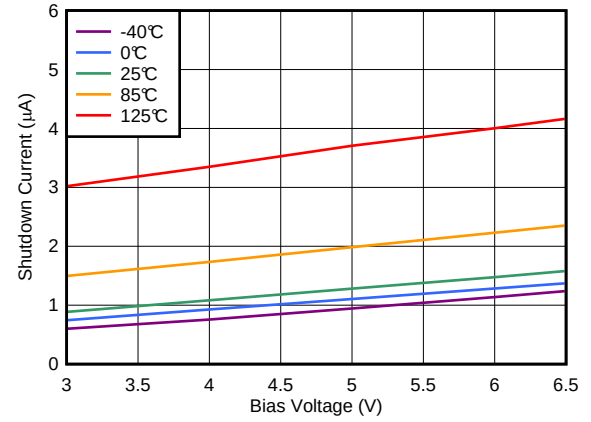
V_{IN} = 1.1 V, I_{OUT} = 5 mA

Figure 33. Quiescent Current vs Bias Voltage



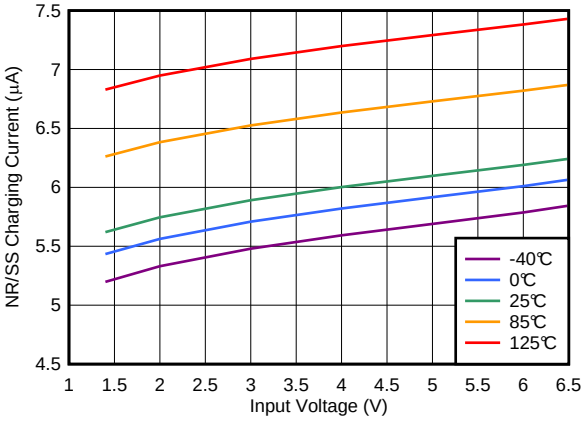
V_{BIAS} = 0 V

Figure 34. Shutdown Current vs Input Voltage



V_{IN} = 1.1 V

Figure 35. Shutdown Current vs Bias Voltage



V_{BIAS} = 0 V

Figure 36. $I_{NR/SS}$ Current vs Input Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)

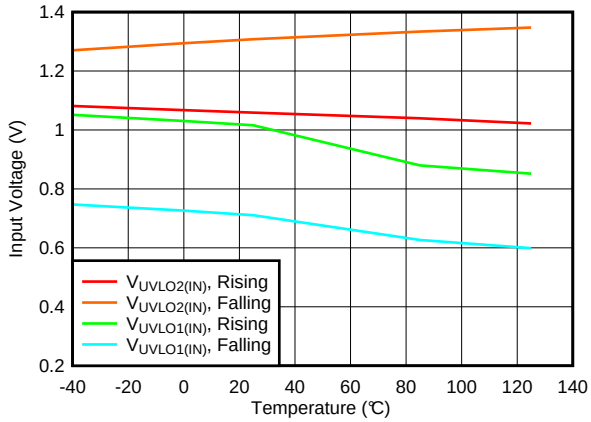

Figure 37. V_{IN} UVLO vs Temperature

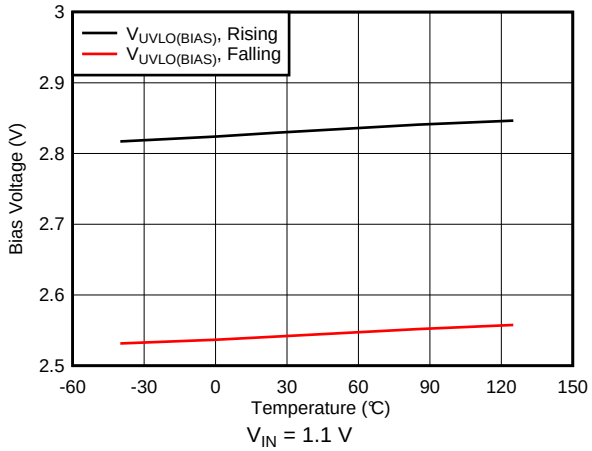

Figure 38. V_{BIAS} UVLO vs Temperature

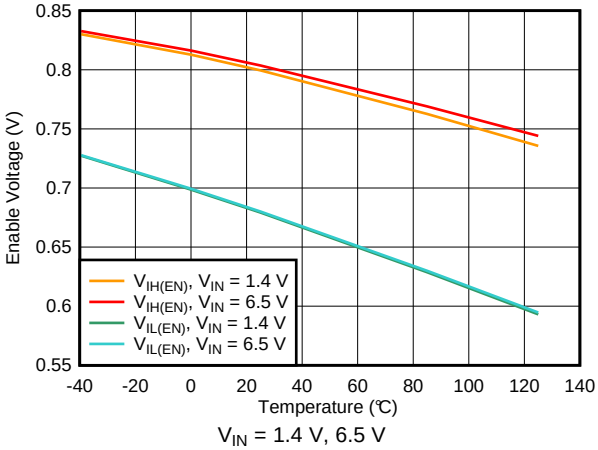

Figure 39. Enable Threshold vs Temperature

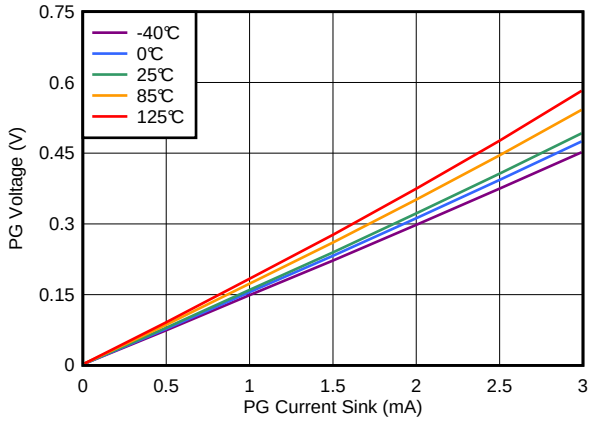

Figure 40. PG Voltage vs PG Current Sink

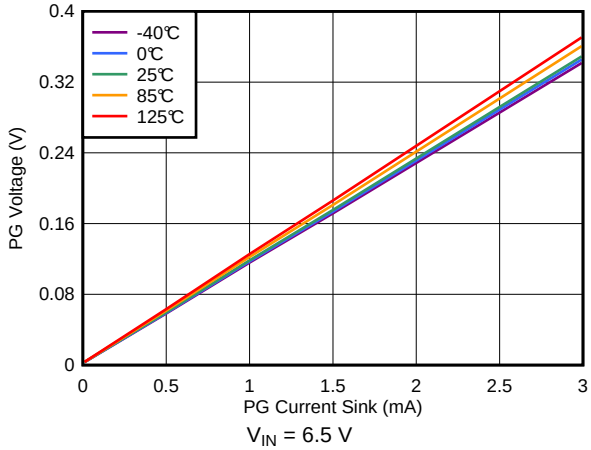

Figure 41. PG Voltage vs PG Current Sink

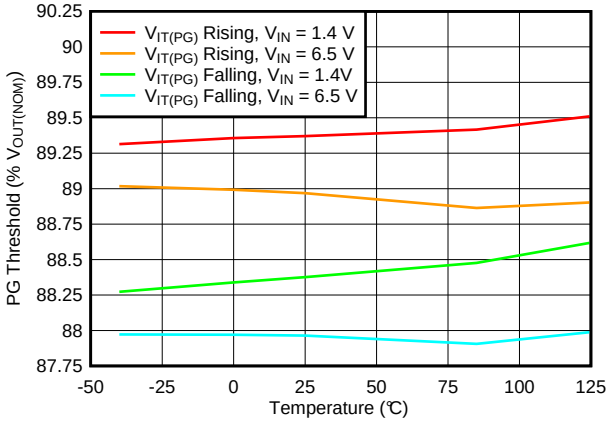

Figure 42. PG Threshold vs Temperature

7 Detailed Description

7.1 Overview

The TPS7A84 is a high-current (3 A), low-noise (4.4 μV_{RMS}), high accuracy (1%) low-dropout linear voltage regulator (LDO). These features make the device a robust solution to solve many challenging problems in generating a clean, accurate power supply.

The TPS7A84 has several features that make the device useful in a variety of applications. As detailed in the *Functional Block Diagram* section, these features include:

- Low-noise, high-PSRR output
- ANY-OUT resistor network
- Optional bias rail
- Power-good output
- Programmable soft-start
- Foldback current limit
- Enable circuitry
- Active discharge
- Thermal protection

Overall, these features make the TPS7A84 the component of choice because of its versatility and ability to generate a supply for most applications.

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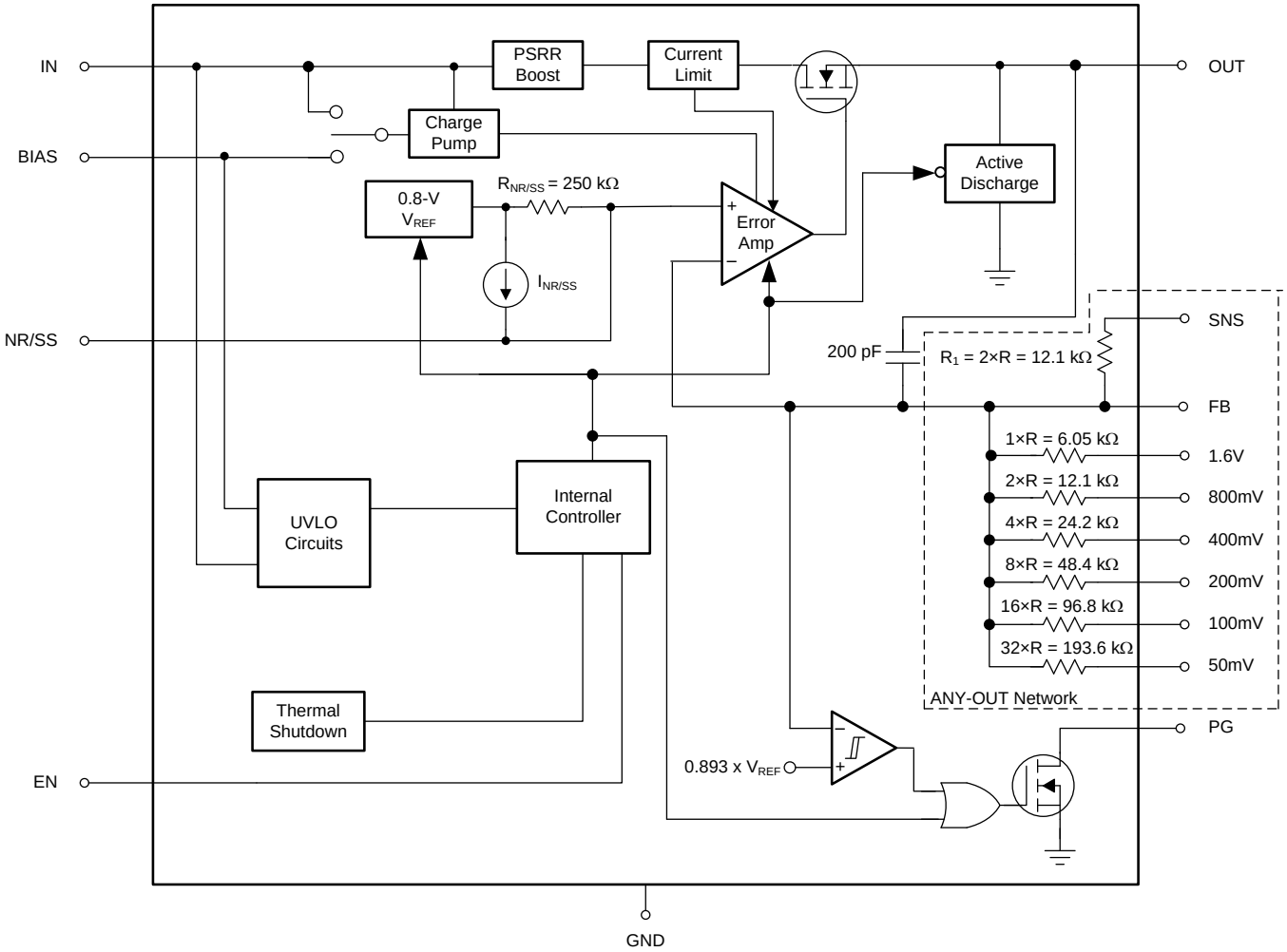
7.2 Functional Block Diagram



NOTE: For the ANY-OUT network, the ratios between the values are highly accurate as a result of matching, but the actual resistance can vary significantly from the numbers listed.

7.3 Feature Description

7.3.1 Low-Noise, High-PSRR Output

The TPS7A84 includes a low-noise reference and error amplifier ensuring minimal noise during operation. The NR/SS capacitor ($C_{NR/SS}$) and feed-forward capacitor (C_{FF}) are the easiest way to reduce device noise. $C_{NR/SS}$ filters the noise from the reference and C_{FF} filters the noise from the error amplifier. The noise contribution from the charge pump is minimal. The overall noise of the system at low output voltages can be reduced by using a bias rail because this rail provides more headroom for internal circuitry.

The high power-supply rejection ratio (PSRR) of the TPS7A84 ensures minimal coupling of input supply noise to the output. The PSRR performance is primarily results from a high-bandwidth, high-gain error amplifier and an innovative circuit to boost the PSRR between 200 kHz and 1 MHz.

The combination of a low noise-floor and high PSRR ensure that the device provides a clean supply to the application; see the *Optimizing Noise and PSRR* section for more information on optimizing the noise and PSRR performance.

7.3.2 Integrated Resistance Network (ANY-OUT)

An internal feedback resistance network is provided, allowing the TPS7A84 output voltage to be programmed easily between 0.8 V to 3.95 V with a 50-mV step by tying the ANY-OUT pins to ground. Tying the ANY-OUT pins to SNS increases the resolution but limits the range of the output voltage because the effective value of R_1 is decreased. Use the ANY-OUT network for excellent accuracy across output voltage and temperature; see the *Application and Implementation* section for more details.

7.3.3 Bias Rail

The device features a bias rail to enable low-input voltage, low-output (LILO) voltage operation by providing power to the internal circuitry of the device. The bias rail is required for operation with V_{IN} < 1.4 V, and is recommended for V_{IN} ≤ 2.2 V to improve dc and ac performance. An internal power-MUX supplies the greater of either the input voltage or the bias voltage to an internal charge pump to power the internal circuitry. Using the bias rail does constitute some sequencing requirements that are detailed in the *Sequencing Requirements* section.

7.3.4 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage ($V_{IT(PG)}$ + $V_{HYS(PG)}$, typically 89.3%), the PG pin open-drain output engages and pulls the PG pin close to GND. When the feedback voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than $V_{HYS(PG)}$ (typically 91.3%), the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended. Using an external voltage detector device such as the TPS3702 is also recommended in applications where more accurate voltage monitoring or overvoltage monitoring is required.

The use of a feed-forward capacitor (C_{FF}) can cause glitches on start-up, and the power-good circuit may not function normally below the minimum input supply range. For more details on the use of the power-good circuitry, see the *Power-Good Operation* section.

7.3.5 Programmable Soft-Start

Soft-start refers to the ramp-up time of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltage. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp time during turn-on. The start-up ramp is monotonic and linear in most conditions, however there is a small set of conditions that cause a small initial jump in output voltage. See the *Application and Implementation* section on implementing a soft-start.

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Feature Description (continued)

7.3.6 Internal Current Limit (I_{LIM})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

The foldback current limit crosses 0 A when V_{OUT} < 0 V and prevents the device from turning on into a negatively-biased output. See the *Negative Biased Output* section on additional ways to ensure start-up when the TPS7A84 output is pulled below ground.

7.3.7 Enable

The enable pin for the TPS7A84 is active high. The output of the TPS7A84 is turned on when the enable pin voltage is greater than its rising voltage threshold (1.1 V, max), and the output of the TPS7A84 is turned off when the enable pin voltage is less than its falling voltage threshold (0.5 V, min). A voltage less than 0.5 V on the enable pin disables all internal circuits. At the next turn-on this voltage ensures a normal start-up waveform with in-rush control, provided there is enough time to discharge the output capacitance.

When the enable functionality is not desired, EN must be tied to V_{IN}. However, when the enable functionality is desired, the enable voltage must come after V_{IN} is above $V_{UVLO1(IN)}$ when a BIAS rail is used. See the *Application and Implementation* section for further details.

7.3.8 Active Discharge Circuit

The TPS7A84 has an internal pulldown MOSFET that connects a resistance of several hundred ohms to ground when the device is disabled to actively discharge the output voltage when the device is disabled.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.3.9 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit monitors the input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent the device from turning on before V_{IN} and V_{BIAS} rise above the lockout voltage. The UVLO circuit also disables the output of the device when V_{IN} or V_{BIAS} fall below the lockout voltage. The UVLO circuit responds quickly to glitches on V_{IN} or V_{BIAS} and attempts to disable the output of the device if either of these rails collapse. As a result of the fast response time of the input supply UVLO circuit, fast and short line transients well below the input supply UVLO falling threshold can cause momentary glitches when asserted or when recovered from the transient. See the *Application and Implementation* section for more details.

7.3.10 Thermal Protection

The TPS7A84 contains a thermal shutdown protection circuit to disable the device when thermal junction temperature (T_J) of the main pass-FET exceeds 160°C (typical). Thermal shutdown hysteresis assures that the LDO resets again (turns on) when the temperature falls to 140°C (typical). The thermal time-constant of the semiconductor die is fairly short, and thus the device cycles on and off when thermal shutdown is reached until the power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125°C. Operation above 125°C can cause the device to exceed its operational specifications. Although the internal protection circuitry of the TPS7A84 is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A84 into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

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7.4 Device Functional Modes

7.4.1 Operation with 1.1 V ≤ V_{IN} < 1.4 V

The TPS7A84 requires a bias voltage on the BIAS pin greater than or equal to 3.0 V if the high-current input supply voltage is between 1.1 V to 1.4 V. The bias voltage pin consumes 2.3 mA, nominally.

7.4.2 Operation with 1.4 V ≤ V_{IN} ≤ 6.5 V

If the input voltage is equal to or exceeds 1.4 V, no BIAS voltage is required. The TPS7A84 is powered from either the input supply or the BIAS supply, whichever is greater. For higher performance, a BIAS rail is recommended for V_{IN} ≤ 2.2 V.

7.4.3 Shutdown

Shutting down the device reduces the ground current of the device to a maximum of 25 µA.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A84 is a linear voltage regulator with an input range of 1.1 V to 6.5 V and an output voltage range of 0.8 V to 5.0 V with a 1% accuracy and a 3-A maximum output current. The TPS7A84 has an integrated charge pump for ease of use and an external bias rail to allow for the lowest dropout across the entire output voltage range.

8.1.1 Recommended Capacitor Types

The TPS7A84 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin 13). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (that is, V_{IN} = 5.5 V to V_{OUT} = 5.0 V) the derating can be greater than 50% and must be taken into consideration.

8.1.2 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A84 is designed and characterized for operation with ceramic capacitors of 47 µF or greater (22 µF or greater of capacitance) at the output and 10 µF or greater (5 µF or greater of capacitance) at the input. Using at least a 47-µF capacitor is highly recommended at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitics. If the trace inductance from the input supply to the TPS7A84 is high, a fast current transient can cause V_{IN} to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by additional input capacitors to dampen the ringing and to keep it below the device absolute maximum ratings.

A combination of multiple output capacitors boosts the high-frequency PSRR, as illustrated in several of the PSRR curves. The combination of one 0805-sized, 47-µF ceramic capacitor in parallel with two 0805-sized, 10-µF ceramic capacitors with a sufficient voltage rating in conjunction with the PSRR boost circuit optimizes PSRR for the frequency range of 400 kHz to 700 kHz, a typical range for dc-dc supply switching frequency. This 47-µF || 10-µF || 10-µF combination also ensures that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Many 0805-sized, 47-µF ceramic capacitors have a voltage derating of approximately 60% to 80% at 5.0 V, so the addition of the two 10-µF capacitors ensures that the capacitance is at or above 22 µF.

8.1.3 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The TPS7A84 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$).The use of an external $C_{NR/SS}$ is highly recommended, especially to minimize in-rush current into the output capacitors. This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak in-rush current during start-up, minimizing start-up transients to the input power bus.

Application Information (continued)

To achieve a monotonic start-up, the TPS7A84 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage approaches the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference ($V_{NR/SS}$). Soft-start ramp time can be calculated with Equation 1:

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (1)$$

Note that $I_{NR/SS}$ is provided in the *Electrical Characteristics* table and has a typical value of 6.2 µA.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and the cutoff frequency can be calculated with Equation 2. The typical value of R_{NR} is 250 kΩ. Increasing the $C_{NR/SS}$ capacitor has a greater affect because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, a 10-nF to 1-µF $C_{NR/SS}$ is recommended.

$$f_{cutoff} = 1/ (2 \times \pi \times R_{NR} \times C_{NR/SS}) \quad (2)$$

8.1.4 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10-nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled. For a detailed description, see application report *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, SBVA042.

8.1.5 Optimizing Noise and PSRR

The ultra-low noise floor and PSRR of the device can be improved by careful selection of:

- $C_{NR/SS}$ for the low-frequency range
- C_{FF} in the mid-band frequency range
- C_{OUT} for the high-frequency range
- V_{IN} - V_{OUT} for all frequencies, and
- V_{BIAS} at lower input voltages

A larger noise-reduction capacitor improves low-frequency PSRR by filtering any noise coupling from the input into the reference. The feed-forward capacitor can be optimized to place a pole-zero pair near the edge of the loop bandwidth and push out the loop bandwidth, thus improving mid-band PSRR. Larger output capacitors and various output capacitors can be used to improve high-frequency PSRR.

A higher input voltage improves the PSRR by giving the device more headroom to respond to noise on the input; see Figure 2. A bias rail also improves the PSRR at lower input voltages because greater headroom is provided for the internal circuits.

The noise-reduction capacitor filters out low-frequency noise from the reference and the feed-forward capacitor reduces output voltage noise by filtering out the mid-band frequency noise. However, a large feed-forward capacitor can create some new issues that are discussed in application report *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, SBVA042.

Note that a large output capacitor reduces high-frequency output voltage noise. Additionally, a bias rail or higher input voltage improves the noise because greater headroom is provided for the internal circuits.

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Application Information (continued)

Table 1 lists the output voltage noise for the 10-Hz to 100-kHz band at a 5.0-V output for a variety of conditions with an input voltage of 5.4 V, an R_1 of 12.1 kΩ, and a load current of 3 A. The 5.0-V output is chosen because this output is the worst-case condition for output voltage noise.

Table 1. Output Noise Voltage at a 5.0-V Output

OUTPUT VOLTAGE NOISE (μV_{RMS})	$C_{NR/SS}$ (nF)	C_{FF} (nF)	C_{OUT} (µF)
11.7	10	10	47 || 10 || 10
7.7	100	10	47 || 10 || 10
6	100	100	47 || 10 || 10
7.4	100	10	1000
5.8	100	100	1000

8.1.6 Soft-Start and In-Rush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

In-rush current is defined as the current into the LDO at the IN pin during start-up. In-rush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, this soft-start current can be estimated by Equation 3:

$$I_{OUT(t)} = \left(\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right) + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t)$ / dt is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance (3)

8.1.7 ANY-OUT Programmable Output Voltage

The TPS7A84 can use either external resistors or the internally-matched ANY-OUT feedback resistor network to set output voltage. The ANY-OUT resistors are accessible via pin 2 and pins 5 to 11 and are used to program the regulated output voltage. Each pin is can be connected to ground (active) or left open (floating), or connected to SNS. ANY-OUT programming is set by Equation 4 as the sum of the internal reference voltage ($V_{NR/SS}$ = 0.8 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 50mV (pin 5), 100mV (pin 6), 200mV (pin 7), 400mV (pin 9), 800mV (pin 10), or 1.6V (pin 11). Table 2 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{FB}.

$$V_{OUT} = V_{REF} + (\Sigma \text{ ANY-OUT Pins to Ground}) \quad (4)$$

Table 2. ANY-OUT Programmable Output Voltage

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 5 (50mV)	50 mV
Pin 6 (100mV)	100 mV
Pin 7 (200mV)	200 mV
Pin 9 (400mV)	400 mV
Pin 10 (800mV)	800 mV
Pin 11 (1.6V)	1.6 V

Table 3 provides a full list of target output voltages and corresponding pin settings when the ANY-OUT pins are only tied to ground or left floating. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.8 V to 3.95 V in 50-mV steps when tying these pins to ground. There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected using 0-Ω resistors (or left open), or hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage. As with the adjustable operation, the output voltage is set according to Equation 5 except that R_1 and R_2 are internally integrated and matched for higher accuracy. Tying any of the ANY-OUT pins to SNS can increase the resolution of the internal feedback network by lowering the value of R_1. See the *Increasing ANY-OUT Resolution for LILO Conditions* section for additional information.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1 / R_2) \quad (5)$$

NOTE

For output voltages greater than 3.95 V, use a traditional adjustable configuration (see the *Adjustable Operation* section).

Table 3. User-Configurable Output Voltage Settings

$V_{OUT(NOM)}$ (V)	50mV	100mV	200mV	400mV	800mV	1.6V	$V_{OUT(NOM)}$ (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.80	Open	Open	Open	Open	Open	Open	2.40	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.90	Open	GND	Open	Open	Open	Open	2.50	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND
1.00	Open	Open	GND	Open	Open	Open	2.60	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.10	Open	GND	GND	Open	Open	Open	2.70	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.20	Open	Open	Open	GND	Open	Open	2.80	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.30	Open	GND	Open	GND	Open	Open	2.90	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.40	Open	Open	GND	GND	Open	Open	3.00	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.50	Open	GND	GND	GND	Open	Open	3.10	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.60	Open	Open	Open	Open	GND	Open	3.20	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.70	Open	GND	Open	Open	GND	Open	3.30	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.80	Open	Open	GND	Open	GND	Open	3.40	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.90	Open	GND	GND	Open	GND	Open	3.50	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2.00	Open	Open	Open	GND	GND	Open	3.60	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.10	Open	GND	Open	GND	GND	Open	3.70	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.20	Open	Open	GND	GND	GND	Open	3.80	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.30	Open	GND	GND	GND	GND	Open	3.90	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

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8.1.8 ANY-OUT Operation

Considering the use of the ANY-OUT internal network (where the unit resistance of 1R is equal to 6.05 kΩ) the output voltage is set by grounding the appropriate control pins, as shown in Figure 43. When grounded, all control pins add a specific voltage on top of the internal reference voltage ($V_{NR/SS}$ = 0.8 V). The output voltage can be calculated by Equation 6 and Equation 7. Figure 43 and Figure 44 show a 0.9-V output voltage, respectively, that provide an example of the circuit usage with and without bias voltage.

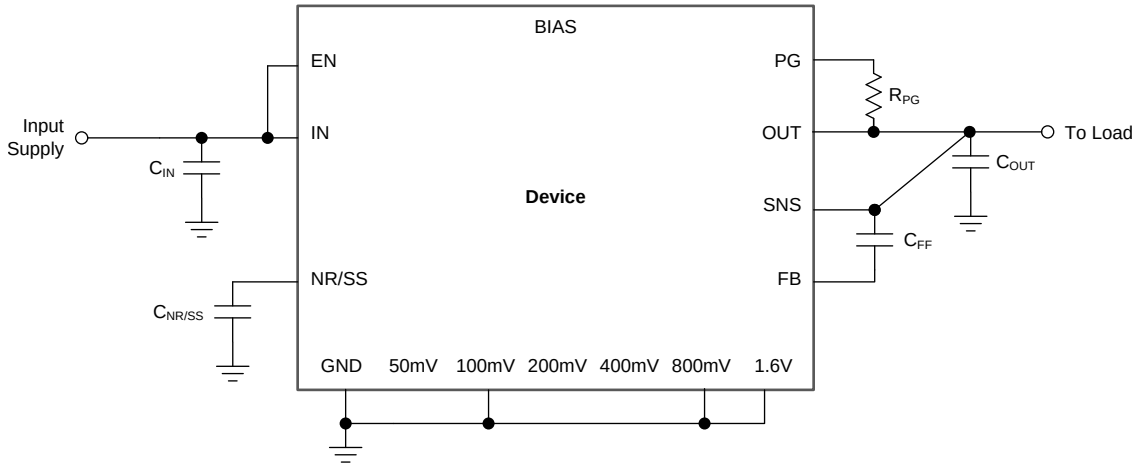

Figure 43. ANY-OUT Configuration Circuit (3.3-V Output, No External Bias)

$$V_{OUT(nom)} = V_{NR/SS} + 1.6\ V + 0.8\ V + 0.1\ V = 0.8\ V + 1.6\ V + 0.8\ V + 0.1\ V = 3.3\ V \quad (6)$$

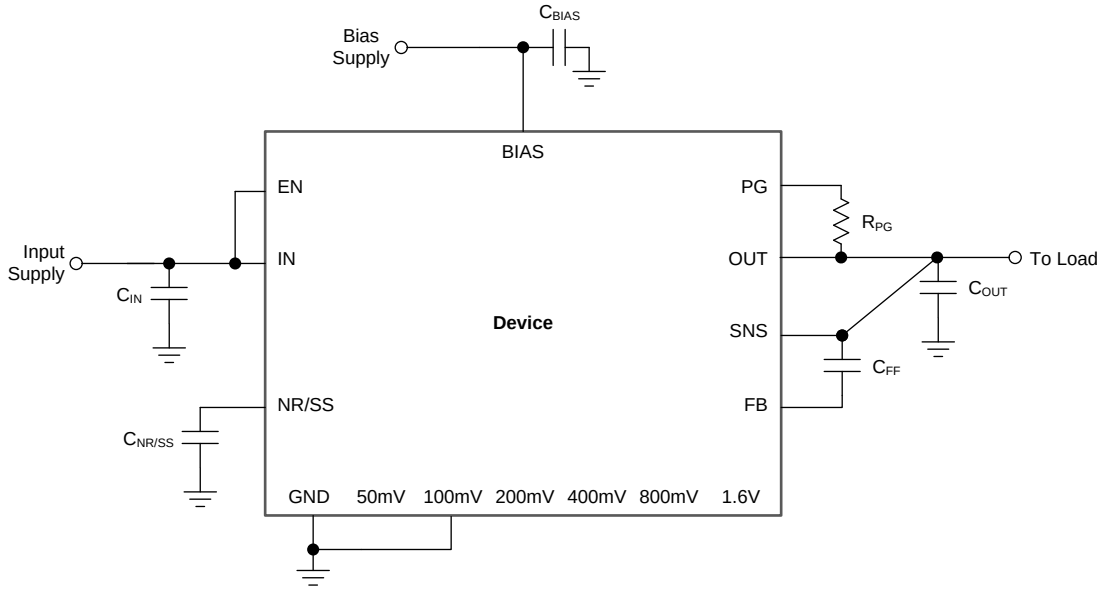

Figure 44. ANY-OUT Configuration Circuit (0.9-V Output with Bias)

$$V_{OUT(nom)} = V_{NR/SS} + 0.1\ V = 0.8\ V + 0.1\ V = 0.9\ V \quad (7)$$

8.1.9 Increasing ANY-OUT Resolution for LILO Conditions

As with the adjustable operation, the output voltage is set according to Equation 5, except that R_1 and R_2 are internally integrated and matched for higher accuracy. Tying any of the ANY-OUT pins to SNS can increase the resolution of the internal feedback network by lowering the value of R_1. One of the more useful pin combinations is to tie the 800mV pin to SNS, which reduces the resolution by 50% to 25 mV but limits the range. The new ANY-OUT ranges are 0.8 V to 1.175 V and 1.6 V to 1.975 V. The new additive output voltage levels are listed in Table 4.

Table 4. ANY-OUT Programmable Output Voltage with 800mV Tied to SNS

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 5 (50mV)	25 mV
Pin 6 (100mV)	50 mV
Pin 7 (200mV)	100 mV
Pin 9 (400mV)	200 mV
Pin 11 (1.6V)	800 V

8.1.10 Adjustable Operation

The TPS7A84 can be used either with the internal ANY-OUT network or by using external resistors. Using the ANY-OUT network allows the TPS7A84 to be programmed from 0.8 V to 3.95 V. To extend this output voltage range to 5.0 V, external resistors must be used. This configuration is referred to as the adjustable configuration of the TPS7A84 throughout this document. Regardless whether the internal resistor network or whether external resistors are used, the output voltage is set by two resistors, as shown in Figure 45. Using the internal resistor ensures a 1% accuracy and minimizes the number of external components.

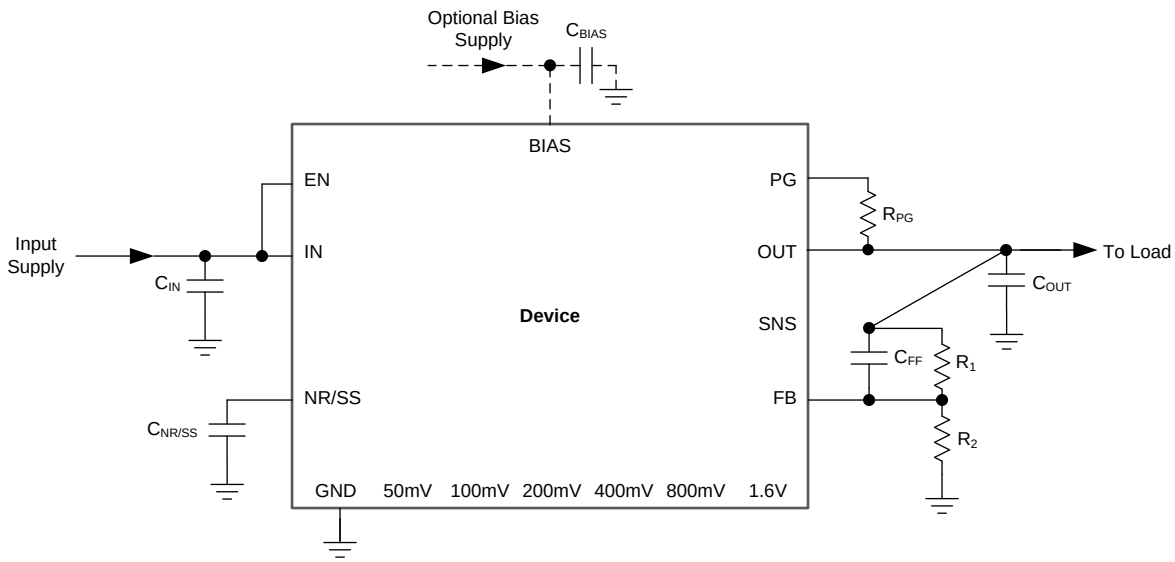

Figure 45. Adjustable Operation

R_1 and R_2 can be calculated for any output voltage range using Equation 8. This resistive network must provide a current equal to or greater than 5 µA for dc accuracy. Using an R_1 of 12.1 kΩ is recommended to optimize the noise and PSRR.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1 / R_2) \quad (8)$$

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Table 5 shows the resistor combinations required to achieve several common rails using standard 1%-tolerance resistors.

Table 5. Recommended Feedback-Resistor Values

$V_{OUT(NOM)}$ (V)	FEEDBACK RESISTOR VALUES	
	R_1 (kΩ)	R_2 (kΩ)
0.9	12.1	97.6
1.00	12.1	48.7
1.10	12.1	32.4
1.20	12.1	24.3
1.50	12.1	13.7
1.80	12.1	9.76
1.90	12.1	8.87
2.50	12.1	5.76
2.85	12.1	4.75
3.00	12.1	4.42
3.30	12.1	3.83
3.60	12.1	3.48
4.5	12.1	2.61
5.00	12.1	2.32

8.1.11 Sequencing Requirements

Supply and enable sequencing is only required when the bias rail is present. The start-up is always monotonic, independent of the sequencing requirements. Under these conditions the following requirements apply:

- V_{BIAS} and V_{IN} can be sequenced in any order, as long as V_{EN} is tied to V_{IN} or established after V_{IN}, as shown in Figure 46

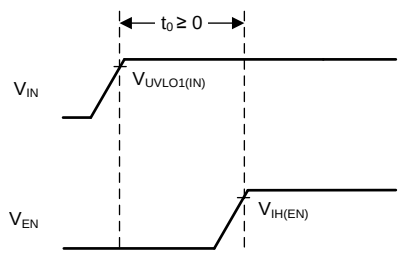

Figure 46. Sequencing Diagram

Two typical application circuits for implementing the sequencing requirements are detailed in the *Sequencing with a Power-Good DC-DC Converter Pin* and *Sequencing with a Microcontroller (MCU)* sections.

8.1.11.1 Sequencing with a Power-Good DC-DC Converter Pin

When a dc-dc converter is used to power the device and the PG of the dc-dc converter is used to enable the device, pull PGup to V_{IN}, as shown in Figure 47.

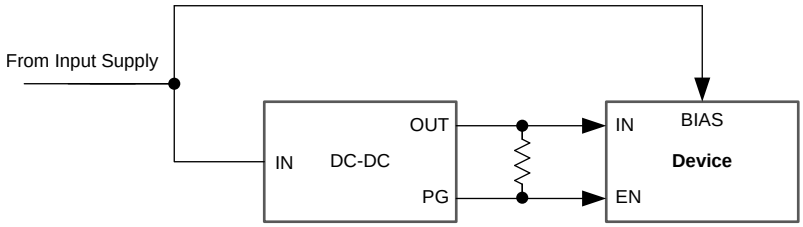

Figure 47. Sequencing with a DC-DC Converter and PG

8.1.11.2 Sequencing with a Microcontroller (MCU)

If a push-pull output stage is used to provide the enable signal to the device and the enable signal can possibly come before V_{IN} when a bias is present (such as with an MCU), convert the enable signal to an open-drain signal as shown in Figure 48. Using an open-drain signal ensures that if the signal arrives before V_{IN}, then the enable voltage does not violate the sequencing requirement.

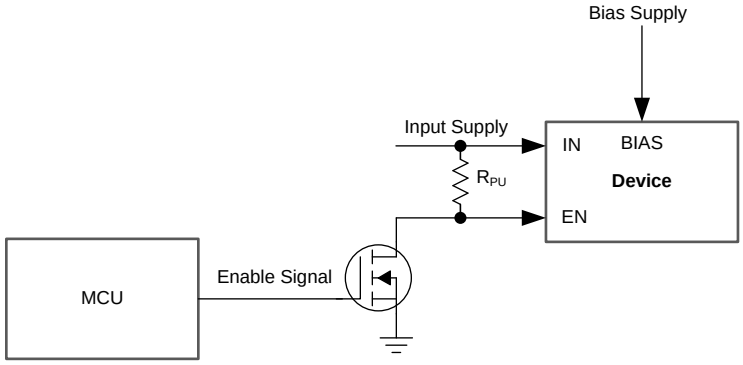

Figure 48. Push-Pull Enable to Open-Drain Enable

8.1.12 Power-Good Operation

To ensure proper operation of the power-good circuit, the pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal may not read a valid digital logic level.

Using a large C_{FF} with a small $C_{NR/SS}$ causes the power-good signal to incorrectly indicate that the output voltage has settled during turn-on. The C_{FF} time constant must be greater than the soft-start time constant to ensure proper operation of the PG during start-up. For a detailed description, see application report *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, SBVA042.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

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8.1.13 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input or bias supplies reach the minimum operational voltage range, and ensures that the device shuts down when the input supply or bias supply collapse.

The UVLO circuit has a minimum response time of several microseconds to fully assert. In this time, a downward line transient below approximately 0.8 V causes a partial assertion of UVLO but the UVLO circuit does not have enough stored energy to fully discharge the internal circuits inside of the device. The effect of the downward line transient can be mitigated by either using a larger input capacitor to limit the fall time of the input supply when operating near the minimum V_{IN}, or by using a bias rail near the minimum V_{IN}.

8.1.14 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$) that is required for regulation. When V_{IN} drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch; see Figure 22, Figure 23, and Figure 24.

Dropout voltage is affected by the drive strength for the gate of the pass element, which is nonlinear with respect to V_{IN} on this device because of the internal charge pump. The charge pump causes a higher dropout voltage at lower input voltages when a bias rail is not used, as illustrated in Figure 20.

For this device, dropout voltage increases exponentially when the input voltage nears its maximum operating voltage because the charge pump is internally clamped to 8.0 V; see Figure 20 and Figure 21.

8.1.15 Behavior when Transitioning from Dropout into Regulation

When the device is in a dropout state (not during start-up), the pass-FET is driven as hard as possible when the control loop is out of balance. During the normal time required for the device to regain regulation, $V_{IN} \geq V_{OUT(nom)} + V_{DO}$, V_{OUT} overshoots if the input voltage slew rate is 0.1 V/µs or faster. The same overshoot can also occur if a load transient causes the device to enter dropout because the error amplifier has a limited response time in recovering from the load dump event. A small dc load can help mitigate this situation.

8.1.16 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained; see Figure 16. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load.

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor

Transitions between current levels changes the internal power dissipation because the TPS7A84 is a high-current device. The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This different output voltage level shows up in the various load transient responses; see Figure 16.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor; see Figure 18.

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8.1.17 Negative Biased Output

The device does not start or operate as expected if the output voltage is pulled below ground. This issue commonly occurs when powering a split-rail system where the negative rail is established before the device is enabled. Several application solutions are:

- Enable the device before the negative regulator and disable the device after the negative regulator.
- Delaying the EN voltage with respect to the IN voltage allows the internal pulldown resistor to discharge any voltage at OUT. If the discharge circuit is not strong enough to keep the output voltage at ground, then use an external pulldown resistor.
- Place a zener diode from IN to OUT to provide a small positive dc bias on the output when the input is supplied to the device, as shown in Figure 49.

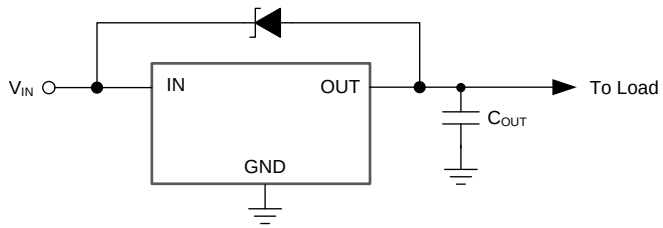

Figure 49. Zener Diode Placed from IN to OUT

- Use a PFET to isolate the output of the device from the load causing the negative bias when the device is off, as shown in Figure 50.

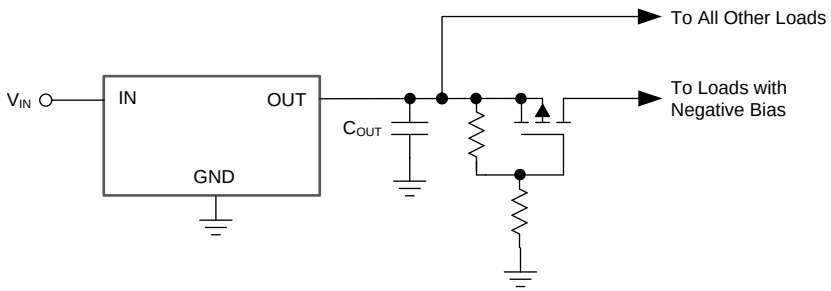

Figure 50. PFET to Isolate the Output from the Load

8.1.18 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be calculated using Equation 9:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \tag{9}$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A84 allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 10.

$$T_J = T_A + (\theta_{JA} \times P_D) \tag{10}$$

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Unfortunately, this thermal resistance (θ_{JA}) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The θ_{JA} recorded in the *Electrical Characteristics* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the VQFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper.

8.1.19 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Electrical Characteristics* table and are used in accordance with Equation 11.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in Equation 9
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (11)

8.2 Typical Applications

8.2.1 Low-Input, Low-Output (LILO) Voltage Conditions

This section discusses the implementation of the TPS7A84 using the ANY-OUT configuration to regulate a 3.0-A load requiring good PSRR at high frequency with low-noise at 0.9 V using a 1.3-V input voltage and a 5.0-V bias supply. The schematic for this typical application circuit is provided in Figure 51.

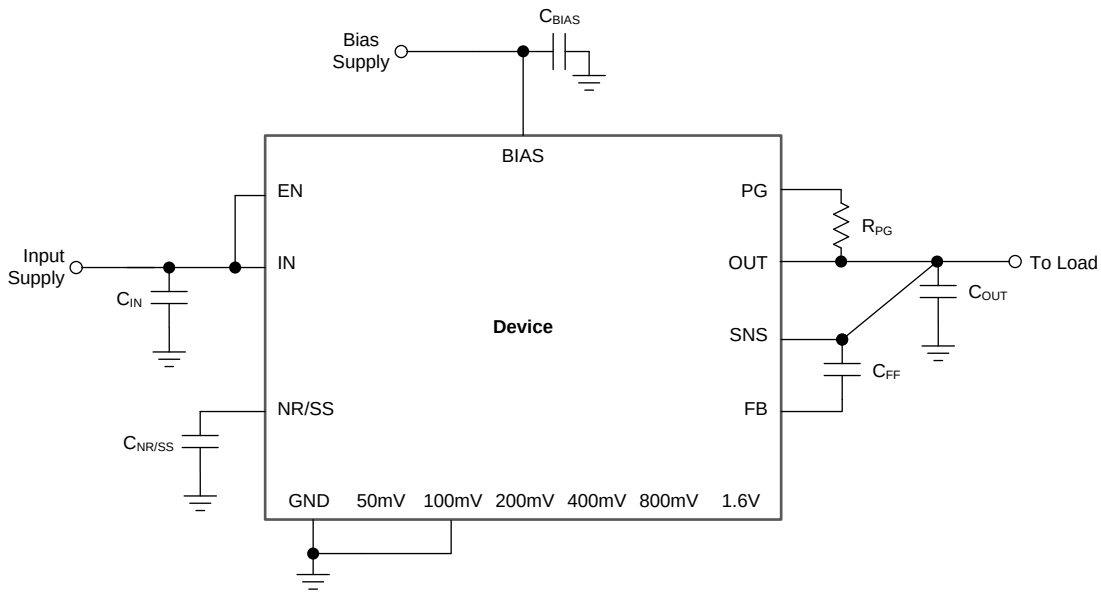

Figure 51. Typical Application

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 6 as the input parameters.

Table 6. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.3 V, ±3%, provided by the dc-dc converter switching at 500 kHz
Bias voltage	5.0 V, ±5%
Output voltage	0.9 V, ±1%
Output current	3.0 A (maximum), 100 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 10 μV_{RMS}
PSRR at 500 kHz	> 40 dB
Start-up time	< 25 ms

8.2.1.2 Detailed Design Procedure

At 3.0 A, the dropout of the TPS7A84 has 180-mV maximum dropout over temperature, thus a 400-mV headroom is sufficient for operation over both input and output voltage accuracy. The bias rail is provided for better performance for the LILO conditions. The PSRR is greater than 40 dB in these conditions, as per Figure 1. Noise is less than 10 μV_{RMS}, as per Figure 8.

The ANY-OUT internal resistor network is also used for maximum accuracy.

To achieve 0.9 V on the output, the 100mV pin is grounded. The voltage value of 100 mV is added to the 0.8-V internal reference voltage for $V_{OUT(nom)}$ equal to 0.9 V, as described in Equation 12.

$$V_{OUT(nom)} = V_{NR/SS} + 0.1\ V = 0.8\ V + 0.1\ V = 0.9\ V \quad (12)$$

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Input and output capacitors are selected in accordance with the *Recommended Capacitor Types* section. Ceramic capacitances of 47 µF for the input and one 47-µF capacitor in parallel with two 10-µF capacitors for the output are selected.

To satisfy the required start-up time and still maintain low-noise performance, a 100-nF $C_{NR/SS}$ is selected. This value is calculated with Equation 13.

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (13)$$

At the 3.0-A maximum load, the internal power dissipation is 1.2 W and corresponds to a 42.48°C junction temperature rise for the RGR package on a standard JEDEC board. With an 55°C maximum ambient temperature, the junction temperature is at 97.5°C. To further minimize noise, a feed-forward capacitance (C_{FF}) of 10 nF is selected.

8.2.1.3 Application Curves

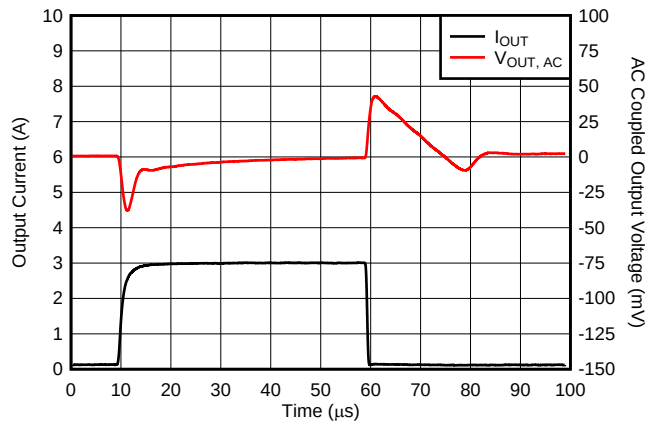

Figure 52. Output Load Transient Response

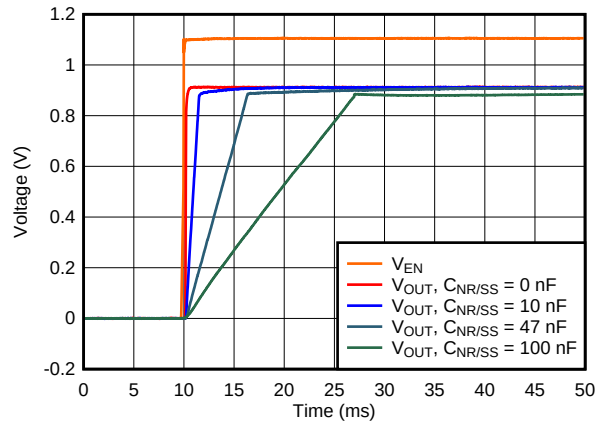

Figure 53. Output Start-Up Response

8.2.2 Typical Application for a 5.0-V Rail

This section discusses the implementation of the TPS7A84 using an adjustable feedback network to regulate a 3-A load requiring good PSRR at high frequency with low-noise at an output voltage of 5.0 V. The schematic for this typical application circuit is provided in Figure 54.

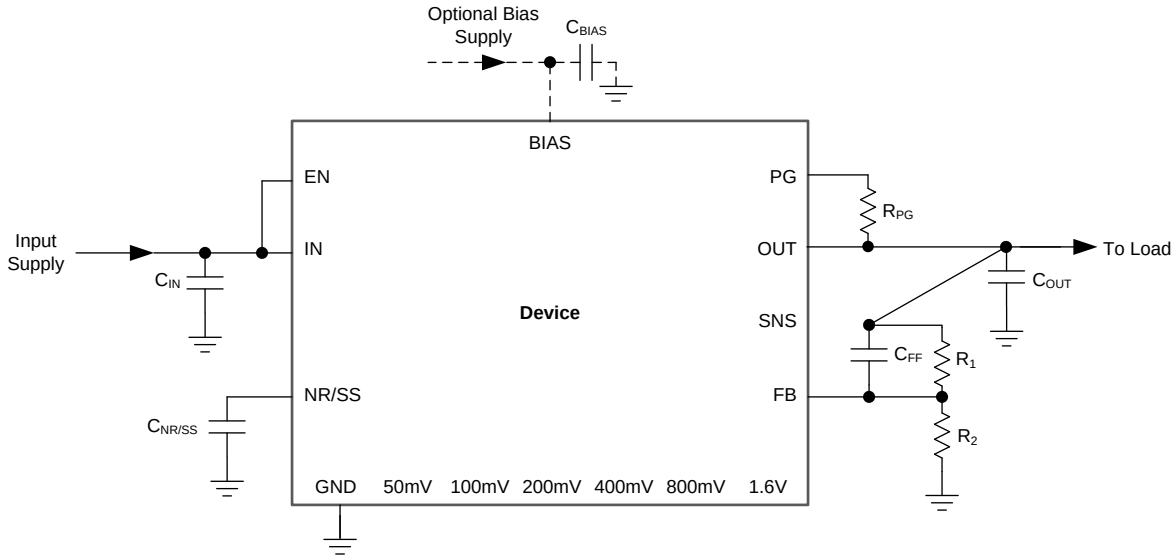

Figure 54. Typical Application

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 6 as the input parameters.

Table 7. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	5.50 V, ±1%, provided by the dc-dc converter switching at 500 kHz
Bias voltage	Not used because V_{OUT} ≥ 2.20 V
Output voltage	5.0 V, ±1%
Output current	3.0 A (maximum), 10 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 10 μV_{RMS}
PSRR at 500 kHz	> 40 dB
Start-up time	< 25 ms

8.2.2.2 Detailed Design Procedure

At 3.0 A and 5.0 V_{OUT}, the dropout of the TPS7A84 has a 340-mV maximum dropout over temperature, thus a 500-mV headroom is sufficient for operation over both input and output voltage accuracy. At full load and high temperature on some devices, the TPS7A84 can enter dropout if both the input and output supply are beyond the edges of their accuracy specification.

For a 5.0-V output. use external adjustable resistors. See the resistor values in listed Table 5 for choosing resistors for a 5.0-V output.

Input and output capacitors are selected in accordance with the *Recommended Capacitor Types* section. Ceramic capacitances of 47 µF for the input and one 47-µF capacitor in parallel with two 10-µF capacitors for the output are selected.

To satisfy the required start-up time and still maintain low noise performance, a 100-nF $C_{NR/SS}$ is selected. This value is calculated with Equation 13.

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (14)$$

At the 3.0-A maximum load, the internal power dissipation is 1.5 W and corresponds to a 53.1°C junction temperature rise for the RGR package on a standard JEDEC board. With an 55°C maximum ambient temperature, the junction temperature is at 108.1°C. To further minimize noise, a feed-forward capacitance (C_{FF}) of 10 nF is selected.

8.2.2.3 Application Curves

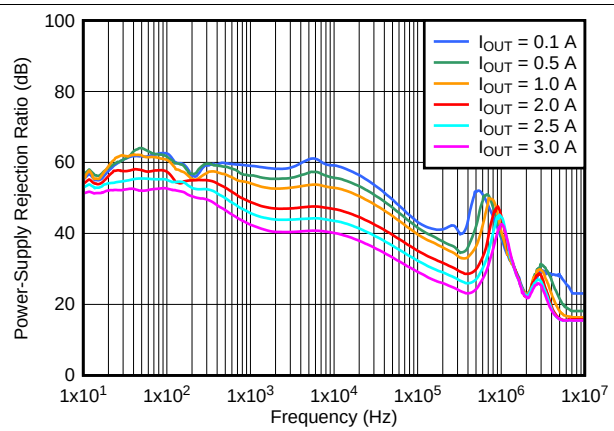

Figure 55. PSRR vs Frequency and I_{OUT} for V_{OUT} = 5.0 V

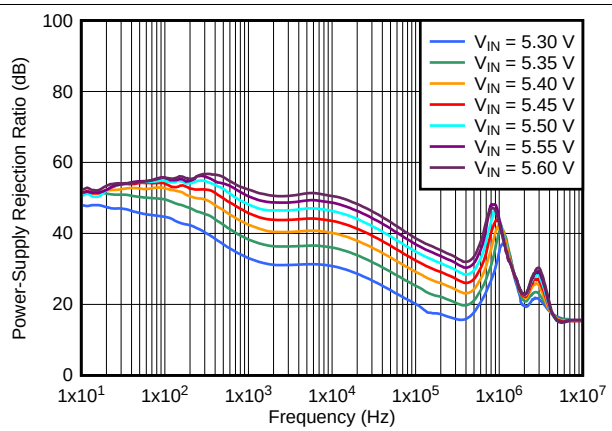

Figure 56. PSRR vs Frequency and V_{IN} for V_{OUT} = 5.0 V at I_{OUT} = 3.0 A

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9 Power-Supply Recommendations

The TPS7A84 is designed to operate from an input voltage supply range between 1.1 V and 6.5 V. If the input supply is less than 1.4 V, then a bias rail of at least 3.0 V must be used. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. The grounding and layout scheme illustrated in Figure 57 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

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10.2 Layout Example

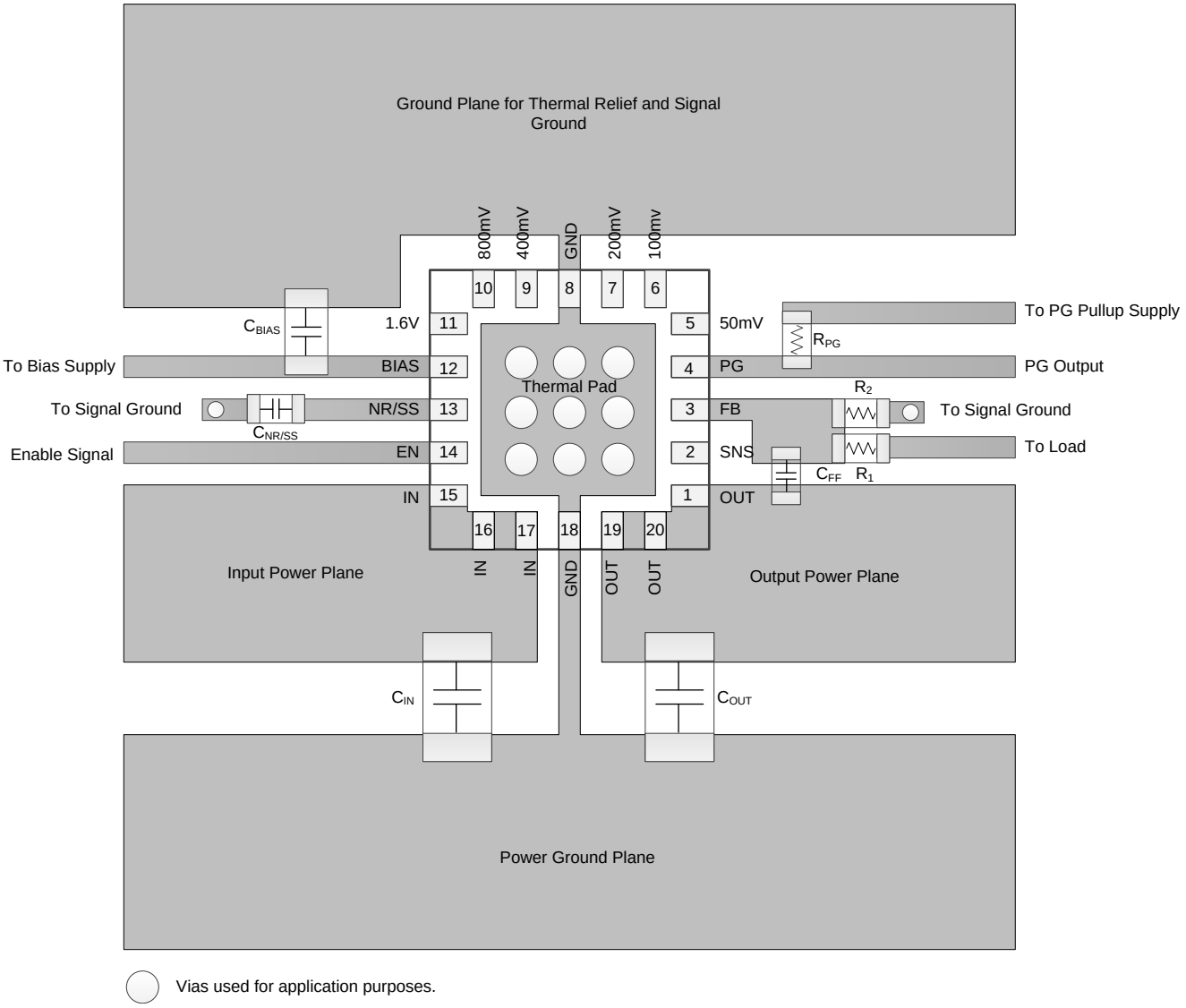

Figure 57. Example Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A84. The summary information for this fixture is shown in Table 8.

Table 8. Design Kits and Evaluation Modules

NAME	LITERATURE NUMBER
TPS7A8300EVM-209 Evaluation Module	SLVU919
TPS7A8300EVM-579 Evaluation Module	SBVU021

The EVM can be requested at the Texas Instruments web site through the TPS7A84 product folder.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A84 is available through the TPS7A84 product folder under simulation models.

11.1.2 Device Nomenclature

Table 9. Ordering Information(1)

PRODUCT	DESCRIPTION
TPS7A84**YYYZ**	**YYY** is the package designator. **Z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- TPS3702 Data Sheet, SBVS251
- TPS7A8300EVM-209 Evaluation Module, SLVU919
- TPS7A8300EVM-579 Evaluation Module, SBVU021
- *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*, SBVA042

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

ANY-OUT, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A8400RGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11CI	Samples
TPS7A8400RGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11CI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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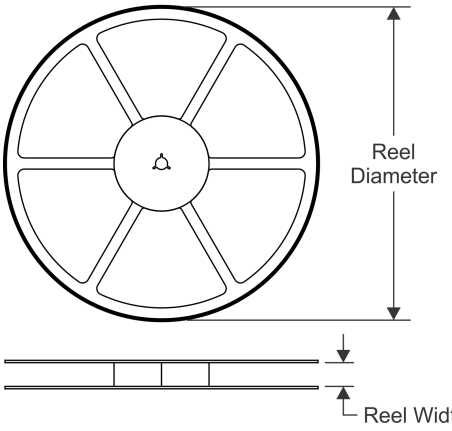
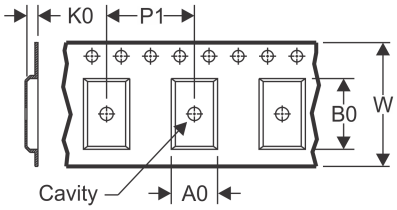
TAPE AND REEL INFORMATION

REEL DIMENSIONS

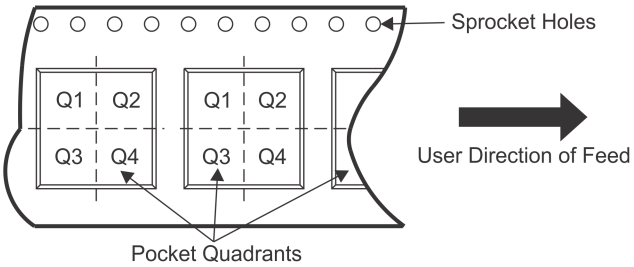


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

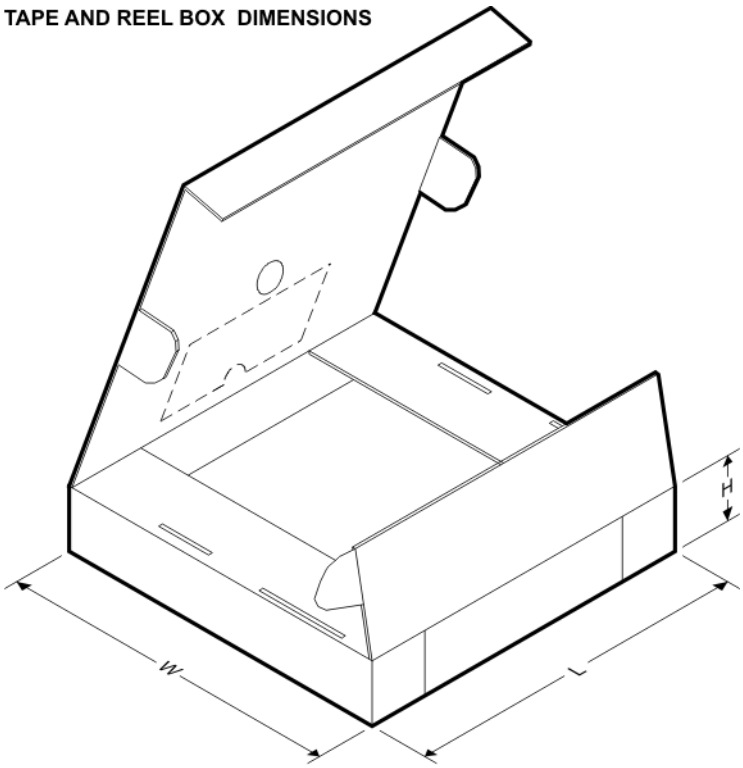
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A8400RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS7A8400RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

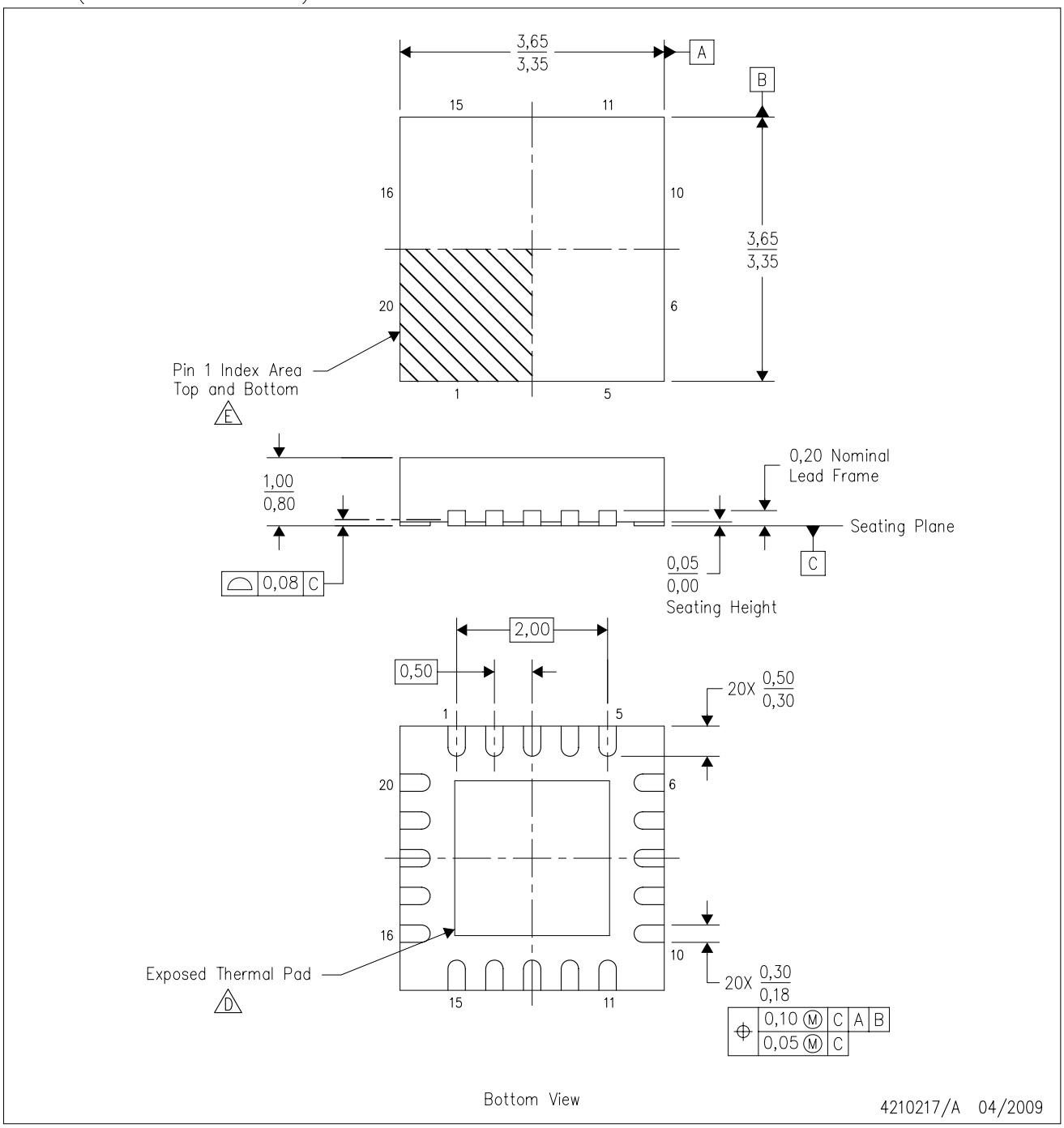
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A8400RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
TPS7A8400RGRT	VQFN	RGR	20	250	210.0	185.0	35.0

RGR (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

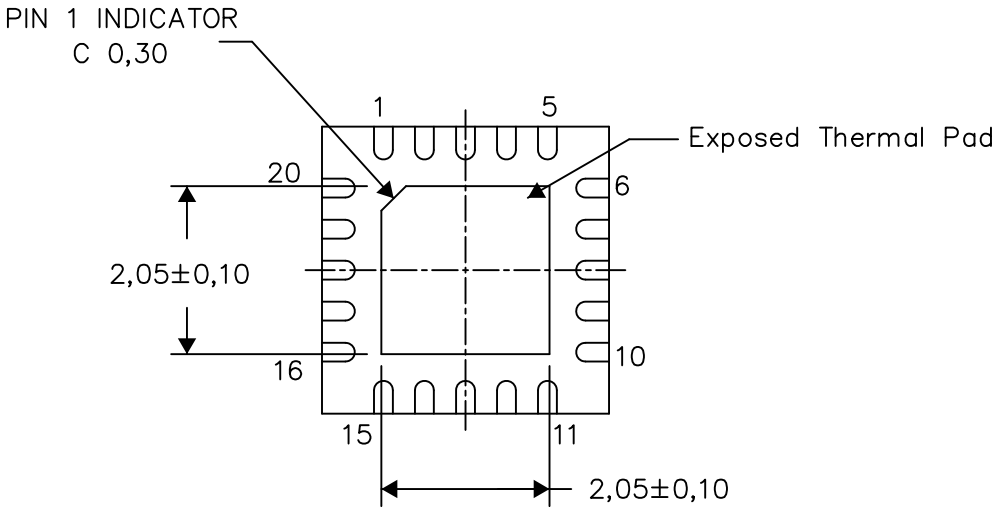
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



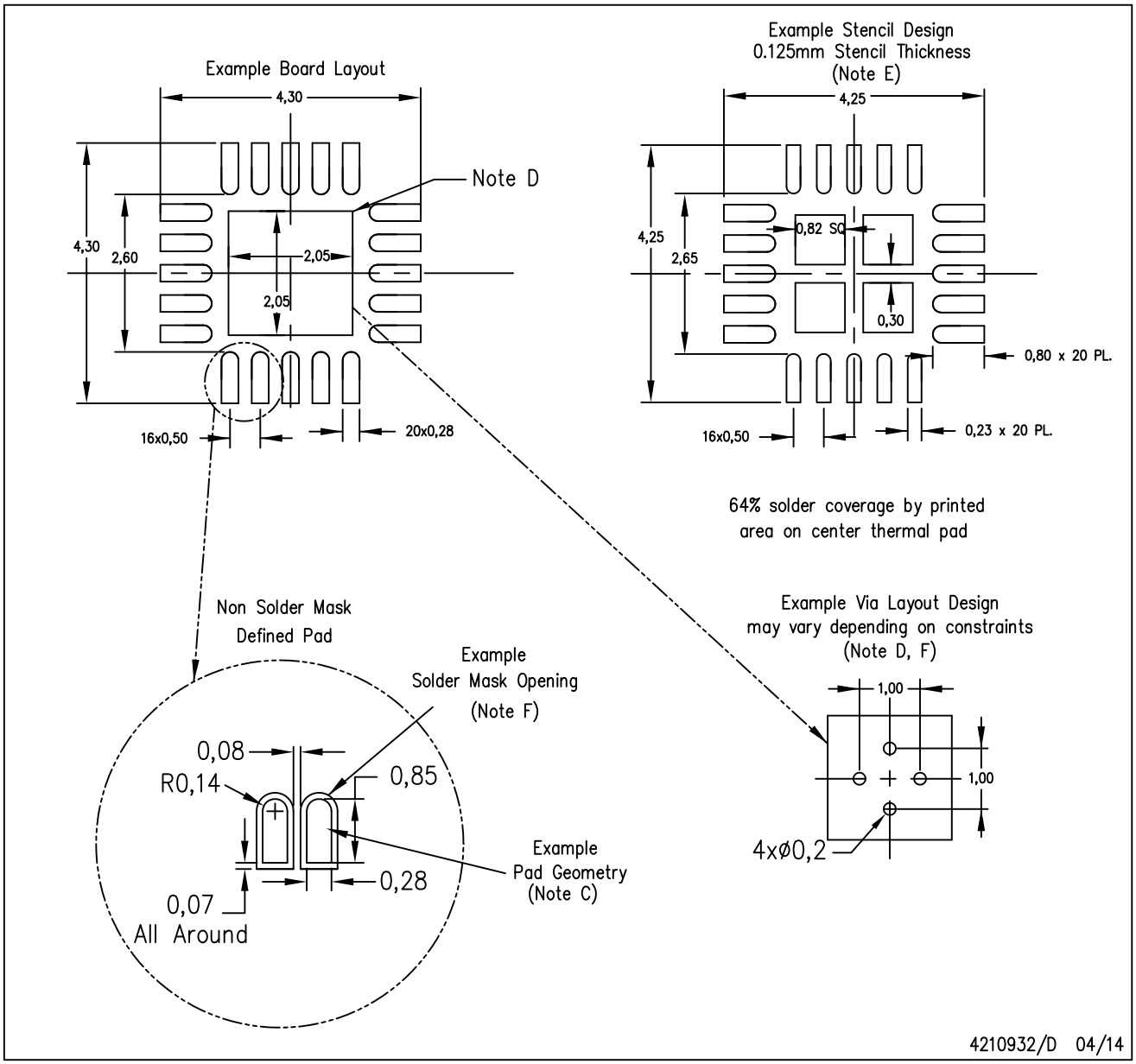
Bottom View

Exposed Thermal Pad Dimensions

4210218/E 04/14

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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