ISL54210

MP3/USB 2.0 High Speed Switch with Negative Signal Handling/Click and Pop Suppression

FN6661
Rev 2.00
March 18, 2010

The Intersil ISL54210 dual SPDT (Single Pole/Double Throw) switch combines low distortion audio and accurate USB 2.0 high-speed data (480Mbps) signal switching in the same low voltage device. When operated with a 2.7V to 3.6V single supply, these analog switches allow audio signal swings below-ground, allowing the use of a common USB and audio headphone connector in Personal Media Players and other portable battery powered devices.

The ISL54210 incorporates circuitry for the detection of the USB V_{BUS} voltage, which is used to switch between the audio and USB signal sources.

It has an enable pin (CTRL) to open all switches and activate the audio click/pop (C/P) circuitry. The high off-isolation and special C/P circuitry of the audio switches eliminates click and pops in the head-phones when the audio CODEC drivers are powering up/down or when a headphone is inserted or removed from the jack.

It's available in a tiny 10 Ld 1.8mmx1.4mm ultra-thin µTQFN package and a 10 Ld 3mmx3mm TDFN package. It operates over a temperature range of -40°C to +85°C.

Related Literature (see page 19)

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Application Note AN1407 "ISL54210EVAL1Z Evaluation Board User's Manual"

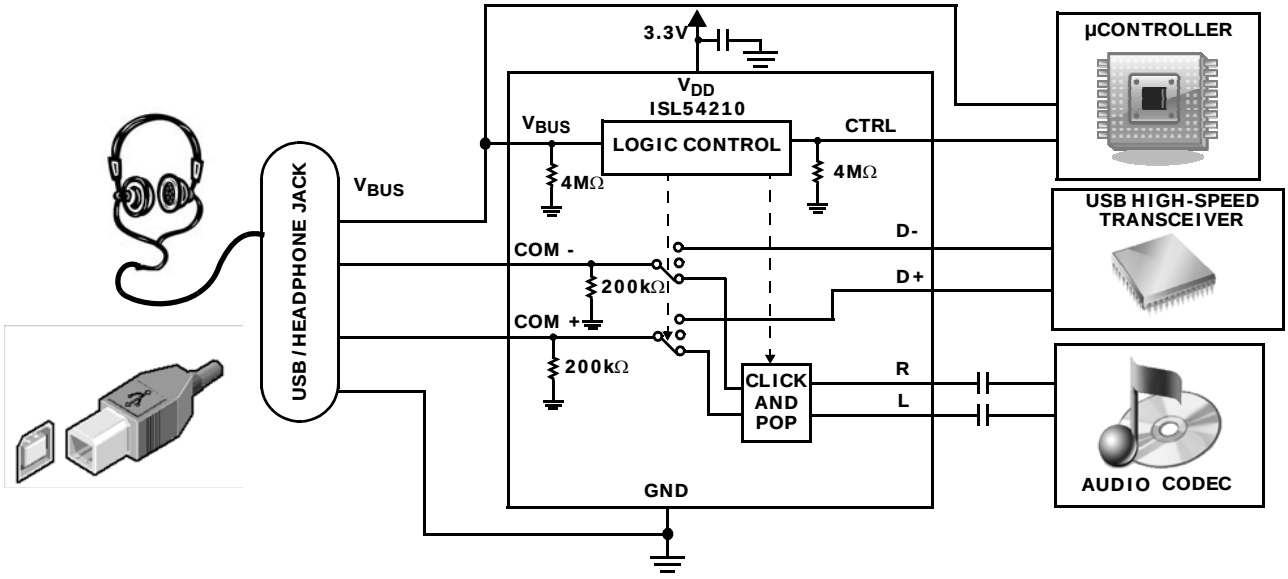
Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Detection of V_{BUS} Voltage on USB Cable
- Low Distortion Negative Signal Capability
- Clickless/Popless Audio Switches
- Enable Pin to Open all Switches
- Low Distortion Headphone Audio Signals
  - 0.014% THD+N at 1mW into 32Ω Load
- -100dB Crosstalk (20Hz to 20kHz)
- 95dB Off-Isolation (20Hz to 100kHz)
- 2.7V to 3.6V Single Supply Operation (V_{DD})
- 700MHz of -3dB Bandwidth USB Switch
- 4.2pF of low ON Capacitance @ 240MHz
- Available in µTQFN and TDFN Packages
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components
- Pb-Free (RoHS Compliant)

Applications* (see page 19)

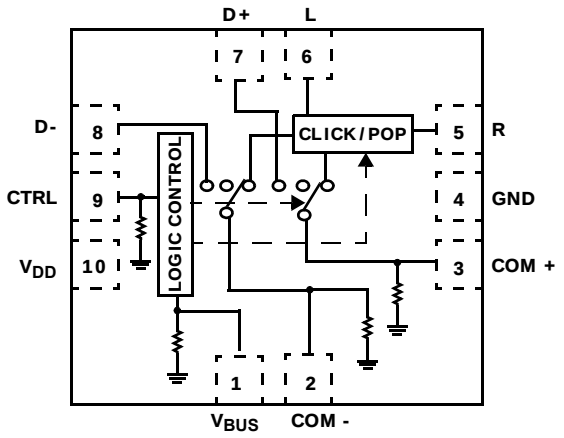
- MP3 and other Personal Media Players
- Cellular/Mobile Phones
- PDAs
- Audio/USB Switching

Application Block Diagram

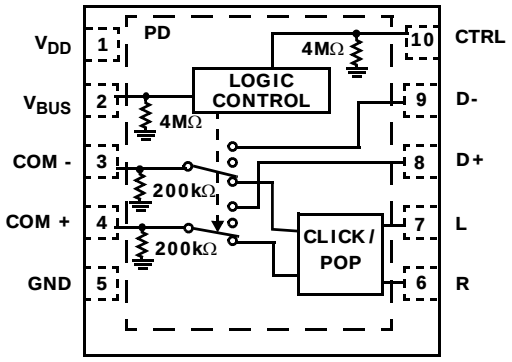


Pin Configurations (Note 1)

ISL54210
(10 LD 1.8mmx1.4mm µTQFN)
TOP VIEW



ISL54210
(10 LD 3.0mmx3.0mm TDFN)
TOP VIEW



NOTE:

1. Switches Shown for V_{BUS} = Logic “0” and CTRL = Logic “1”.

Truth Table

ISL54210			
V_{BUS}	CTRL	L, R	D+, D-
0	0	OFF	OFF
0	1	ON	OFF
1	X	OFF	ON

CTRL: Logic “0” when ≤ 0.5V or Floating, Logic “1” when ≥ 1.4V

V_{BUS}: Logic “0” when ≤ V_{DD} + 0.2V or Floating, Logic “1” when ≥ V_{DD} + 0.8V

Pin Descriptions

ISL54210			
µTQFN	TDFN	NAME	FUNCTION
1	2	V_{BUS}	Digital Control Input
2	3	COM-	Voice and Data Common Pin
3	4	COM+	Voice and Data Common Pin
4	5	GND	Ground Connection
5	6	R	Audio Right Input
6	7	L	Audio Left Input
7	8	D+	USB Differential Input
8	9	D-	USB Differential Input
9	10	CTRL	Digital Control Input (Audio Enable)
10	1	V_{DD}	Power Supply
-	PD	PD	Thermal Pad. Tie to Ground or Float

Ordering Information

PART NUMBER (Note 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54210IRTZ (Note 3)	4210	-40 to +85	10 Ld 3mmx3mm TDFN	L10.3x3A
ISL54210IRTZ-T (Notes 2, 3)	4210	-40 to +85	10 Ld 3mmx3mm TDFN	L10.3x3A
ISL54210IRUZ-T (Notes 2, 4)	0	-40 to +85	10 Ld 1.8mmx1.4mm µTQFN	L10.1.8x1.4A
ISL54210EVAL1Z	Evaluation Board			

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54210. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3V to 5.5V
Input Voltages
D+, D-, L, R (Note 6) . . . . . -2V to ((V_{DD}) + 0.3V)
V_{BUS} (Note 6) . . . . . -2V to 5.5V
CTRL (Note 6) . . . . . -0.3V to ((V_{DD}) + 0.3V)
Output Voltages
COM-, COM+ (Note 6) . . . . . -2V to ((V_{DD}) + 0.3V)
Continuous Current (Audio Switches) . . . . . ±150mA
Peak Current (Audio Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±300mA
Continuous Current (USB Switches) . . . . . ±40mA
Peak Current (USB Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
Human Body Model, COM Pins. . . . . >6kV
Human Body Model, All Pins . . . . . >4kV
Machine Model . . . . . >300V
Charged Device Model . . . . . >1.5kV
Latch-up Tested per JEDEC; Class II Level A . . . . . at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld µTQFN Package (Notes 8, 10)	160	105
10 Ld 3x3 TDFN Package (Notes 7, 9)	55	18

Maximum Junction Temperature (Plastic Package). . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on D+, D-, L, R, COM-, COM+, CTRL, V_{BUS} exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
9. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
10. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{BUSH} = 3.8V, V_{BUSL} = 3.2V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 11), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Audio Switches (L, R)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 2.7V to 3.6V, V_{BUS} = float, CTRL = 1.4V	Full	**-1.5**	-	**1.5**	V
ON-Resistance, r_{ON}	V_{DD} = 3.0V, V_{BUS} = 3.2V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V (see Figure 2, Note 15)	+25	-	2.4	2.8	Ω
		Full	-	-	**3.8**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.0V, V_{BUS} = 3.2V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = Voltage at max r_{ON} over signal range of -0.85V to 0.85V (Notes 15, 16)	+25	-	0.1	0.32	Ω
		Full	-	-	**0.4**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 3.0V, V_{BUS} = 3.2V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (Notes 14, 15)	+25	-	0.02	0.06	Ω
		Full	-	-	**0.07**	Ω
Insertion Loss, G_{ON}	V_{DD} = 3.0V, V_{BUS} = 0V, CTRL = V_{DD}, R_{LOAD} = 32Ω	+25	-	-0.78	-	dB
Insertion Loss, G_{ON}	V_{DD} = 3.0V, V_{BUS} = 0V, CTRL = V_{DD}, R_{LOAD} = 15Ω	+25	-	-1.5	-	dB

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{BUSH} = 3.8V, V_{BUSL} = 3.2V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 11), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
Discharge Pull-Down Resistance, R_L, R_R	V_{DD} = 3.6V, V_{BUS} = 3.2V, CTRL = 0.5V, V_{COM-} or V_{COM+} = -0.85V, 0.85V, V_L or V_R = -0.85V, 0.85V, V_{D+} and V_{D-} = floating; measure current through the discharge pull-down resistor and calculate resistance value.	+25	-	40	-	Ω
USB Switches (D+, D-)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 2.7V to 3.6V, V_{BUS} = 5.0V, CTRL = 0V or V_{DD}	Full	**0**	-	**V_{DD}**	V
ON-Resistance, r_{ON}	V_{DD} = 3.3V, V_{BUS} = 4.4V, CTRL = 1.4V, I_{COMx} = 1mA, V_{D+} or V_{D-} = 3.3V (see Figure 3, Note 15)	+25	-	25	35	Ω
		Full	-	-	**40**	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, V_{BUS} = 4.4V, CTRL = 0V or V_{DD}, I_{COMx} = 40mA, V_{D+} or V_{D-}= 0V to 400mV (see Figure 3, Note 15)	25	-	5.4	6	Ω
		Full	-	-	**7.5**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3V, V_{BUS} = 4.4V, CTRL = 0V or V_{DD}, I_{COMx} = 40mA, V_{D+} or V_{D-}= Voltage at max r_{ON} (Notes 15, 16)	25	-	0.02	0.25	Ω
		Full	-	-	**0.25**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 3.3V, V_{BUS} = 4.4V, CTRL = 0V or V_{DD}, I_{COMx} = 40mA, V_{D+} or V_{D-}= 0V to 400mV (Notes 14, 15)	25	-	0.45	0.55	Ω
		Full	-	-	**0.6**	Ω
OFF Leakage Current, $I_{D+(OFF)}$ or $I_{D-(OFF)}$	V_{DD} = 3.6V, V_{BUS} = 0V, CTRL = 3.6V, V_{COM-} or V_{COM+} = 0.5V, 0V, V_{D+} or V_{D-} = 0V, 0.5V, V_L and V_R = float	25	-10	4	10	nA
		Full	**-50**	-	**50**	nA
ON Leakage Current, I_{DX}	V_{DD} = 3.6V, V_{BUS} = 5.25V, CTRL = 0V or V_{DD}, V_{D+} or V_{D-} = 2.7V, V_{COM-} or V_{COM+} = Float, V_L and V_R = float; measuring current through 200k resistor at COM side	25	-20	11	20	µA
		Full	**-30**	-	**30**	µA
DYNAMIC CHARACTERISTICS						
USB Turn-ON Time, t_{ON}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	43	-	ns
USB Turn-OFF Time, t_{OFF}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	14.5	-	ns
Audio Turn-ON Time, t_{ON}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	7.5	-	µs
Audio Turn-OFF Time, t_{OFF}	V_{DD} =2.7V, R_L = 50Ω, C_L = 10pF (see Figure 1)	25	-	130	-	ns
Skew, t_{SKEW}	V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps, (Duty Cycle = 50%) (see Figure 6)	25	-	50	-	ps
Total Jitter, t_J	V_{DD} =3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, R_L = 50Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps	25	-	210	-	ps
Propagation Delay, t_{PD}	V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, R_L = 45Ω, C_L = 10pF (see Figure 6)	25	-	250	-	ps

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{BUSH} = 3.8V, V_{BUSL} = 3.2V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 11), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
Audio Crosstalk R to COM-, L to COM+	V_{DD} = 3.0V, V_{BUS} = float, CTRL = 3.0V, R_L = 32Ω, f = 20Hz to 20kHz, V_R or V_L = 0.707V_{RMS} ($2V_{P-P}$) (see Figure 5)	25	-	-100	-	dB
Crosstalk (Audio to USB, USB to Audio)	V_{DD} = 3.0V, R_L = 50Ω, f = 100kHz (see Figure 5)	25	-	-100	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 50Ω, f = 100kHz	25	-	95	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 15Ω, f = 20Hz to 20kHz	25	-	111	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 32Ω, f = 20Hz to 20kHz	25	-	105	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 1kΩ, f = 20Hz to 20kHz	25	-	75	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 10kΩ, f = 20Hz to 20kHz	25	-	57	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 100kΩ, f = 20Hz to 20kHz	25	-	45	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, V_{BUS} = Float, CTRL = 3.0V, V_L or V_R = 180mV_{RMS} (509mV_{P-P}) R_L = 32Ω	25	-	0.014	-	%
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, V_{BUS} = Float, CTRL = 3.0V, V_L or V_R = 0.707V_{RMS} ($2V_{P-P}$), R_L = 32Ω	25	-	0.056	-	%
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, V_{BUS} = 0V, CTRL = 3.0V, V_L or V_R = 180mV_{RMS} (509mV_{P-P}), R_L = 15Ω	25	-	0.043	-	%
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, V_{BUS} = 0V, CTRL = 3.0V, V_L or V_R = 0.707V_{RMS} ($2V_{P-P}$), R_L = 15Ω	25	-	0.19	-	%
Click and Pop	V_{DD} = 3.3V, CTRL = 0V, V_{BUS} = float, R_L = 1kΩ, V_L or V_R = 0 to 1.25V DC step or 1.25V to 0V DC step (see Figure 7)	25	-	60	-	µVp
Click and Pop	V_{DD} = 3.3V, CTRL = 0.5Hz square wave, V_{BUS} = float, R_L = 1kΩ, V_L or V_R = AC-coupled to ground (see Figure 8)	25	-	500	-	µVp
USB Switch -3dB Bandwidth	Signal = 0dBm, 0.2VDC offset, R_L = 50Ω, C_L = 5pF	25	-	700	-	MHz
D+/D- OFF Capacitance, C_{D+OFF}, C_{D-OFF}	f = 1MHz, V_{DD} = 3.0V, V_{BUS} = float, CTRL = 3.0V, V_{D-} or V_{D+} = V_{COMx} = 0V (see Figure 4)	25	-	4	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 1MHz, V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V, V_{D-} or V_{D+} = V_{COMx} = 0V (see Figure 4)	25	-	9	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 240MHz, V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V, V_{D-} or V_{D+} = V_{COMx} = 0V (see Figure 4)	25	-	4.2	-	pF

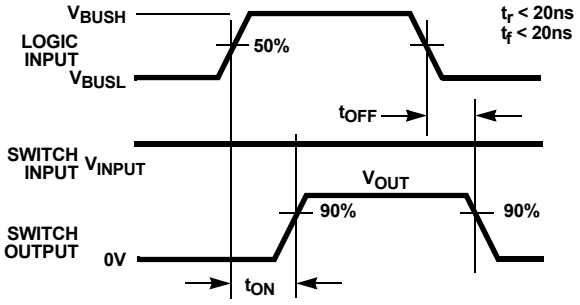
Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{BUSH} = 3.8V, V_{BUSL} = 3.2V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 11), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.7**	-	**3.6**	V
Positive Supply Current, I_{DD} (Audio Mode)	V_{DD} = 3.6V, V_{BUS} = 0V, CTRL = 3.6V	25	-	7	10	µA
		Full	-	-	**12**	µA
Positive Supply Current, I_{DD} (USB Mode)	V_{DD} = 3.6V, V_{BUS} = 5.25V, CTRL = 3.6V	25	-	2.4	4	µA
		Full	-	-	**5**	µA
Positive Supply Current, I_{DD} (Mute Mode)	V_{DD} = 3.6V, V_{BUS} = 0V, CTRL = 0V	25	-	2.4	4	µA
		Full	-	-	**5**	µA
V_{BUS} Current, I_{VBUS}	V_{DD} = 0V, V_{BUS} = 5.25V, CTRL = Float	25	-	-	1	µA
DIGITAL INPUT CHARACTERISTICS						
V_{BUS} Voltage Low, V_{VBUSL}	V_{DD} = 2.7V to 3.6V	Full	-	-	**V_{DD} + 0.2V**	V
V_{BUS} Voltage High, V_{VBUSH}	V_{DD} = 2.7V to 3.6V	Full	**V_{DD} + 0.8V**	-	-	V
CTRL Voltage Low, V_{CTRLL}	V_{DD} = 2.7V to 3.6V	Full	-	-	**0.5**	V
CTRL Voltage High, V_{CTRLH}	V_{DD} = 2.7V to 3.6V	Full	**1.4**	-	-	V
Input Current, I_{VBUSL}, I_{CTRLL}	V_{DD} = 3.6V, V_{BUS}= 0V or float, CTRL = 0V or Float	Full	**-50**	2	**50**	nA
Input Current, I_{VBUSH}	V_{DD} = 3.6V, V_{BUS} = 5.25V, CTRL = 0V or float	Full	**-2**	1	**2**	µA
Input Current, I_{CTRLH}	V_{DD} = 3.6V, V_{BUS} = 0V or float, CTRL = 3.6V	Full	**-2**	1	**2**	µA
V_{BUS} Pull-Down Resistor, R_{VBUS}	V_{DD} = 3.6V, V_{BUS} = 5.25V, CTRL = 0V or float, measure current through the internal pull-down resistor and calculate resistance value.	Full	-	4	-	MΩ
CTRL Pull-Down Resistor, R_{CTRL}	V_{DD} = 3.6V, V_{BUS} = 0V or float, CTRL = 3.6V, measure current through the internal pull-down resistor and calculate resistance value.	Full	-	4	-	MΩ

NOTES:

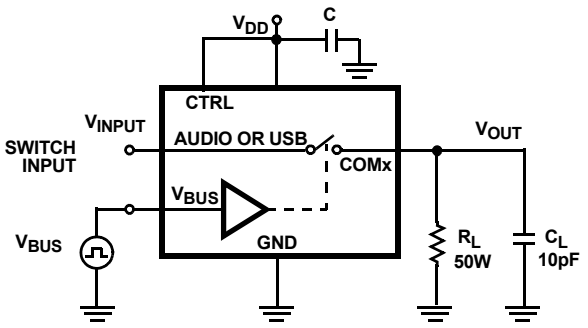
11. V_{LOGIC} = Input voltage to perform proper function.
12. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
14. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
15. Limits established by characterization and are not production tested.
16. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between L and R or between D+ and D-.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

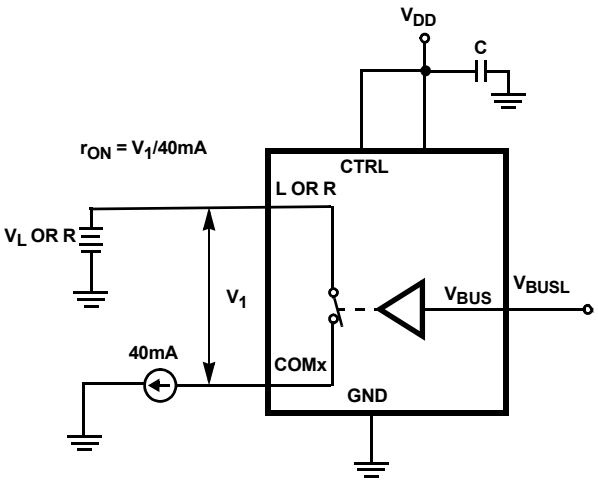


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

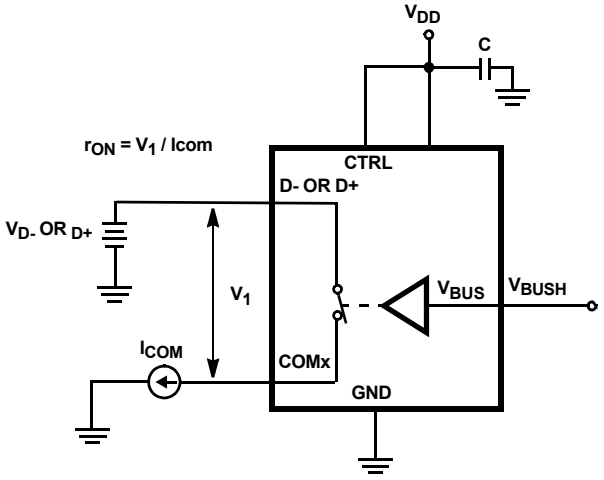
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



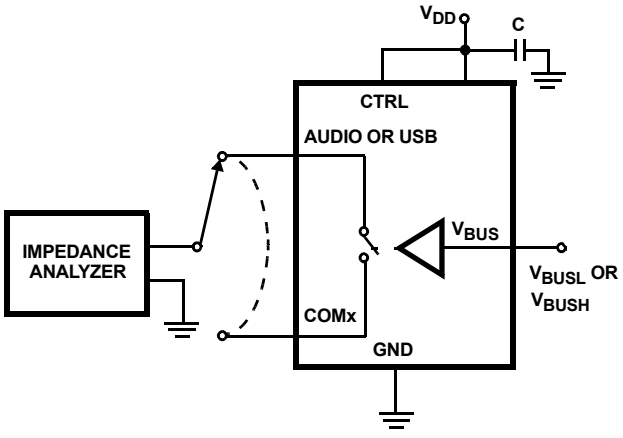
REPEAT TEST FOR ALL SWITCHES

FIGURE 2. AUDIO r_{ON} TEST CIRCUIT



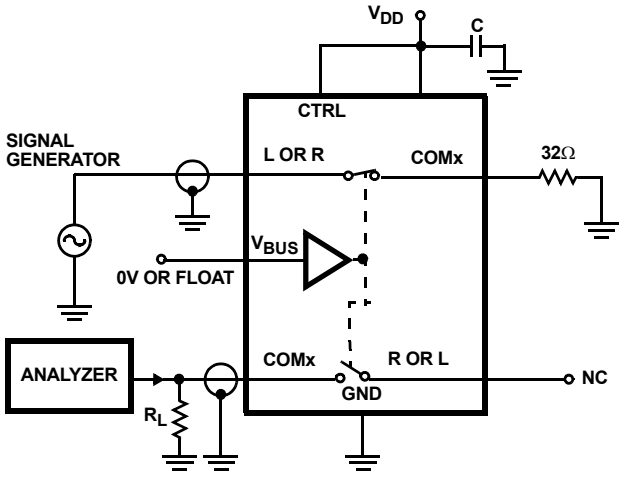
REPEAT TEST FOR ALL SWITCHES

FIGURE 3. USB r_{ON} TEST CIRCUIT



REPEAT TEST FOR ALL SWITCHES

FIGURE 4. CAPACITANCE TEST CIRCUIT



REPEAT TEST FOR ALL SWITCHES

FIGURE 5. AUDIO CROSSTALK TEST CIRCUIT

Test Circuits and Waveforms (Continued)

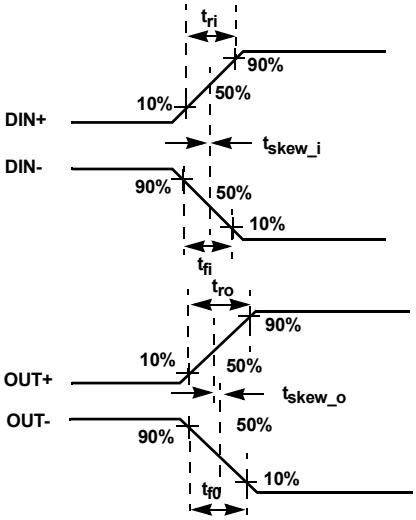
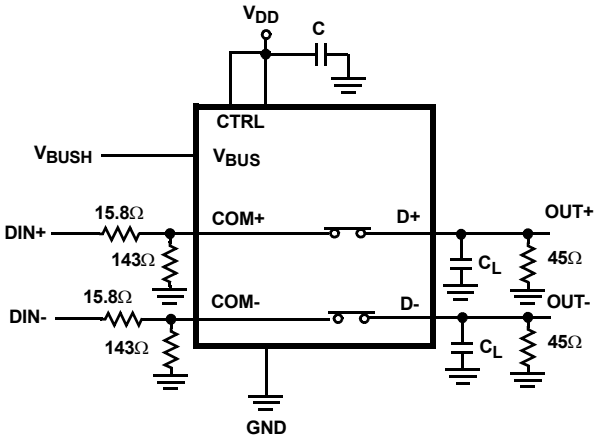


FIGURE 6A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

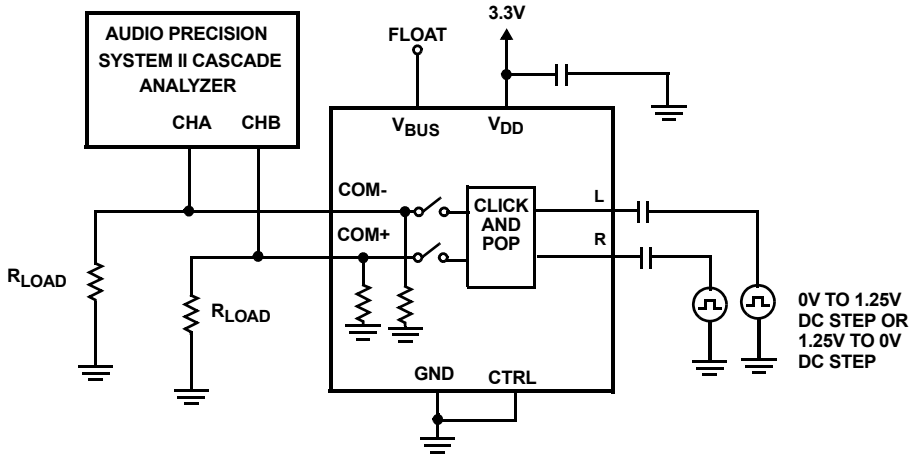
|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 6B. TEST CIRCUIT

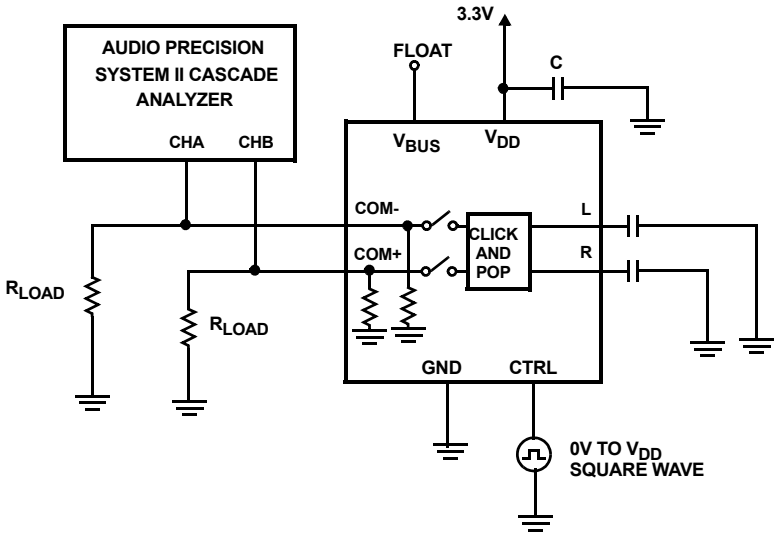
FIGURE 6. SKEW TEST



SET AUDIO ANALYZER FOR PEAK DETECTION, 32 SAMPLES/SEC, A WEIGHTED FILTER, MANUAL RANGE 1X/Y, UNITS TO DBV

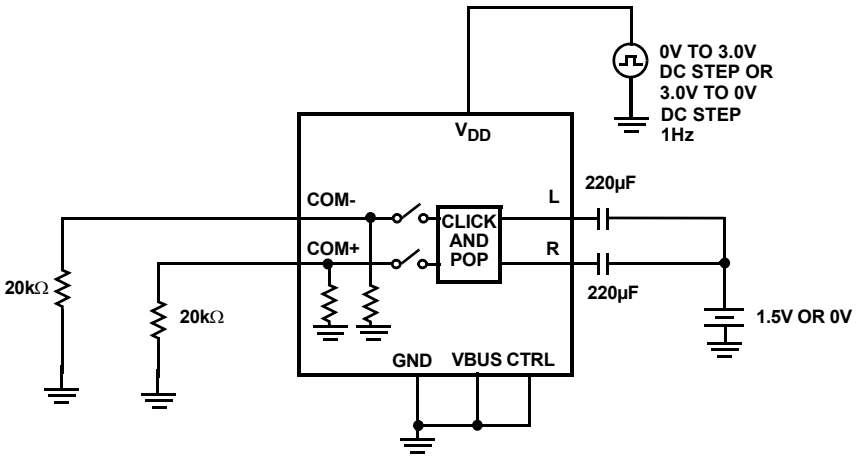
FIGURE 7. CLICK AND POP TEST CIRCUIT

Test Circuits and Waveforms (Continued)



SET AUDIO ANALYZER FOR PEAK DETECTION, 32 SAMPLES/SEC, A WEIGHTED FILTER, MANUAL RANGE 1X/Y, UNITS TO DBV

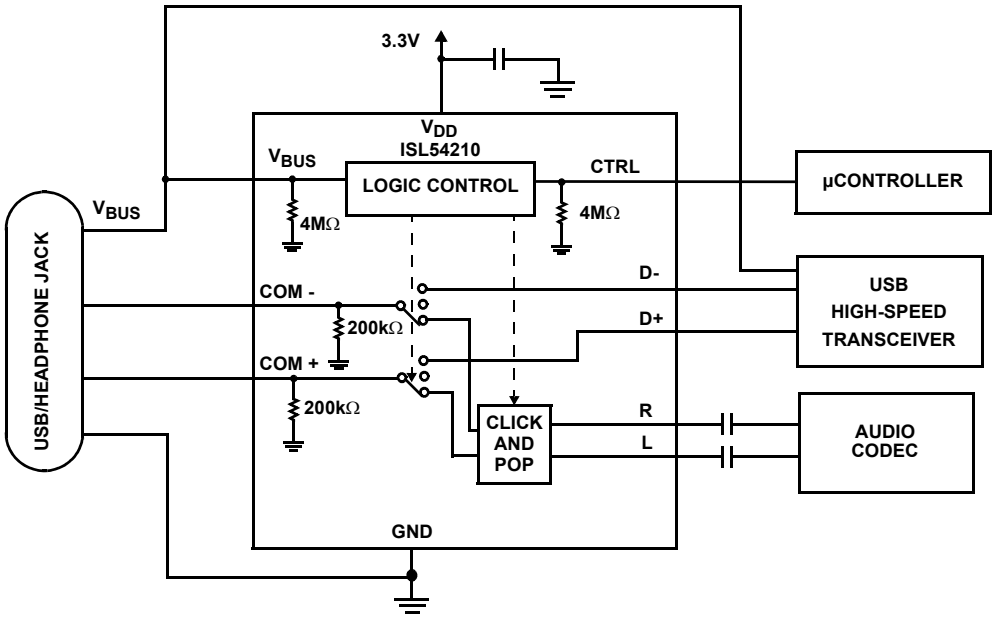
FIGURE 8. CLICK AND POP TEST CIRCUIT



POWER SUPPLY TURN-ON/TURN-OFF CLICK AND POP TRANSIENT TEST

FIGURE 9. CLICK AND POP TEST CIRCUIT #2

Typical Application Block Diagram



Detailed Description

The ISL54210 device is a dual single pole/double throw (SPDT) analog switch that operates from a single DC power supply in the range of 2.7V to 3.6V. It was designed to function as a dual 2-to-1 multiplexer to select between USB differential data signals and audio L and R stereo signals. It comes in tiny µTQFN and TDFN packages for use in MP3 players, PDAs, cellphones, and other personal media players.

The part consists of two 2.5Ω audio switches and two 5.5Ω USB switches. The audio switches can accept signals that swing below ground. They were designed to pass audio left and right stereo signals, that are ground referenced, with minimal distortion. The USB switches were designed to pass high-speed USB differential data signals with minimal edge and phase distortion.

The ISL54210 was specifically designed for MP3 players, personal media players and cellphone applications that need to combine the audio headphone jack and the USB data connector into a single shared connector, thereby saving space and component cost. A “Typical Application Block Diagram” of this functionality is shown on page 11.

The ISL54210 incorporates circuitry for the detection of the USB V_{BUS} voltage, which is used to switch between the audio CODEC drivers and USB transceiver of the MP3 player or cellphone. The ISL54210 contains a logic control pin (CTRL) that when driven low while V_{BUS} is low, opens all switches and activates the audio click and pop circuitry.

A detailed description of the two types of switches are provided in the following sections. In a typical application, the USB transmission and audio playback are intended to be mutually exclusive operations.

Audio Switches

The two audio switches (L, R) are 2.5Ω switches that can pass signals that swing below ground. Crosstalk between the audio switches is <-100dB over the audio band. These switches have excellent off-isolation >105dB over the audio band with a 32Ω load.

Over a signal range of ±1V ($0.707V_{RMS}$) with V_{DD} > 2.7V, these switches have an extremely low r_{ON} resistance variation. They can pass ground referenced audio signals with very low distortion (<0.06% THD+N) when delivering 15.6mW into a 32Ω headphone speaker load. See Figures 16, 17, 18, and 19 THD+N in “Typical Performance Curves” beginning on page 14.

The audio drivers should be connected at the L and R side of the switch (pins 5 and 6 for µTQFN, pins 6 and 7 for TDFN) and the speaker loads should be connected at the COM side of the switch (pins 2 and 3 for µTQFN, pins 3 and 4 for TDFN).

The audio switches have click and pop circuitry on the L and R side that is activated when the V_{BUS} voltage is ≤ V_{DD} + 0.2V or floating and the CTRL voltage ≤ to 0.5V or floating. The ISL54210 should be put in this mode before powering down or powering up of the audio CODEC drivers. In this mode, both the audio and USB in-line switches will be OFF and the audio click and pop circuitry will be ON. The high off-isolation of the audio switches along with the click and pop circuitry will isolate the transients generated during power-up and power-down of the audio CODECs from getting through to the headphones, thus eliminating click and pop noise in the headphones.

The audio switches are active (turned ON) whenever the V_{BUS} voltage is ≤ V_{DD} + 0.2V or floating and the CTRL voltage ≥ to 1.4V.

USB Switches

The two USB switches (D+, D-) are 5.5Ω bidirectional switches that were specifically designed to pass high-speed USB differential signals typically in the range of 0V to 400mV. The switches have low capacitance and high bandwidth to pass USB high-speed signals (480Mbps) with minimum edge and phase distortion to meet USB 2.0 signal quality specifications. See Figure 20 for high-speed eye pattern taken with switch in the signal path.

These switches can also swing rail-to-rail and pass USB full-speed signals (12Mbps) with minimal distortion. See Figure 21 for full-speed eye pattern taken with switch in the signal path.

The maximum signal range for the USB switches is from -1.5V to V_{DD}. The signal voltage at D- and D+ should not be allowed to exceed the V_{DD} voltage rail or go below ground by more than -1.5V.

The USB switches are active (turned ON) whenever the V_{BUS} voltage is ≥ to V_{DD} + 0.8V. V_{BUS} is internally pulled low, so when V_{BUS} is floating the USB switches are OFF.

ISL54210 Operation

The following discusses using the ISL54210 in the "Typical Application Block Diagram" on page 11.

V_{DD} SUPPLY

The DC power supply connected at V_{DD} (Pin 10 for µTQFN, Pin 1 for TDFN) provides the required bias voltage for proper switch operation. Its voltage should be kept in the range of 2.7V to 3.6V when used in a USB/Audio application to ensure you get proper switching when the V_{BUS} voltage is at its lower limit of 4.4V.

In a typical USB/Audio application for portable battery powered devices, the V_{DD} voltage will come from a battery or an LDO and be in the range of 2.7V to 4.3V. For best possible USB full-speed operation (12Mbps), it is recommended that the V_{DD} voltage be ≥2.7V in order to get a USB data signal level above 2.7V.

Before power-up and power-down of the ISL54210 part, the V_{BUS} and CTRL control pins should be driven to ground or tri-stated. This will put the switch in the mute state which turns all switches OFF and activates the click and pop circuitry. Which will minimize transients at the speaker loads during power-up and power-down.

LOGIC CONTROL

The state of the ISL54210 device is determined by the voltage at the V_{BUS} pin (Pin 1 for µTQFN, Pin 2 for TDFN) and the CTRL pin (Pin 9 for µTQFN, Pin 10 for TDFN). The part has three states or modes of operation: Audio Mode, USB Mode and Mute Mode. Refer to the "Truth Table" on page 2.

The V_{BUS} pin and CTRL pin are internally pulled low through 4MΩ resistors to ground and can be left floating or tri-stated. The CTRL control pin is only active when V_{BUS} is logic "0".

Logic Control Voltage Levels:

V_{BUS} = Logic "0" (Low) when $V_{BUS} \leq V_{DD}$ + 0.2V or Floating.
V_{BUS} = Logic "1" (High) when $V_{BUS} \geq V_{DD}$ + 0.8V
CTRL = Logic "0" (Low) when ≤ 0.5V or Floating.
CTRL = Logic "1" (High) when ≥ 1.4V

Audio Mode

If the V_{BUS} pin = Logic "0" and CTRL pin = Logic "1", the part will be in the Audio mode. In Audio mode, the L (left) and R (right) 2.5Ω audio switches are ON, the D- and D+ 5.5Ω switches are OFF (high impedance) and the audio click and pop circuitry is OFF (high impedance).

In a typical application, V_{DD} will be in the range of 2.7V to 3.6V and will be connected to the battery or LDO of the MP3 player or cellphone. When a headphone is plugged into the common connector, nothing gets connected at the V_{BUS} pin (its internally pulled low) and as long as the CTRL = Logic "1" the ISL54210 part remains in the audio mode and the audio drivers of the player can drive the headphones and play music.

USB Mode

If the V_{BUS} pin = Logic "1" and CTRL pin = Logic "0" or Logic "1" the part will go into USB mode. In USB mode, the D- and D+ 5.5Ω switches are ON and the L and R 2.5Ω audio switches are OFF (high impedance).

When a USB cable from a computer or USB hub is connected at the common connector, the voltage at the V_{BUS} pin will be driven with the USB VBUS voltage which will be in the range of 4.4V to 5.25V. The ISL54210 part will go into the USB mode. In USB mode, the computer or USB hub transceiver and the MP3 player or cellphone USB transceiver are connected and digital data will be able to be transmitted back and forth.

When the USB cable is disconnected the ISL54210 automatically turns the D+ and D- switches OFF.

Mute Mode

If the V_{BUS} pin = Logic "0" and CTRL pin = Logic "0", the part will be in the Mute mode. In the Mute mode, the audio switches and the USB switches are OFF (high impedance) and the audio click and pop circuitry is ON.

Before powering down or powering up of the audio CODECs drivers, the ISL54210 should be put in the Mute mode. In Mute mode transients present at the L and R signal pins due to the changing DC voltage of the audio drivers will not pass to the headphones preventing clicks and pops in the headphones. See "AC-Coupled click and pop operation" on page 13.

Before power-up and power-down of the ISL54210 part, the V_{BUS} and CTRL control pins should be driven to ground or tri-stated. This will put the switch in the mute state, which turns all switches OFF and activates the click and pop circuitry. This will minimize transients at the

speaker loads during power-up and power-down. See Figure 30 in the “Typical Performance Curves” on page 18.

AC-COUPLED CLICK AND POP OPERATION

Single supply audio drivers have their signal biased at a DC offset voltage (usually at 1/2 the DC supply voltage of the driver). As this DC bias voltage comes up or goes down during power-up or power-down of the driver, a transient can be coupled into the speaker load through the DC blocking capacitor (see the“Typical Application Block Diagram” on page 11).

When a driver is OFF and then turned ON, the rapidly changing DC bias voltage at the output of the driver will cause an equal voltage at the input side of the switch due to the fact that the voltage across the blocking capacitor cannot change instantly. If the switch is in the Audio mode or there is no low impedance path to discharge the blocking capacitor voltage at the input of the switch, before turning on the audio switch, a transient discharge will occur in the speaker, generating a click/pop noise.

Proper elimination of a click/pop transient at the speaker loads while powering up or down of the audio drivers requires that the ISL54210 have its click/pop circuitry activated by putting the part in the Mute mode. This allows the transients generated by the audio drivers to be discharged through the click and pop shunt circuitry.

Once the driver DC bias has reached $V_{DD}/2$ and the transient on the switch side of the DC blocking capacitor has been discharged to ground through the click/pop shunt circuitry, the audio switches can be turned ON and connected through to the speaker loads without generating any undesirable click/pop noise in the speakers.

With a typical DC blocking capacitor of 220µF and the click/pop shunt circuitry designed to have a resistance of 20Ω to 70Ω, allowing a 100ms wait time to discharge the transient before placing the switch in the Audio mode will prevent the transient from getting through to the speaker load. See Figures 28 and 29 in the “Typical Performance Curves” page 17.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

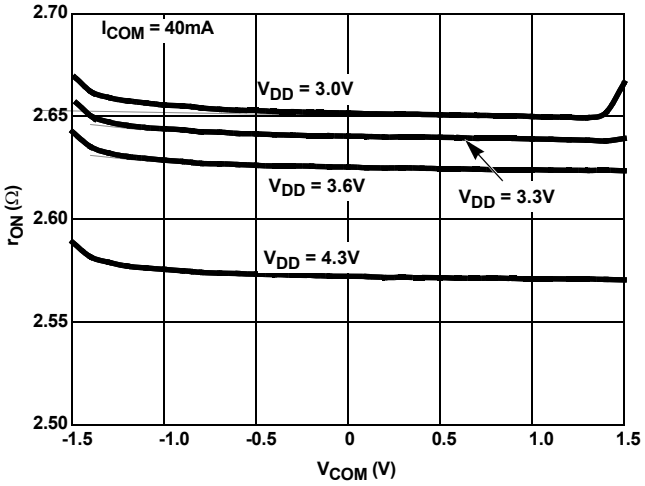


FIGURE 10. AUDIO ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

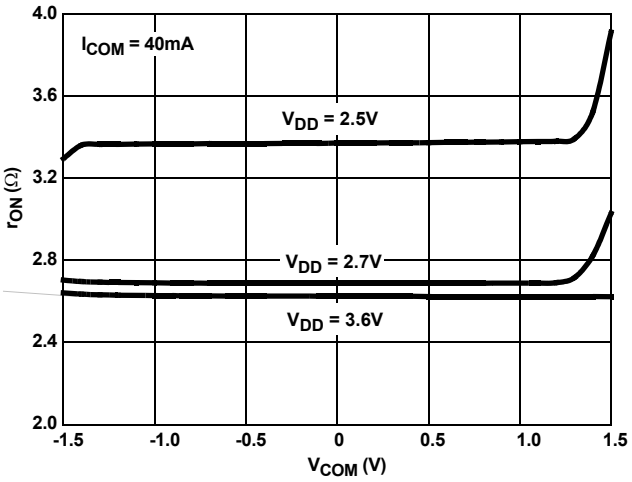


FIGURE 11. AUDIO ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

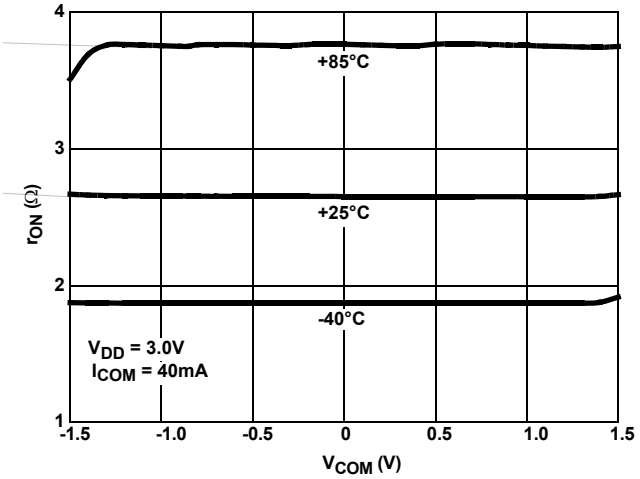


FIGURE 12. AUDIO ON-RESIDTANCE vs SWITCH VOLTAGE vs TEMPERATURE

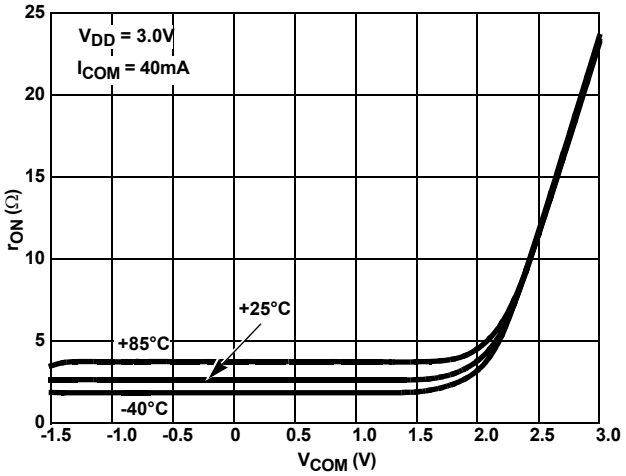


FIGURE 13. AUDIO ON-RESIDTANCE vs SWITCH VOLTAGE vs TEMPERATURE

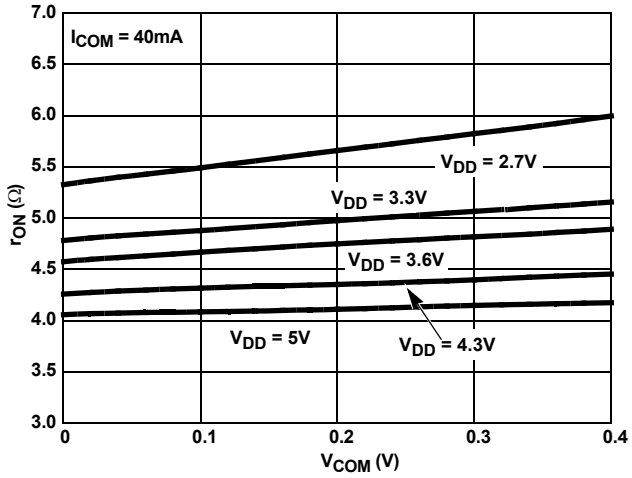


FIGURE 14. USB ON-RESIDTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

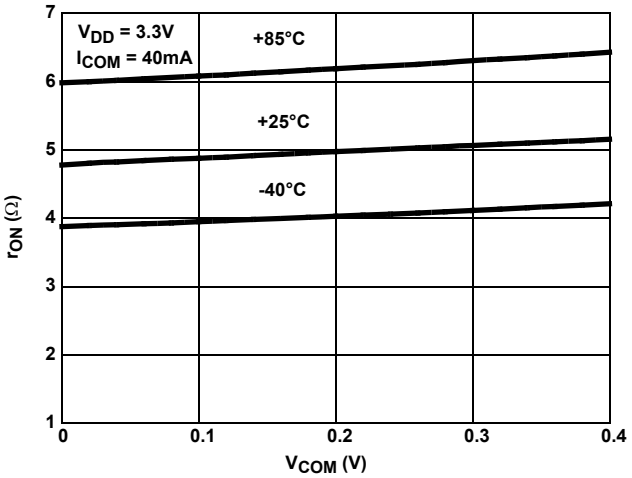


FIGURE 15. USB ON-RESIDTANCE vs SWITCH VOLTAGE vs TEMPERATURE

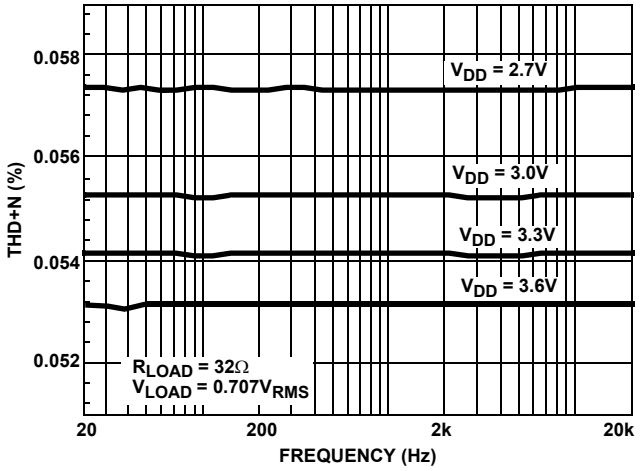


FIGURE 16. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

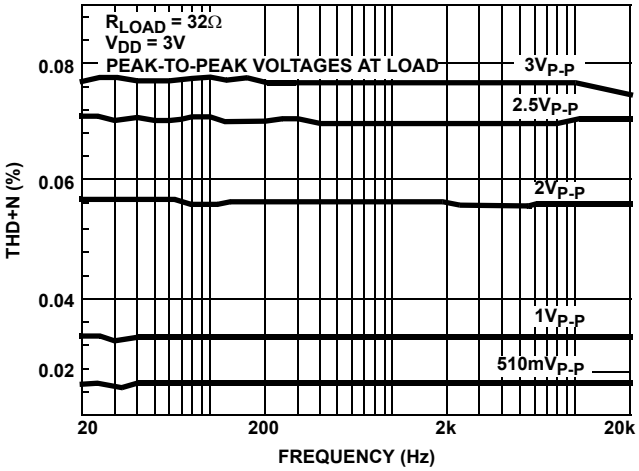


FIGURE 17. THD+N vs SIGNAL LEVELS vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

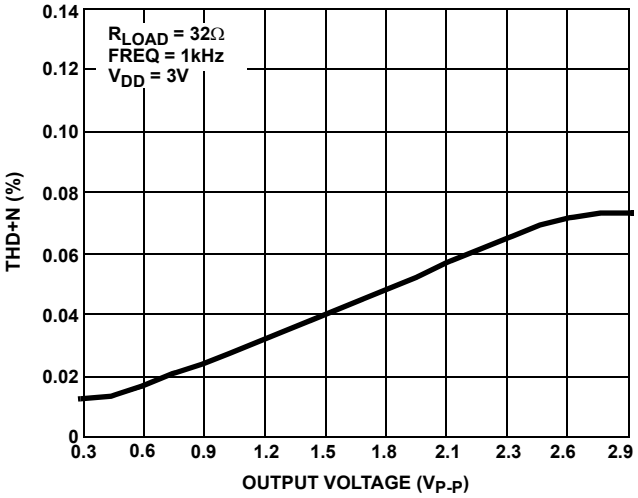


FIGURE 18. THD+N vs OUTPUT VOLTAGE

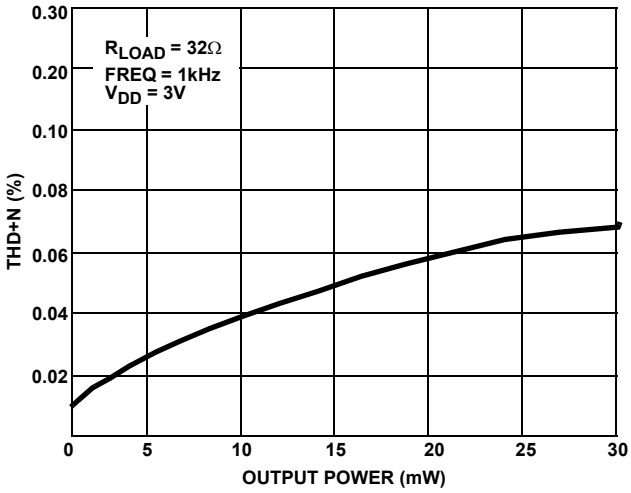


FIGURE 19. THD+N vs OUTPUT POWER

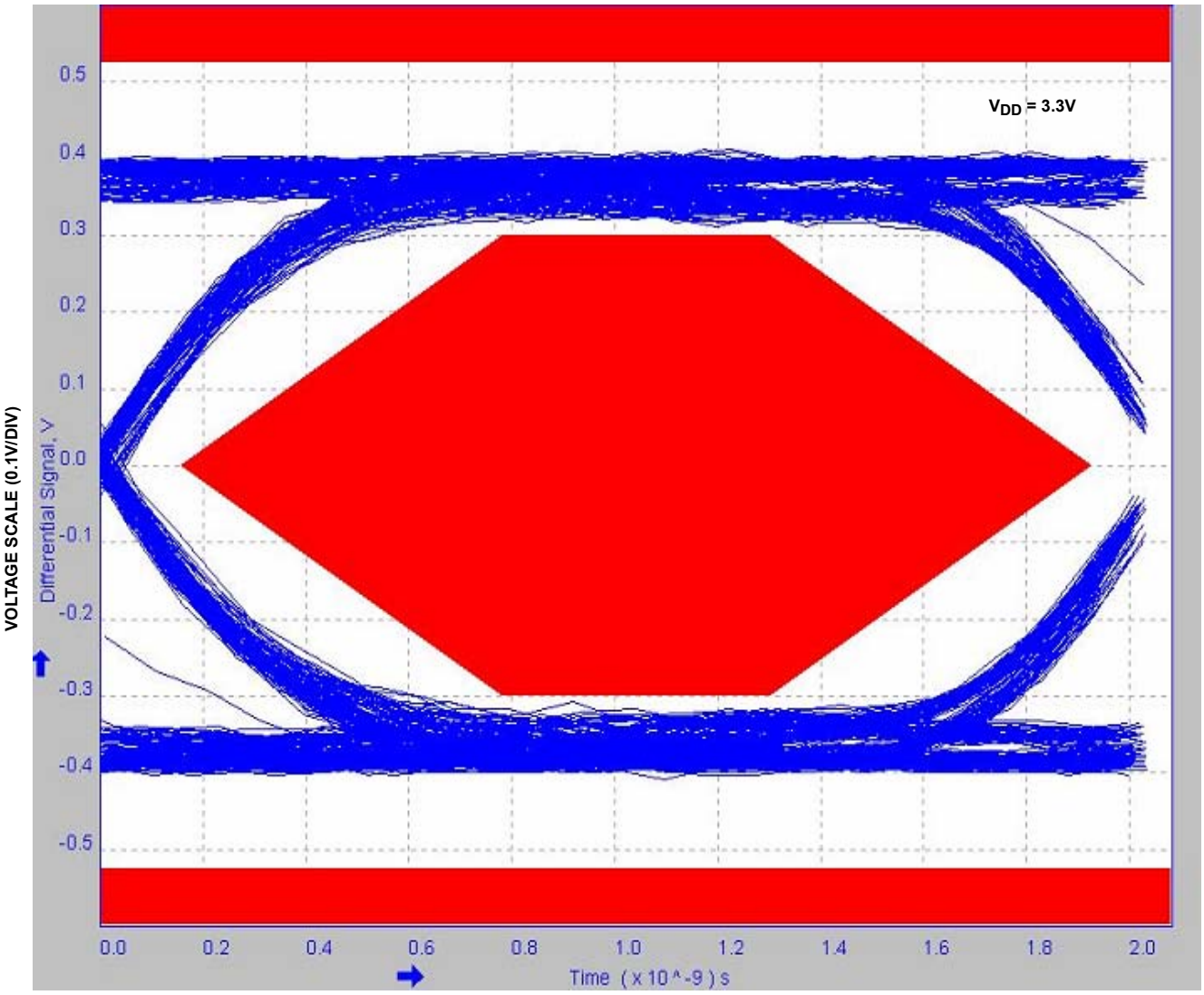


FIGURE 20. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

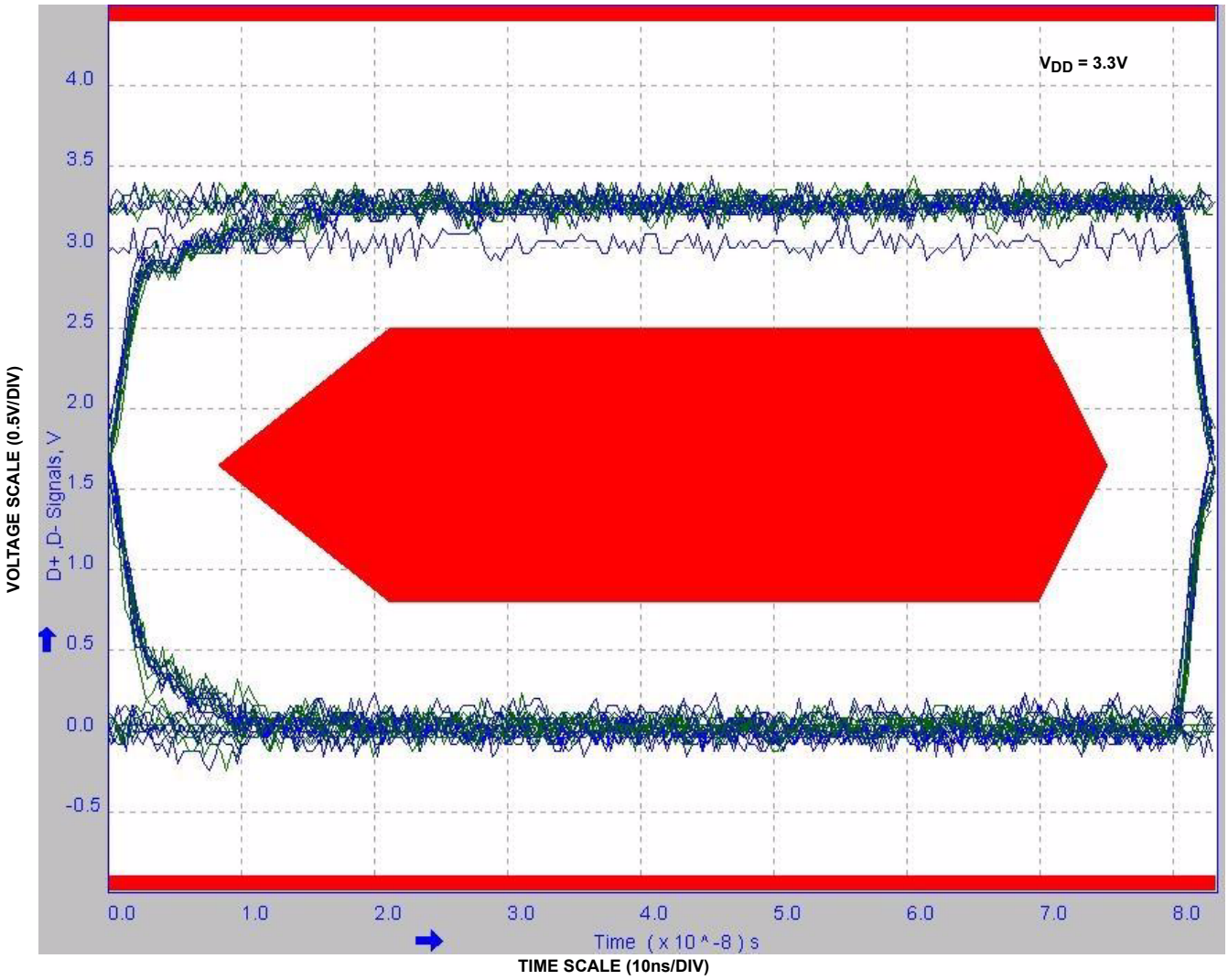


FIGURE 21. EYE PATTERN: 12Mbps USB SIGNAL WITH USB SWITCHES IN THE SIGNAL PATH

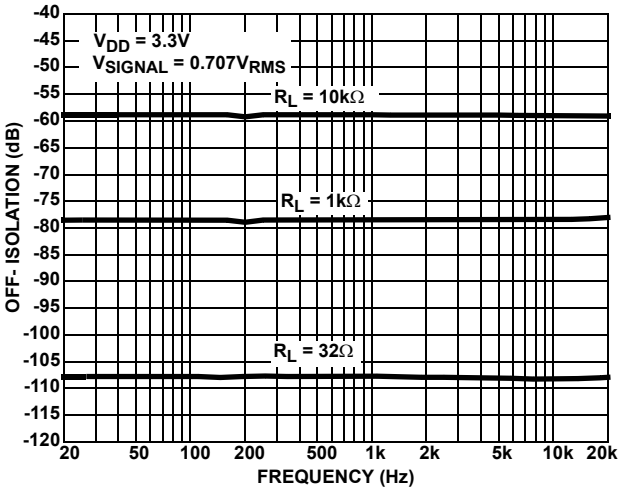


FIGURE 22. OFF-ISOLATION AUDIO SWITCHES vs LOADING

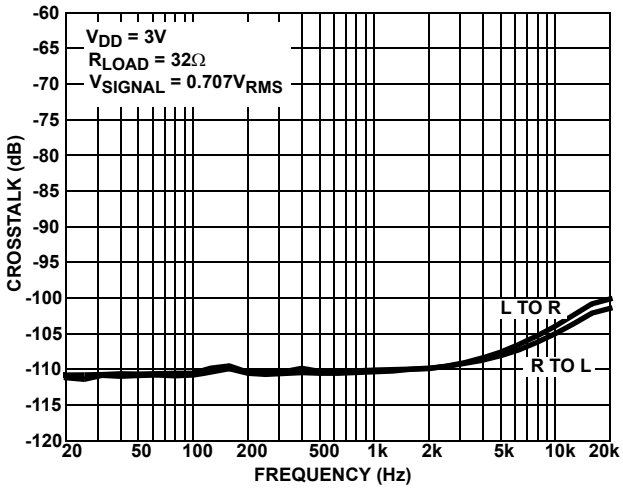


FIGURE 23. AUDIO CHANNEL-TO-CHANNEL CROSSTALK

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

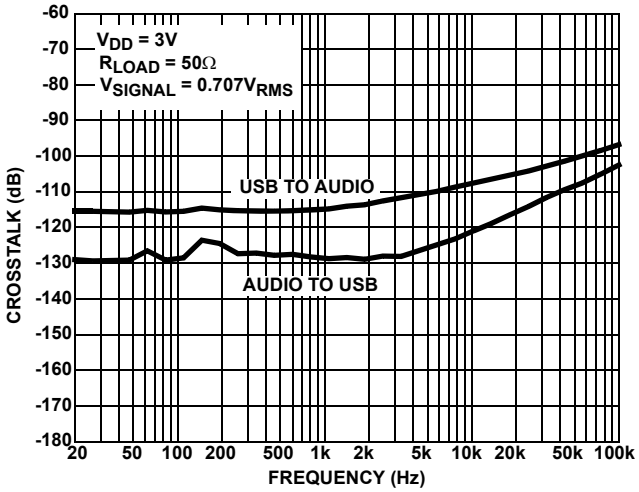


FIGURE 24. CHANNEL-TO-CHANNEL CROSSTALK

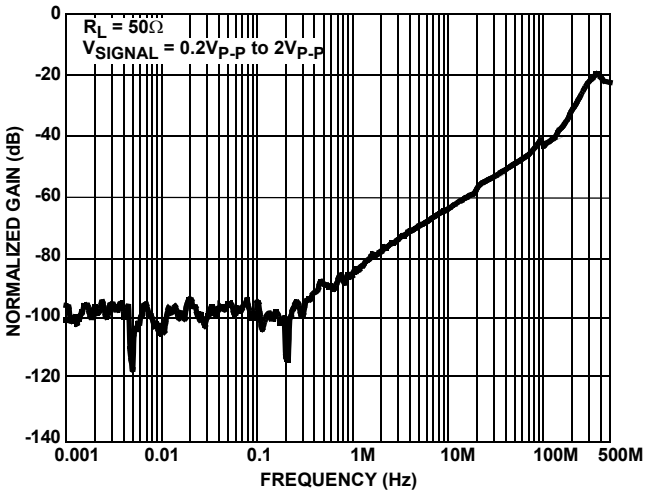


FIGURE 25. OFF-ISOLATION USB SWITCHES

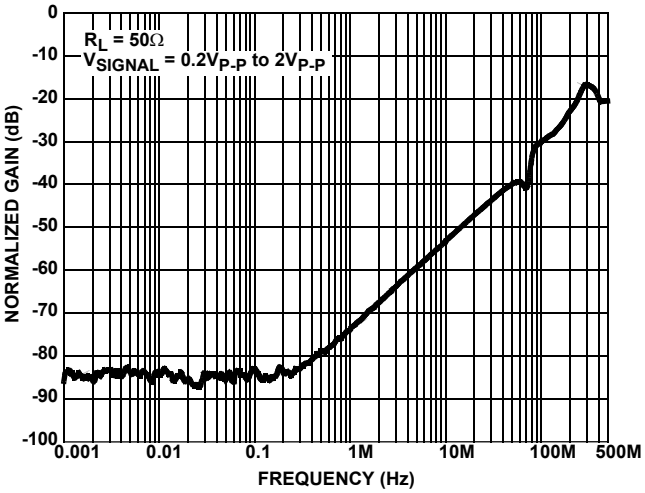


FIGURE 26. OFF-ISOLATION AUDIO SWITCHES

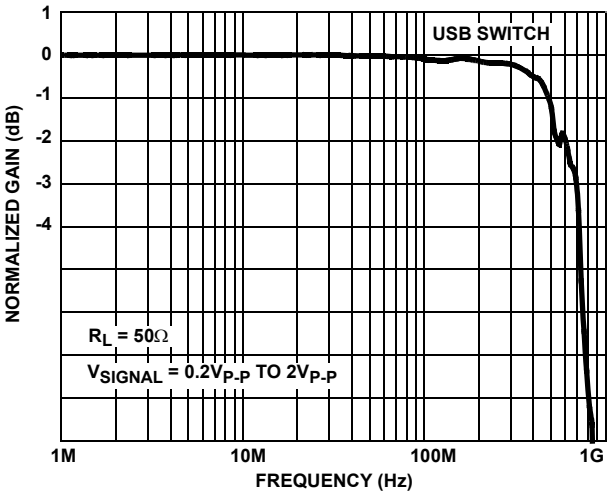


FIGURE 27. FREQUENCY RESPONSE

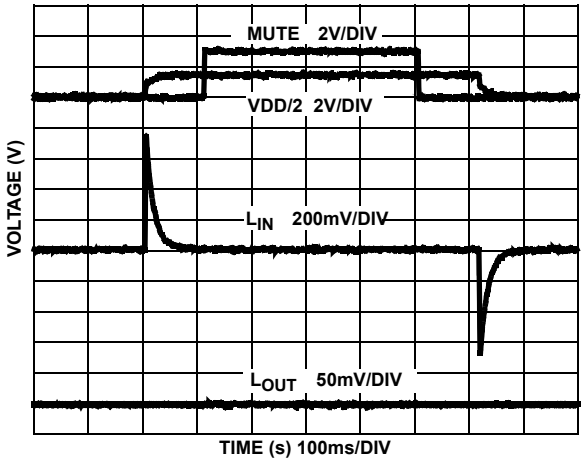


FIGURE 28. 32Ω AC-COUPLED CLICK AND POP REDUCTION

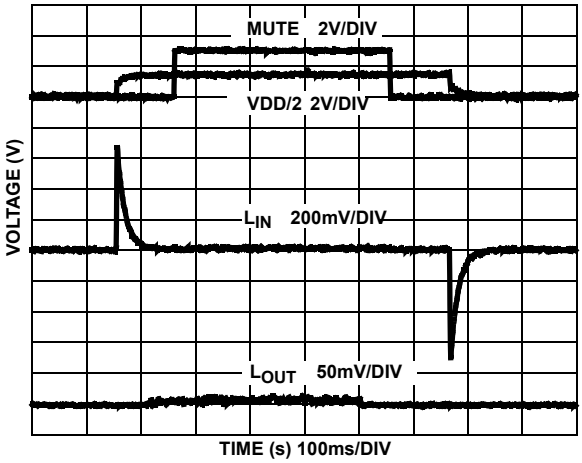


FIGURE 29. 1kΩ AC-COUPLED CLICK AND POP REDUCTION

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

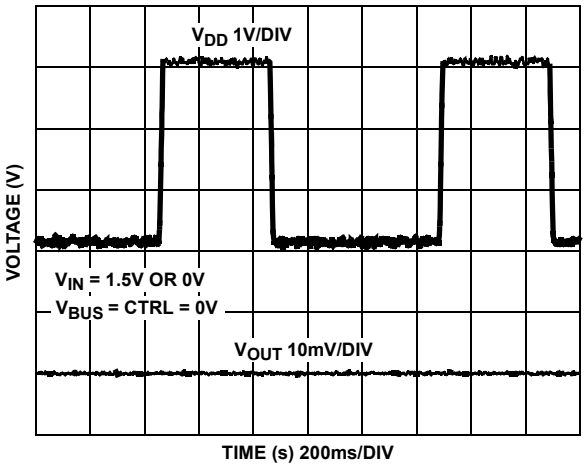


FIGURE 30. POWER-UP / POWER-DOWN CLICK AND POP TRANSIENT

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

98

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
3/18/10	FN6661.2	Converted to New Intersil Template Replaced note, page 3: "θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details." with "direct attached note" Added "Boldface limits apply over the operating temperature range, -40°C to +85°C." to Electrical Specifications table. On page 1 in "Related Literature" section added App Note AN1407. On page 1 in "Features" section added "Low On Capacitance at 240MHz 4.2pF" On page 2 added thermal pad (PD) to TDFN pinout and added PD column to "Pin Descriptions" table. Page 4 in "Abs Max Rating" section added HBM rating for COM pins of 6kV and Latchup level. Thermal information Tjc for uTQFN changed from "61.9" to "105" and note for Tja was added to reference no direct attach, added Tjc to show the case temp location at top center. Page 4 in Electrical Spec Table - Removed Note Reference from Typical Column and Added to specific specs in Audio Switches and USB Switches as follows: On Resistance, rON Matching Between Channels and rON Flatness. Page 6 in electrical specifications table added "On Capacitance at 240MHz parameter. Page 15 Figure 20 Change from USB far end mask to USB near end mask. Page 18 in "Die Characteristics" section added TDFN thermal pad potential.
1/6/09	FN6661.1	Corrected Order Information.
7/2/08	FN6661.0	Initial Release to web

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL54210

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

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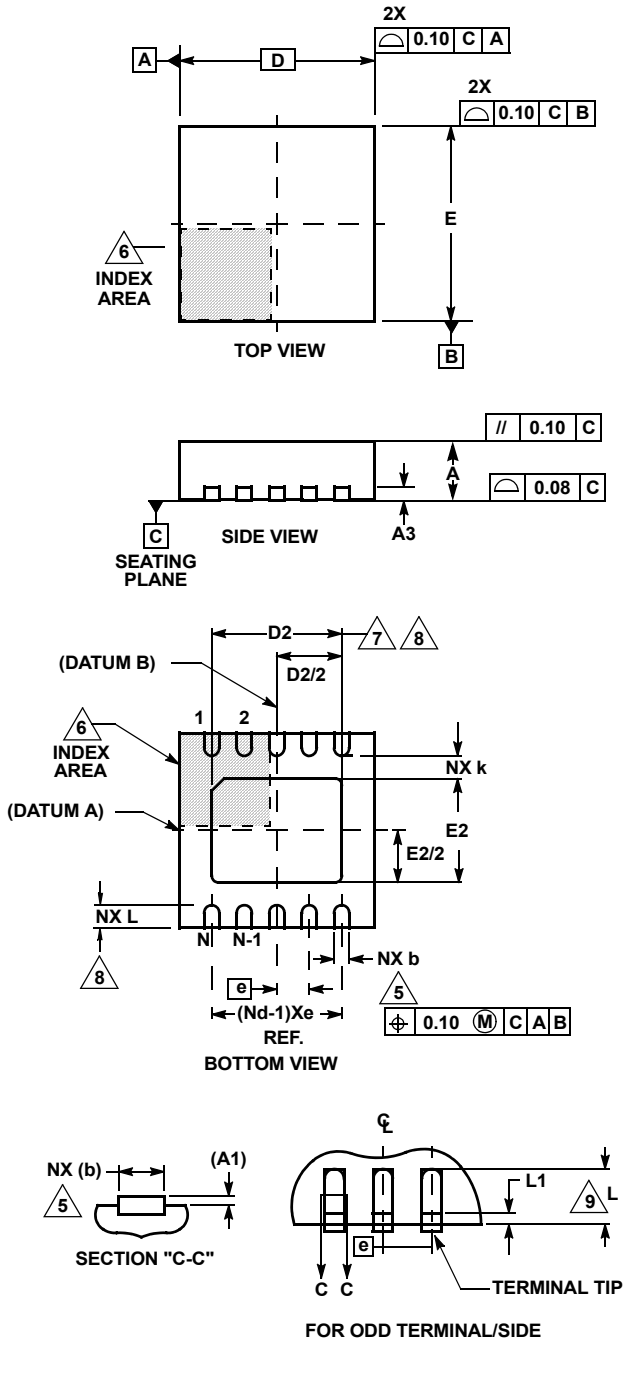
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Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

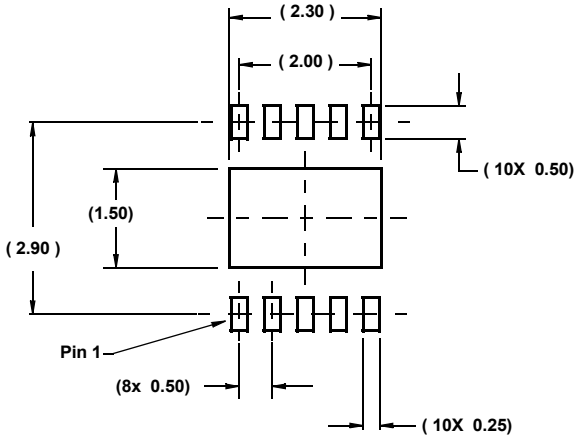
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N		10		2
Nd		5		3

Rev. 4 8/09

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.



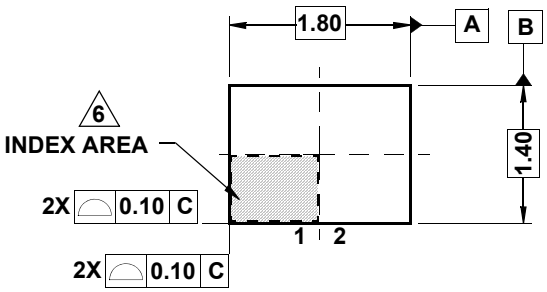
TYPICAL RECOMMENDED LAND PATTERN

Package Outline Drawing

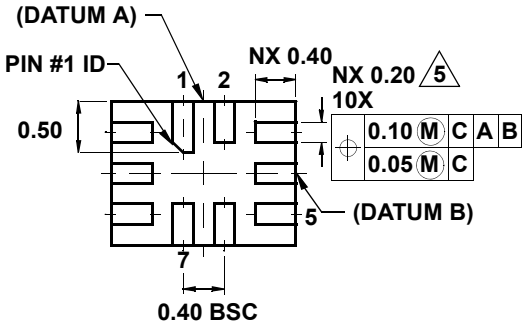
L10.1.8x1.4A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

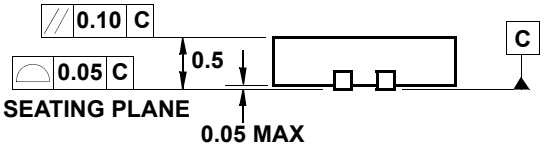
Rev 4, 9/09



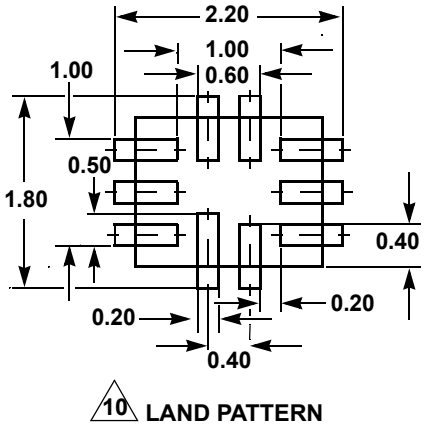
TOP VIEW



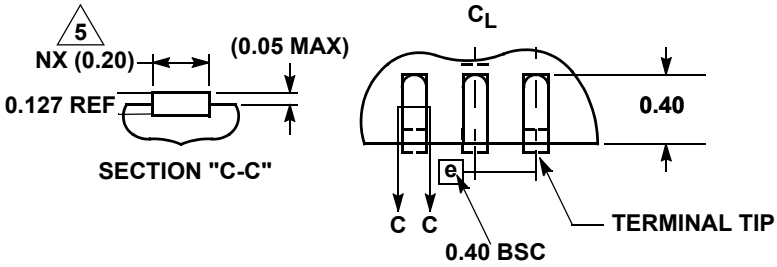
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals. Total 10 leads.
3. Nd and Ne refer to the number of terminals on D (4) and E (6) side, respectively.
4. All dimensions are in millimeters. Tolerances ±0.05mm unless otherwise noted. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.