General Description

The epc901 IC is a high-performance CCD line sensor capable of storing a total of 4 frames in the frame store elements for ultra high-speed image acquisition. The acquisition of the image is controlled by the external control signal SHUTTER. The epc901 flags when a frame is ready for read-out by asserting the DATA_RDY signal.
The transmission of the frame over the video amplifier is controlled by the external control signal READ. When a read-out is initiated by a pulse on the READ signal, it is sampled by a CDS stage. After a fixed delay the frame can be shifted out through the video amplifier by applying the appropriate amount of read clock edges.

The device offers various configuration options:

- Gain of the read-out stage selectable of 1, 2 or 4
- Transmission direction selectable
- Region of interest (ROI) centre region (pixel 256 to 767)
- Lateral binning of 2 or 4 pixels in order to reduce transmission time and noise
- Single- or multi-frame acquisition
- Clearing of frames stored and periodic flushing of pixel array to avoid blooming.

Features

- Photosensitive CCD array backside illuminated with 1024x1 pixel
- Very high frame rate of up to 50 kfps, in burst mode 500 kfps for 4 images (store up to 4 acquired images on-chip in charge domain)
- Very high sensitivity due to 100% fill factor and epc's unique OHC15L process technology
- Pixel size 7.5 x 120µm
- Correlated-double sampling (CDS) per pixel
- Single-ended or differential analog video output
- Simple 5-pin control interface for acquisition and read-out
- I2C bus interface
- Internal clock source, trimmable
- Two on-chip temperature sensors with 12 bit resolution
- Single supply voltage
- 32 Pin space saving CSP package
- Chip size L x W x T: 8.0 x 1.3 x 0.23 mm

Applications

- Linear and rotary encoder
- Triangulation light barrier / distance measurement
- Line sensor / camera
- Business card readers & portable scanners
- Multi-touch displays / electronic whiteboards
- Finger print readers
- Spectrometers
- Check & ticket readers
- Speed measurement
- Barcode readers

Block diagram

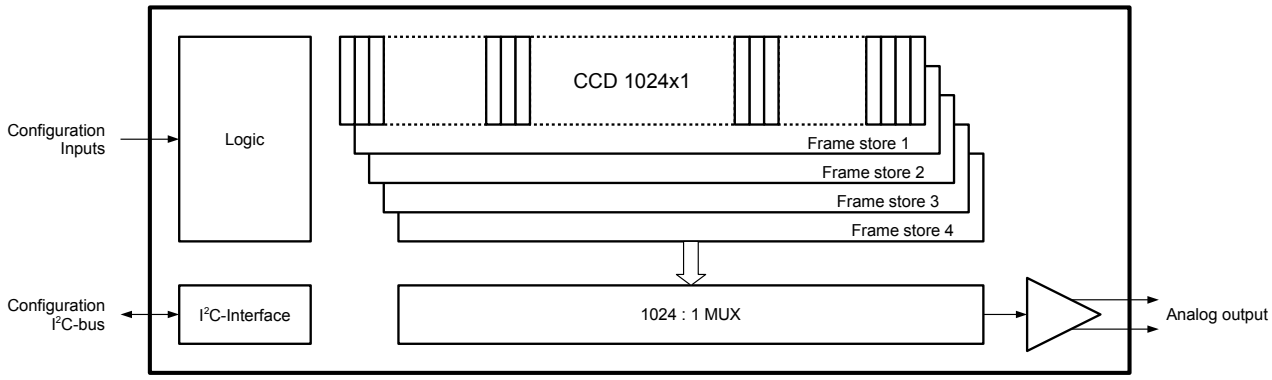


Figure 1: Top-level block diagram of the epc901 IC

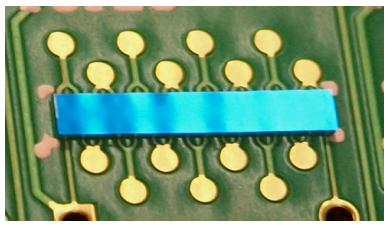


Figure 2: Picture of the epc901

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1. Block diagram

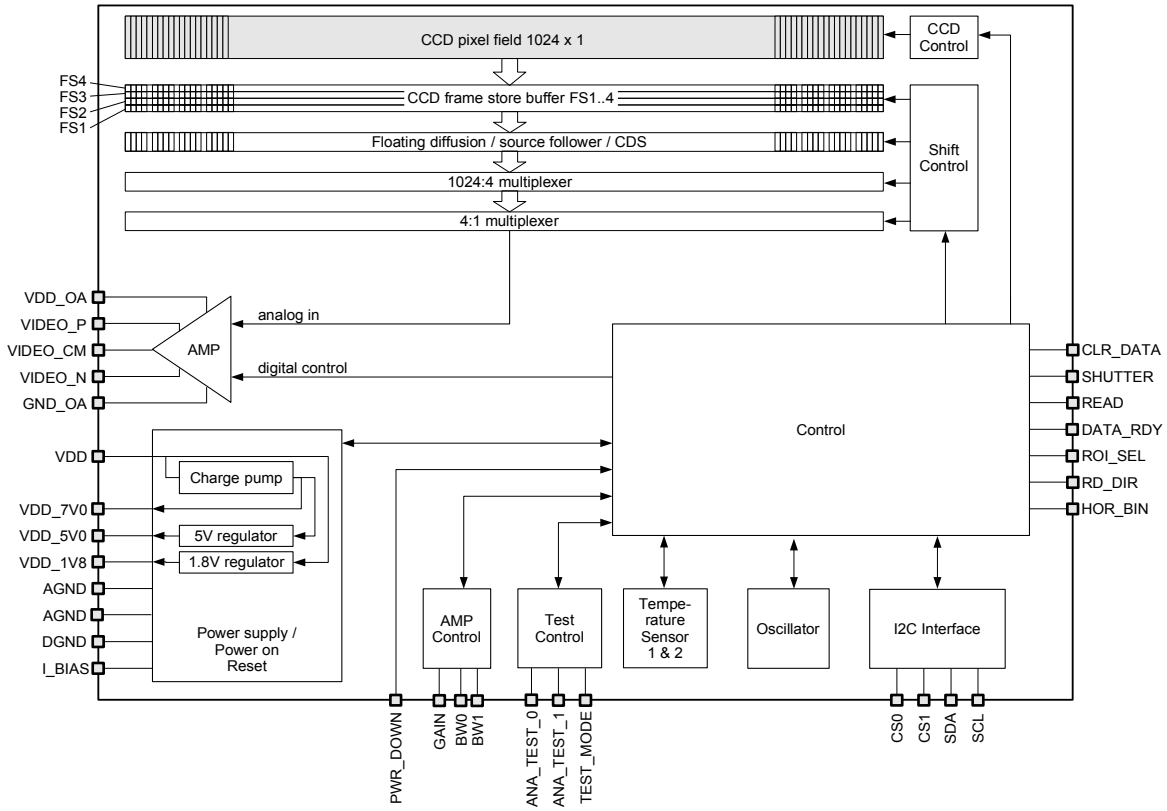


Figure 3: Block diagram

2. Pin-out

2.1. Pin assignment

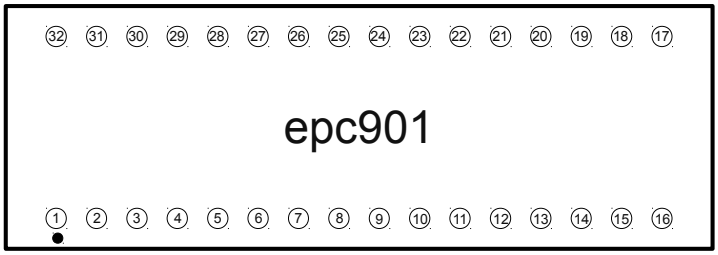


Figure 4: Pin-out of epc901 with view to the photo-sensitive side (top-view)

2.2. Pin table

Pin no.	Pin name	Pin type	Default [V]	Description
Digital pins				
2	PWR_DOWN	DI	0	Power-down mode enable
3	CLR_DATA	DI	0	Clear internal data memory controller
5	CLR_PIX	DI	0	Rising edge resets pixels and its controller
6	SHUTTER	DI	0	Exposure active when SHUTTER set
12	READ	DI	0	Read-out control and read clock
4	DATA_RDY	DO		Flag when data on video interface is ready. Used as a strap pin to turn on/off the charge pump
13	SDA	DIOD	VDD	I2C serial data (open drain)
14	SCL	DIOD	VDD	I2C serial clock (open drain)
15	ROI_SEL	DI	0	Region of interest selection
17	CS1	TER	VDD/2	I2C chip select 1
19	CS0	TER	VDD/2	I2C chip select 0
21	GAIN	TER	VDD/2	Select gain of read-out path
22	BW0	TER	VDD/2	LSB of bandwidth of video amplifier
23	BW1	TER	VDD/2	MSB of bandwidth of video amplifier
24	RD_DIR	DI	0	Read-out direction
25	HOR_BIN	TER	VDD/2	Horizontal binning selection
30	TEST_MODE	DI	0	Chip test
Analog pins				
8	VIDEO_N	AO		Negative terminal of video output
9	VIDEO_P	AO		Positive terminal of video output
11	VIDEO_CM	AI	VDD/2 or 0	Voltage to set video output common-mode
27	I_BIAS	AI		Bias current
28	ANA_TEST_1	AIO	0	Analog test in-/output 1
29	ANA_TEST_0	AIO	0	Analog test in-/output 0
Supply pins				
26	VDD	Supply		Positive chip supply voltage
10	VDD_OA	Supply		Positive supply of video amplifier
32	VDD_1V8	AO / Supply		Decoupling of digital partition
18	VDD_5V0	AO / Supply		Decoupling of CCD bias voltage, input is supplied externally (refer to 12.2.)
20	VDD_7V0	AO / Supply		Decoupling of charge pump
16	AGND	Supply		Analog ground
1	AGND	Supply		Analog ground
7	GND_OA	Supply		Video amplifier ground
31	DGND	Supply		Digital ground

Definitions:

- DI: Digital input pin, with an internal pull-down resistor of approx. 100-250kΩ
- DO: Digital output pin
- DIOD: General purpose bidirectional digital pin with open-drain output, requires external pull-up resistor
- AO: Analog output
- AI: Analog input
- AIO: Analog input and output
- TER: Ternary input pin, with a pull-down and an equal pull-up resistor of approx. 100-250kΩ which tie the pin to the VDD/2 state.

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2.3. Power domain separation and ESD protection

The epc901 chip has internally 5 different power domains and 3 ground references which are interconnected with ESD protection diodes. All pins are also equipped with ESD protection diodes. Figure 5 shows this functional circuit. The diodes have a breakthrough voltage of 0.3V. The designer has to take care that none of these diodes become conductive either at power-up, power-down or normal operation.

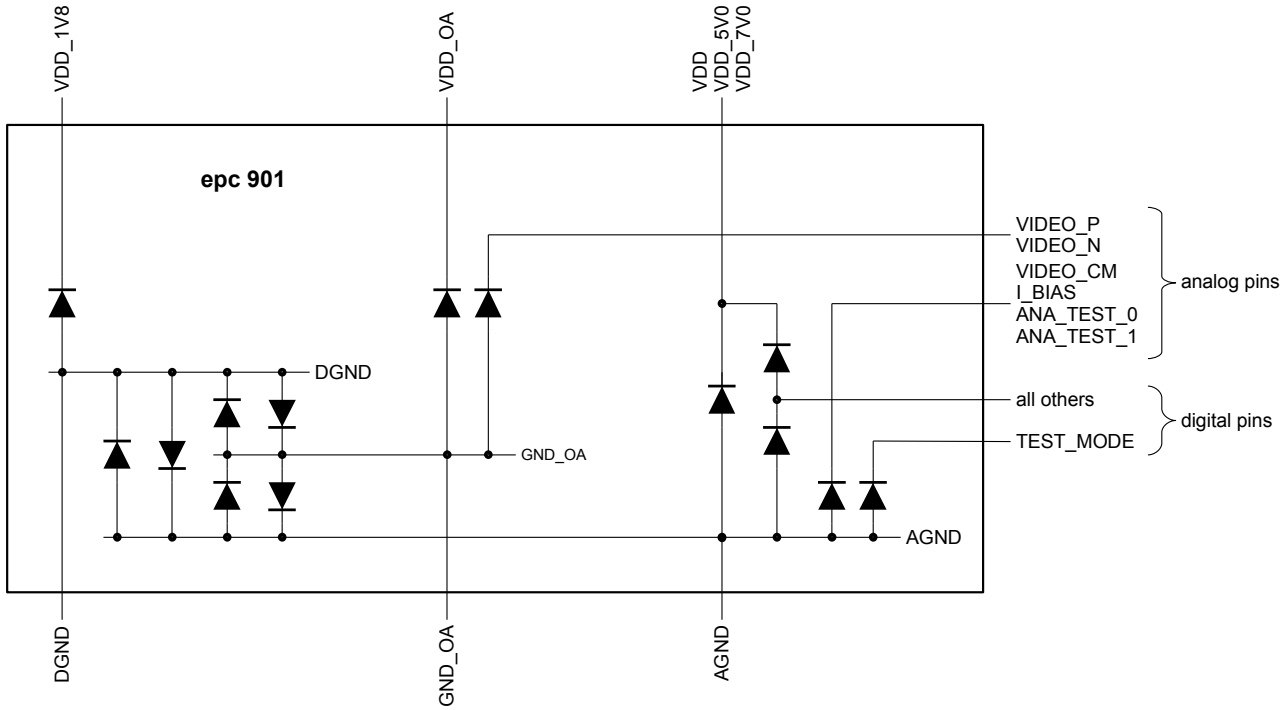


Figure 5: ESD protection diode circuit

3. Electrical, optical and timing characteristics

(T_A = 25°C, V_{DD} = 3.0V unless otherwise noted)

3.1. Recommended operating conditions

Parameter	Description		Min	Typ	Max	Unit
$V_{DD\ Nominal}$	Nominal supply voltage on VDD and VDD_OA		2.70	3.00	3.45	V
	Supply voltage on VDD and VDD_OA with Read Clock of max. 1 MHz.		2.45			
PSRR	Power supply rejection ratio VDD and VDD_OA.	Differential		13		dB
		Single ended		9		dB
T_J	Junction temperature range		-40		85	°C
$R_{th\ J\text{-}A}$	Thermal resistance junction - ambient			65		K/W

3.2. System characteristics

Parameter	Description	Min	Typ	Max	Unit
R_{VIDEO}	Frame rate on video output	1		50k	fps
$B_{3dB,VIDEO}$	3dB-bandwidth of video output @ C_{LVIDEO} = 40pF	10	11		MHz
B_{I2C}	I2C transmission rate			400	kbit/s

3.3. Electrical characteristics

Parameter	Description		Min	Typ	Max	Unit
$I_{DD}+I_{DD_OA}$ [1]	Total current consumption on pins VDD and VDD_OA (refer to section 12.)					
	Differential mode, full video bandwidth, 50kfps [2], Charge pump: ON Temperature sensors: ON	Idle mode (READ = L)		26	39	mA
		Peak, during read-out		48	72	mA
	Differential mode, full video bandwidth, 50kfps [2], external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF	Idle mode (READ = L)		10	15	mA
		Peak, during read-out		16	24	mA
	Differential mode, low video bandwidth, 1kfps [4], external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF	Idle mode (READ = L)		6.0	9.0	mA
		Peak, during read-out		6.0	9.0	mA
	Single-ended mode, low video bandwidth, 1kfps [4] Charge pump: ON Temperature sensors: ON	Idle mode (READ = L)		21	30	mA
		Peak, during read-out		40	60	mA
	Single-ended mode, low video bandwidth, 1kfps [4], external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF	Idle mode (READ = L)		5.0	10.0	mA
		Peak during read-out		5.0	10.0	mA
	Power-Save mode (POWR_DOWN = H, shutter still working), external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF			1.3	2	mA
	In-rush current at power-up during approximately 5ms Charge pump: ON			60	90	mA
	In-rush current at power-up during approximately 2ms, external VDD5V0 supply [3] Charge pump: OFF			50	75	mA
I_{DD_5V}	Current consumption on pin VDD_5V0 [3], Differential/single-ended mode, full video bandwidth, 50kfps [2] external VDD5V0 supply [3]) Charge pump: OFF			1.2	2.5	mA
V_{DIL}	Low voltage level on binary digital inputs [5] (Level L)				0.2*V_{DD}	V
V_{DIH}	High voltage level on binary digital inputs [5] (Level H)		0.5*V_{DD}			V
V_{DOL}, V_{TERIL}	Low voltage level on binary and ternary digital outputs (Level L)				0.2*V_{DD}	V

Parameter	Description		Min	Typ	Max	Unit
V_{DOH}, V_{TERIH}	High voltage level on binary and ternary digital outputs (Level H)		0.8*V_{DD}			V
V_{TERIM}	Centre voltage level on ternary digital inputs (Level M)		0.4*V_{DD}		0.6*V_{DD}	V
I_{DI}	Sink current at digital inputs				10	µA
R_{DI}	Internal pull-down resistor		100		250	kΩ
R_{TER}	Internal voltage dividing resistors which force the input to VDD/2		100		250	kΩ
I_{DO}	Sink / source current at digital outputs				3	mA
V_{VDD1V8}	Internally generated voltage on pin VDD1V8		1.62	1.8	1.98	V
V_{VDD5V0}	Internally generated voltage on pin VDD5V0		4.5	5.0	5.5	V
V_{DD7V0}	Internally generated voltage on pin VDD7V0		6.0	6.5	7.0	V
$V_{VIDEO_P,N}$	Voltage range at output of video amplifier (@ gain 1)		0.25		V_{DD}-0.25	V
V_{CM_SE}	Voltage at VIDEO_CM to select single-ended mode				0.4	V
V_{CM_D}	Common-mode voltage in differential mode, set on pin VIDEO_CM. Note: For V_{CM_D}>1V, differential mode is detected automatically by default. For V_{CM_D}<1V, differential mode has to be enabled by setting bit AMP_OVR in register FORCE_ANA_CTRL_SIGS (see section 10.3.)		0.5	V_{DD}/2	V_{DD}/2+0.1	V
$R_{IN,CM}$	Input resistance of VIDEO_CM		100			kΩ
$CMRR_{CM}$	Common-mode rejection ratio on VIDEO_CM (f ≥ 100 kHz)	100kHz … 50MHz		17		dB
		100kHz … 10Mhz		24		dB
$V_{OFF,VIDEO,CM}$	Common-mode offset of video amplifier output				±50	mV
$V_{OFF,VIDEO,SIG}$	Signal offset of video amplifier output				±100	mV
C_{LVIDEO}	Load capacitance on video output	single ended	5		100	pF
		differential	5		25	pF
$R_{INT,VIDEO}$	Output resistance of the video amplifier	single ended		32	100	Ω
		differential		11	100	Ω
R_{LVIDEO}	Load resistance on video output		3			kΩ

Notes:
[1] The current values change after the first Read Pulse after boot-up. The values here are after this first Read Pulse.
[2] Video amplifier BW = HIGH_BW, VIDEO_GBW_SEL_REG = 0x3.
[3] VDD5V0 has only to be supplied externally in case the charge pump is configured to be off. See section 12.2.
[4] Video amplifier BW = LOW_BW, VIDEO_GBW_SEL_REG = 0x0.
[5] I2C pins SCL and SDA are according to I2C standards

3.4. Temperature sensor characteristics

Parameter	Description	Min	Typ	Max	Unit
T_{TEMP}	Temperature measurement range	-40		+85	ºC
$OFFSET_{TEMP}$	Temperature sensor offset		-10.1·10[3]		LSB
$GAIN_{TEMP}$	Temperature sensor gain. The typical measured temperature value of e.g. the left temperature sensor can be calculated from the value of the sensor output registers TEMP_SENS_L_MSB and TEMP_SENS_L_LSB as follows: $T_{\mathrm{TEMP_L}} = \frac{\mathrm{TEMP_L}[12:0] - OFFSET_{TEMP}}{GAIN_{TEMP}}$ [ºK] Note: Values for $OFFSET_{TEMP}$ and $GAIN_{TEMP}$ are rough. For absolute measurements or precise relative measurements, calibration is required.	24	48	96	LSB/ºK
P_{TS}	Resolution of the temperature sensors		13		bits
N_{TEMP}	Noise		2	4	LSB
LIN_{TEMP}	Linearity of temperature sensors over the full temperature range		±2	±4	ºK
f_{TEMP}	Update rate of the temperature sensors (configurable)	0.1		10	Hz

3.5. Timing parameters

Parameter	Description		Min	Typ	Max	Unit
$T_{STARTUP}$	Start-up time after applying external supply/supplies (includes ramp-up of charge pump)				10	ms
T_{CP_UP}	Charge pump power-up time: time from changing the bit CP_PD from 1 to 0 until chip is operational (internal VDD5V)				5	ms
T_{WAKE_UP}	Wake-up time from Power-Save mode			7	12	µs
f_{OSC}	Oscillator clock frequency at nominal trim value (OSC_TRIM_REG at default value)	room temperature	22.4	36	48	MHz
		-20°C < T_A < 65°C	18	36	58	MHz
$f_{OSC_MAX_TRIM}$	Frequency of oscillator clock that can be achieved through trimming [3] at room temperature.		32			MHz
$T_{SU,CONF}$	Setup time of configuration pins with respect to rising edge of read pulse		50			ns
$T_{H,CONF}$	Hold time of configuration pins with respect to rising edge of read pulse		3			Oscillator clock cycles
$T_{SHUTTER}$	Pulse width of SHUTTER signal		5			Oscillator clock cycles
T_{FLUSH}	Flush period [1]		30		32	Oscillator clock cycles
T_{SHIFT}	Shift period [1]		24		26	Oscillator clock cycles
T_{RD_PULSE}	Pulse width of Read Pulse		3			Oscillator clock cycles
T_{CDS}	CDS operation				37	Oscillator clock cycles
T_{STORE}	Duration how long a frame may be stored in the frame-store		10			ms
T_{RD_CLK}	Period of the read clock		18.5		10'000	ns
f_{READ}	READ clock rate (the inverse of T_{RD_CLK}) [2]		0.1		54	MHz
D	READ clock duty cycle @ f_{READ} max		45	50	55	%
$T_{H,VIDEO}$	Period during which the output of the video amplifier is held stable after the last read clock edge			50		µs
$T_{PERIOD,FLUSH}$	Periodicity of the periodic flush operation [4]			100		ms
T_{PULSE,CLR_DATA}	Pulse width on CLR_DATA		3			Oscillator clock cycles
B_{I2C}	I2C transmission rate				400	kbit/s

Notes:
[1] By measuring the frequency of the internal clock oscillator (see section 9.), the duration of the internal flush and shift periods can be calculated exactly.
[2] To achieve the maximum clock frequency, the duty cycle of the read clock has to be 50% with a maximal tolerance of ±5%.
[3] The internal oscillator must not be trimmed to a frequency higher than 50MHz.
[4] Refer to section 5.6. for more details.

3.6. Absolute maximum ratings

Description	Conditions
Power supply voltage (VDD)	-0.3V to +5V
Voltage to any Pin	-0.3 to VDD +0.3V
Storage Temperature Range (T_S)	-40°C to +85°C
Relative humidity	0 to 95% non-condensing
ESD rating	all pins except VDD7V0 vs. VDD1V8: HBM class 2 (2kV to <4kV, JEDEC) Pin VDD7V0 vs. VDD1V8: HBM class 1B (500V to <1kV, JEDEC) Note: Pin VDD7V0 is in the final circuit loaded with 2.2µF low ESR capacitor.

3.7. Optical characteristics

(Gain 1, video bandwidth 1MHz, differential mode)

Parameter	Description		Min	Typ	Max	Unit
W_{PIX}	Width of pixels			7.5		µm
H_{PIX}	Height of pixels			120		µm
N_{PIX}	Number of pixels			1024		
N_{FS}	Number of frames stored on-chip (including the pixel array)			4		
FF	Optical fill factor in pixel array			100		%
CG	Conversion gain (standard version)		3	5	8	µV/e-
	Optical sensitivity (λ = 630 nm, gain = 1)			71		V/(Lux*s)
QE	Quantum efficiency (λ = 630 nm)			90		%
FW [4]	Full-well capacity per frame		400			ke-
N_{READ_D}	Read noise, differential mode, optimal settings [1]			700	1000	µVrms
N_{READ_SE}	Read noise, single ended mode, optimal settings [1]			500	700	µVrms
LIN	Linearity[2]	Differential mode		1.0	2.0	%
		Single-ended mode		2.0	4.0	%
I_{LAG}	Image lag @ max. Vpp and @ 400ke-	Single-frame acquisition (see section 5.2)			0.2	%
		Multi-frame acquisition (see section 5.3)			0.5	%
$\delta V_{DARK,PIX}$	Output voltage drift due to dark current in pixel area			1.0	10.0	V/s
$\delta V_{DARK,FS}$	Output voltage drift due to dark current in frame store area				0.3	V/s
Θ_{DARK}	Thermal drift of dark current		Doubles approx. every 8°K			
PRNU[3]	Photo response non-uniformity (@ 0.5*FW[4])			2		%
DSNU[3]	Dark pixel non-uniformity @ T_{EXP} = 100 µs			±0.3		% FW
M_{FW}	Irradiance to generate FW electrons per pixel in 1 ns (λ = 630 nm)			155		mW/mm^2
	Surface reflectivity (@ 550 to 860 nm, 90° incident angle)			2		%
	Surface reflectivity (@ 550 to 860 nm, 60° incident angle)			4		%
	Pixel cross-talk (@ 630nm, 90° incident angle)			20		%
	Cross-talk width @ 1σ			4		µm

Table 1: Optical specification

Notes:

[1] Charge pump off, temp sensor off, video amplifier BW=LOW_BW, VIDEO_GBW_SEL_REG=0x0 (minimum video amplifier bias current, Read Clock 1MHz).

[2] The linearity is defined as the maximum deviation of the pixel responses between 10% and 80% FW[4] from the straight line between 10% and 80% FW[4]. Pixels with high dark current excluded.

[3] Pixel 3 .. 1020

[4] FW corresponds to 2V swing at the output in differential mode.

3.7.1. Typical spectral range and quantum efficiency (QE)

The following diagrams show the quantum efficiency as a function of wavelength. The curve is a measurement where the chip has a wide-range anti-reflection coating which is optimized at 650 nm.

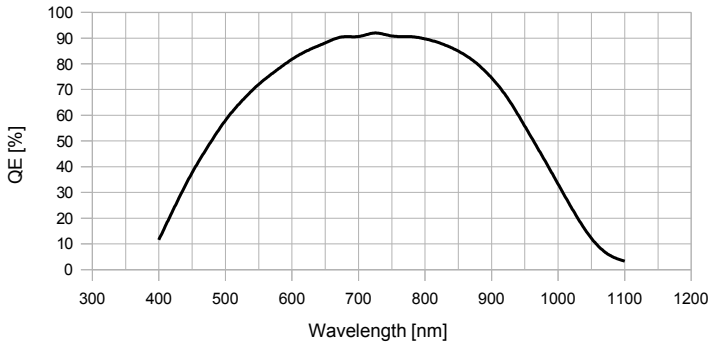
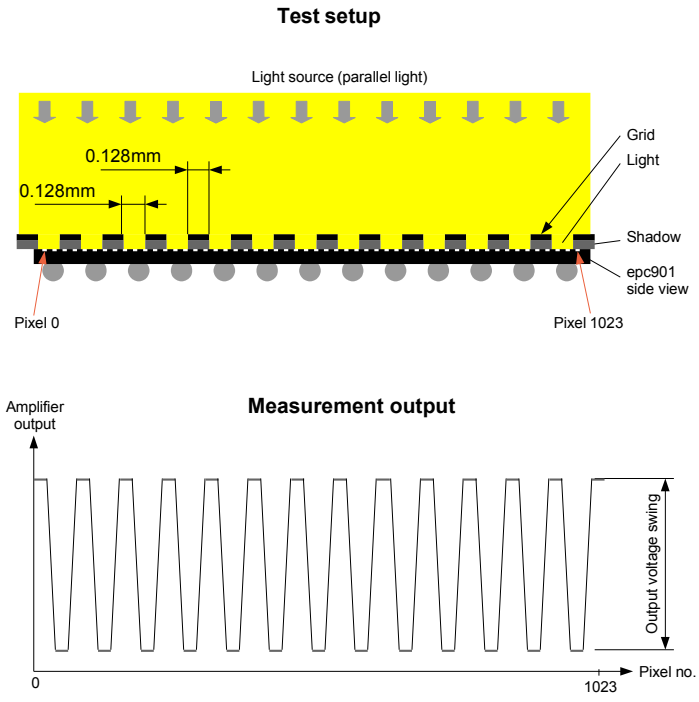


Figure 6: Quantum efficiency as a function of wavelength

3.8. Frequency response

The signal amplitude at the output of the video amplifier is a function of the optical modulation and the read-out clock frequency. The optical modulation is defined as follows:



The amplitude at the video amplifier output as a function of the Read Clock frequency is as follows (temperature sensor off, differential mode):

Read Clock frequency	Mode	BW (video amplifier bandwidth setting)	VIDEO_GBW_SEL_REG	GAIN	Min. useful signal swing	SNR typ. (charge pump off)		SNR typ. (charge pump on)		Useful pixel range [1]
						min	typ	min	typ	
1MHz	Differential	LOW_BW	0x0	1	2.0Vpp	66dB	70dB	65dB	67dB	3..1020
10MHz	Differential	HIGH_BW	0x3	1	1.5Vpp	55dB	58dB	53dB	55dB	3..1020
54MHz	Differential	HIGH_BW	0x3	1	0.5Vpp	46dB	49dB	44dB	46dB	3..1020
54MHz	Differential	HIGH_BW	0x3	2	0.75Vpp	46dB	49dB	42dB	46dB	3..1020
54MHz	Differential	HIGH_BW	0x3	4	1.25Vpp	46dB	49dB	42dB	46dB	3..1020
1MHz	Single-ended	LOW_BW	0x0	1	1.6Vpp	67dB	70dB	N/A	N/A	3..1020

Table 2: Useful video amplifier signal swing and SNR for different settings

Note:
[1] For the ROI_SEL=H, the read-out region as defined in Table 5 is the useful pixel range

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4. Chip configuration

The epc901 IC can be configured either by the configuration pins or through I2C commands. At power-up or software reset, the status of the configuration pins are read and used to operate the chip. The configuration can later on be changed with I2C commands (refer to Table 9). Make sure that the bit RD_CONF_CTRL is set properly.

4.1. Configuration pin description

Pin Name	Low (GND)	High-Z	High (VDD)	Comments
RD_DIR	Pixel 0 .. 1023		Pixel 1023 .. 0	
ROI_SEL	Pixel 0 .. 1023		Pixel 256 .. 767	Readout region of the pixel array
Gain	2	1	4	Multiplier for the conversion gain
HOR_BIN	2 pixel	1 pixel	4 pixel	Defines horizontal binning. Binning here means averaging over 2 or 4 pixels in the voltage domain (not charge domain!) e.g. for HOR_BIN=H, pixels 0..3, 4..7, 8..11 etc. are averaged as follows $V_{\text{BINNING_BY_4}}[i]=\frac{V[i]+V[i+1]+V[i+2]+V[i+3]}{4}$, i = 0, 3, 7, .., 1020 Binning can be used to reduce the read-out time by the binning factor. Note: Binning 2 (HOR_BIN = 0) is not applicable for single-ended mode.
VIDEO_CM	Single ended	Differential	n/a	Refer also to section 11.1. Circuit for differential mode
DATA_RDY	Charge pump on	N/A	Charge pump off	Refer to section 4.3.

BW0		X		Max. video bandwidth (referred to as 16MHz, see section 4.4. Frequency response setting)
BW1		X		

BW0			X	High video bandwidth (referred to as 8MHz)
BW1	X			

BW0	X			Low video bandwidth (referred to as 4MHz)
BW1			X	

BW0			X	Min. video bandwidth (referred to as 1MHz, see section 4.4. Frequency response setting)
BW1			X	

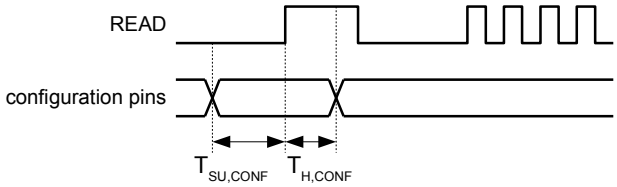
Table 3: Configuration pin description

Notes:

- The shaded values are recommended for typical and easy to use applications.
- The bandwidth of the video amplifier (configured through BW and VIDEO_GBW_SEL_REG) affects the current consumption of the chip and the noise at the output. The lower the bandwidth the lower the noise and the lower the current consumption. Thus, it is a good concept to keep the bandwidth as low as possible.
- The configuration pins are read into the registers ACQ_TX_CONF_EFF and BW_VIDEO_CONF_EFF (and become effective) upon reset (i.e. power-up or software reset). In case RD_CONF_CTRL is left at default setting 0 (see Table 9), the configuration pins are also read upon the rising edge of READ (refer to section 5.4.).
- The re-sampled values of the configuration pins take effect immediately if the configuration is controlled by the configuration pins.
- The configuration set by the configuration pins can be overwritten by writing to the registers ACQ_TX_CONF and/or BW_VIDEO_CONF through I2C (see section 10.). The overwrite functionality has to be enabled by setting RD_CONF_CTRL=1 (see Table 9).
- The CS0 and CS1 pin configuration are described in section 10.1.1. Device addressing.

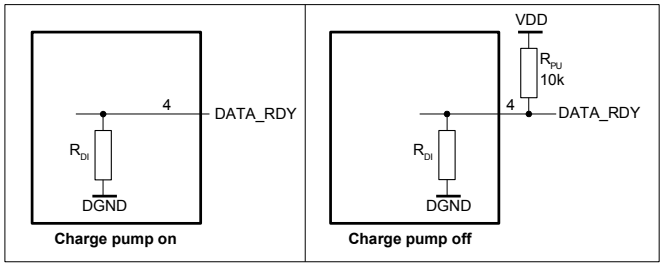
4.2. Dynamic change of the configuration pins

If the configuration pins shall dynamically be changed in the application, the setup and hold time as shown in the diagram below have to be used for a safe operation of the IC.



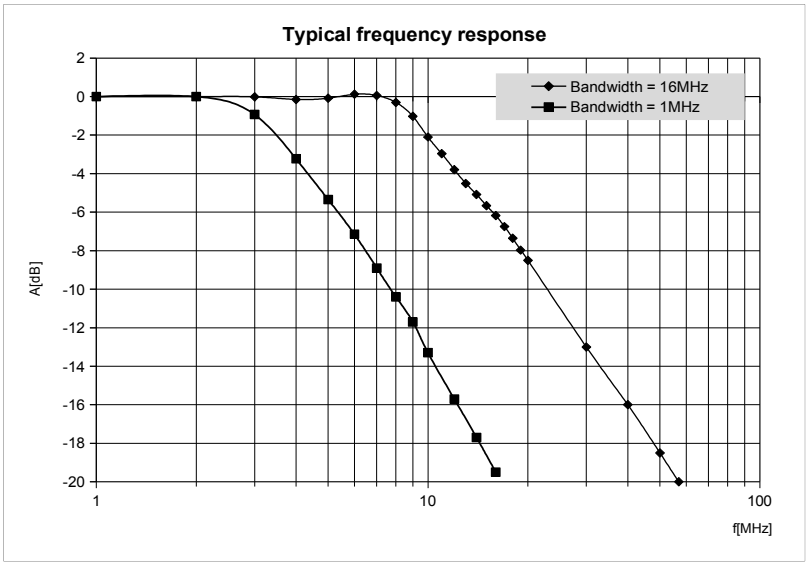
4.3. Charge pump on/off through DATA_RDY strap pin

The DATA_RDY pin is used as a strap pin to enable/disable the charge pump. At power-up, the voltage level on DATA_RDY is checked. In case of a logic-low level, which is set by the internal pull-down resistor, the charge pump is on by default. In case of a logic-high level, which can be set by an external 10k pull-up resistor, the charge pump is off by default (see figure below).



4.4. Frequency response setting

The following Bode plot shows the typical frequency response of the readout chain, according to the settings of the configuration pins BW0 and BW1, refer to section 4.1. Configuration pin description and Table 7.



5. Imager operation

5.1. General remarks

The epc901 line imager chip is based on a backside illumination technology (BSI). The image is taken from the backside of the chip, whereas the electrical circuits and the pins are on the frontside. Thus, the chip must be flip-chip mounted to the PCB in order to expose the backside to the incoming light.

It is not possible with BSI to shield the photosensitive area with an integrated, electrically controlled shutter when there no light shall be detected. In other words, the pixel CCD is continuously photo-sensitive and collects charge generated by the detected photons (unwanted exposure). Thus, the CCD must be flushed or erased by the unwanted charge before an image can be acquired.

READ Pulse - The pulse applied to pin READ_CLK to initiate the read-out of a frame.
READ Clock - The clock applied to pin READ_CLK to read out the frame (after the Read Pulse).

5.2. Image acquisition

After the exposure time defined by the user, the charge collected in the CCD has to be shifted into an area which is not photo-sensitive. This area is called frame store. The shift process samples the charge collected by the CCD in the frame store. The following diagram shows this operation.

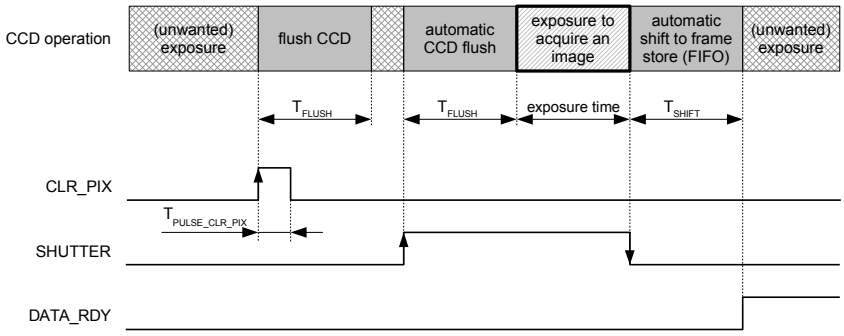


Figure 7: Image acquisition timing

The acquisition of a frame is controlled by a pulse on pin SHUTTER (see Figure 7). The rising edge of a pulse on SHUTTER triggers the internal flush operation to erase the CCD from any unwanted electrons prior to the exposure. The exposure starts automatically after the flush operation is completed. The CCD collects electrons thereafter as long as the SHUTTER pin is high. Upon the falling edge of SHUTTER, the charge collected in the CCD pixel field is automatically shifted to the CCD frame store which is a photo-insensitive area (see (1) in Figure 8). As soon as the frame is ready for read-out, the signal DATA_RDY goes high. The image is ready to be readout as described in section 5.4..

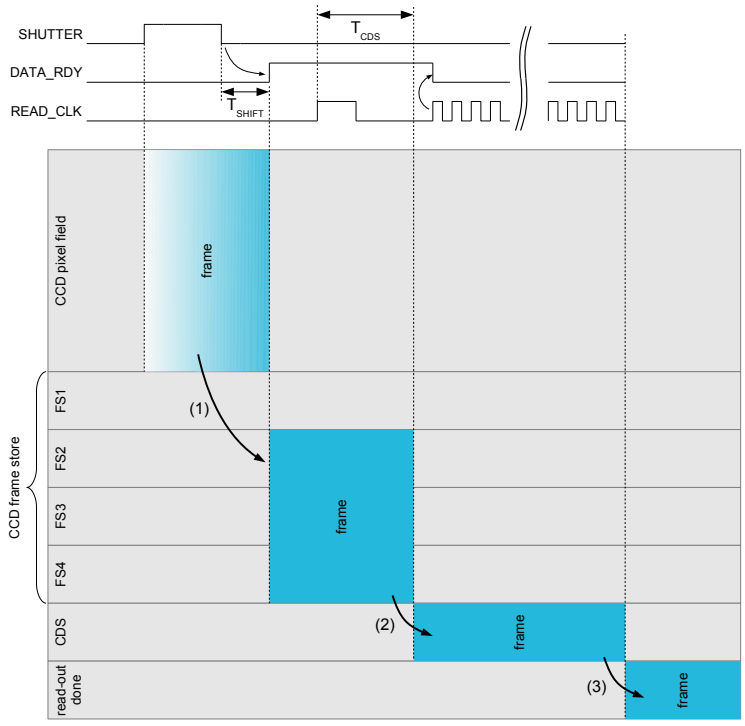


Figure 8: Illustrative example of single-frame acquisition and read-out

It is to note that the CCD continues to be photo-sensitive during the shift operation i.e. for a time T_{SHIFT} after the falling edge of SHUTTER.

5.3. Multi frame acquisition

Up to 4 images can be acquired and stored in the CCD frame store in a fast sequence without intermediate read-out. The CCD frame store is organized in 4 CCD frame store elements (FS1-FS4), thereby each CCD frame store element can store one frame/image. The first captured image initially occupies 3 frame store elements as for a single-frame acquisition (see section 5.2 and Figure 8). epc901 automatically detects a multi-frame acquisition when detecting the second SHUTTER signal without prior read-out. Upon the second shutter the first image is shifted to a single frame store element (see (2) in Figure 9). The frames are shifted from the CCD pixel field to and through the CCD frame store in a FIFO-manner i.e. the first captured image is the first one read out. The read-out is described in more detail in section 5.4. As soon as 4 frames have been captured without prior read-out, at least one read-out has to be issued prior the next shutter in order to make FS1 available again. Excessive shutter pulses are ignored.

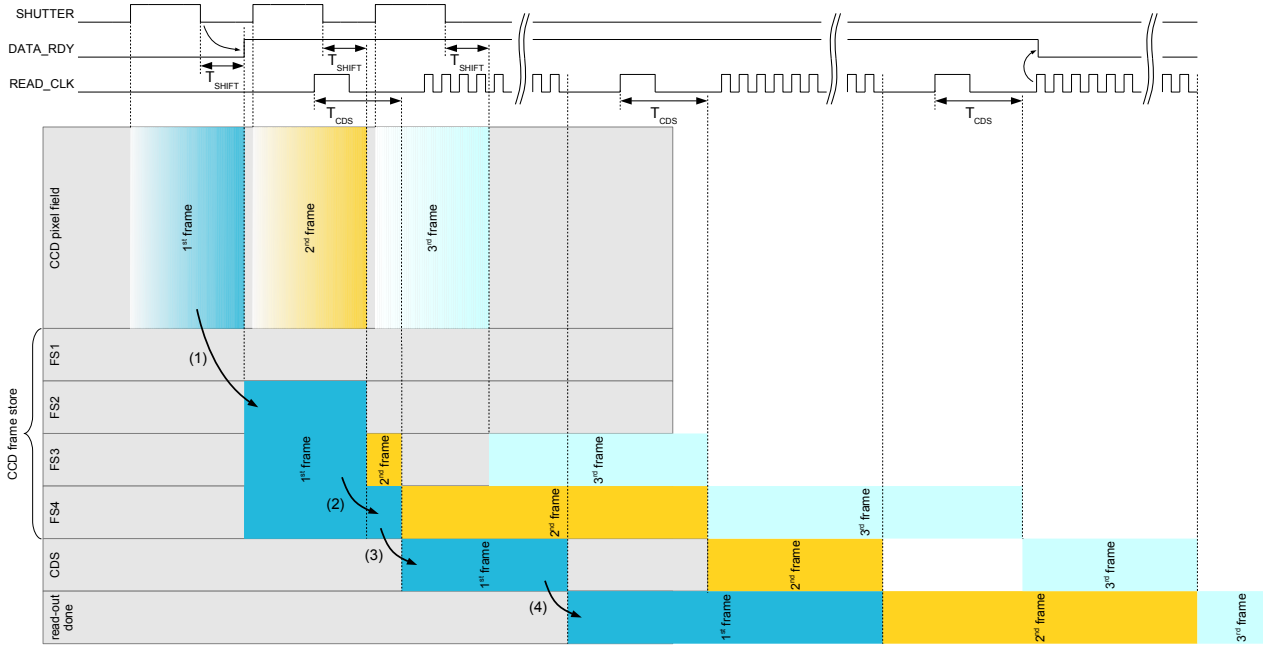


Figure 9: Illustrative example of multi-frame acquisition and read-out

5.4. Image readout

After one or more images have been captured, the first image (FIFO) can be read out through the video interface on the pins VIDEO_P and VIDEO_N. The read-out is controlled by the READ pin. The following timing diagram shows its usage:

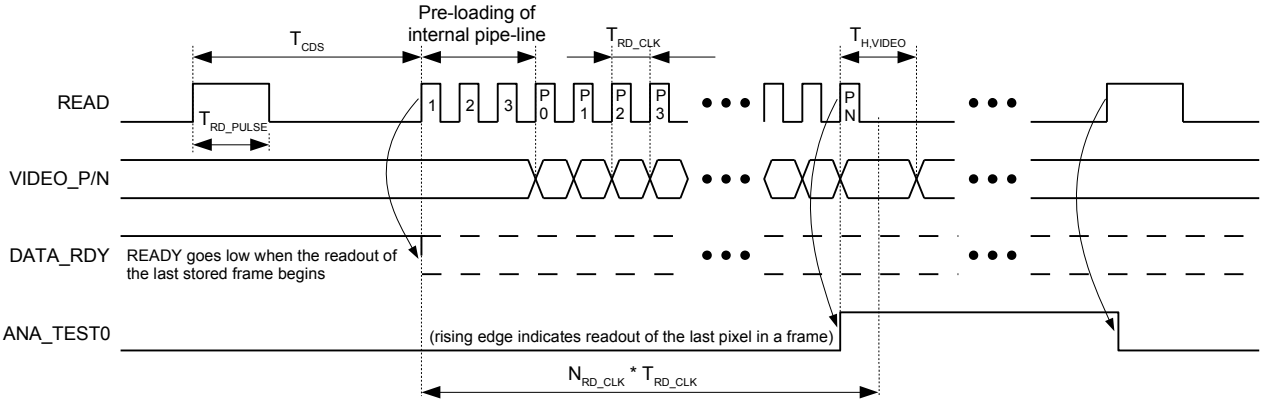


Figure 10: Image readout timing of one frame

The first pulse of a read sequence applied to pin READ is a Read Pulse and must have a duration of T_{RD_PULSE}. Upon a Read Pulse, the last frame in the CCD frame store is sampled pixel-wise onto a capacitor array thereby the pixel charges are converted into pixel voltages

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according to the specified conversion gain (CG). This operation is called correlated double-sampling (CDS) and lasts for the time T_{CDS} (refer also to the block diagram in Figure 3 or Table 10). Following the Read Pulse, respecting a delay of at least T_{CDS}, Read Clock pulses are applied to the READ pin in order to transfer the pixel voltages to the VIDEO_P/N pins. The first 3 Read Clock pulses, designated with 1, 2 and 3 in Figure 10, are used to pre-load the pipeline. Thus the first 3 pixel voltage values on VIDEO_P/N can be ignored. The subsequent Read Clock pulses, designated with P0 ... PN in Figure 10, transfer the pixel voltage values through the video amplifier to the VIDEO_P/N pins.

After all pixels are read out, the output of the video amplifier is held stable for a time $T_{H,VIDEO}$ or until the next Read Pulse, whatever occurs first. The transmission of the last pixel is indicated by a high state of the pin ANA_TEST0 upon the last Read Clock pulse rising edge. ANA_TEST0 goes low again upon the following rising edge at READ.

Any subsequent pulse of duration T_{RD_PULSE} is interpreted as a Read Pulse and thus a new read-out sequence is initiated.

The signal DATA_RDY remains high as long as there is at least one frame stored in the CCD frame store. If no more frames are stored except the one that is currently read out, the signal DATA_RDY goes to low state on the first positive Read Clock edge (see Figure 10). If no frame is stored, the chip does nothing upon a Read Pulse.

IMPORTANT

- It is important to sample the analog output signal of the vide amplifier just before the rising edge of the next read pulse. This time point allows the readout circuits and the video amplifier to be fully settled. Also at this time point, the lowest possible readout noise can be achieved.
- The following time periods shall never overlap in any multi frame acquisition or by parallel reading during exposure: T_{FLUSH} with T_{CDS} and T_{SHIFT} with T_{CDS}. Refer for these signal to Figure 7 and Figure 10.

5.5. Readout configuration

Read-out can be configured through the configuration pins (see section 4.1). Depending on binning and ROI selection, different numbers of pixels are available for read-out. E.g. if binning of 2 is selected, only 512 values can be read out because always two pixels are binned. Thus, only 512 + 3 Read Clock pulses must be applied in this example. The following table shows the number of Read Clock pulses according to the configuration:

ROI_SEL pin	HOR_BIN pin	Number of Read Clock pulses N_{RD_CLK}
L	L	512+3
L	M	1024+3
L	H	256+3
H	L	256+3
H	M	512+3
H	H	128+3

Table 4: ROI_SEL/HOR_BIN settings

5.6. Periodic flushing

As explained in section 5.2., the imager is photosensitive all the time. So it constantly converts incoming light into charge. If the pixel field (the CCD) is not flushed periodically, excessive charge can be generated which may spill over from the pixel field to neighboring circuits, e.g. the frame store buffers. Thus, periodic flushing by applying a CLR_PIX pulse during the time no images are acquired is highly recommended, at least with a periodicity of $T_{PERIOD,FLUSH}$ (refer to section 3.5.). However, the need to do so depends on how much light is received and how long is the time between two SHUTTER pulses.

For a given application, it is a good idea to evaluate the setup first before the system software is implemented. During evaluation, one measure of the charge generated in the pixel by applying a SHUTTER signal with the length of the time between the intended acquisition of two images shall be executed. If the maximal pixel value exceeds 90% of full well (= 90% of output swing), it is highly recommended to place additional CLR_PIX pulses during the time where no image acquisition takes place.

A pulse on SHUTTER is ignored if it is issued within T_{FLUSH} after the rising edge of CLR_PIX. If a rising edge on CLR_PIX occurs while SHUTTER is high or during the subsequent internal shift period T_{SHIFT}, the pulse on CLR_PIX is ignored.

In power-down mode, the CCD is not photo-sensitive and therefore no charge is collected. However, the transition from power-down mode to operation flushes the CDD and the frame store automatically.

5.7. Clearing the CCD pixel field and the CCD frame store with CLR_DATA

The frames stored in the CCD pixel field and the CCD frame store can be erased simultaneously by a pulse on CLR_DATA with a minimum pulse width of T_{PULSE,CLR_DATA}. The clear operation is triggered by the rising edge of CLR_DATA. After the CCD frame store and the CCD pixel field are cleared, the chip is ready to acquire new images.

A rising edge on CLR_DATA also aborts an on-going read-out and a new image acquisition can be initiated immediately. As long as DATA_RDY is not asserted (upon the new image acquisition), the read-out of the frame in the CDS can be continued without any impact on the frame (for multi-frame operation see section 5.3)

A rising edge of CLR_DATA during a shift operation might be ignored and is therefore to avoid. It is allowed to assert SHUTTER and CLR_DATA at the same time.

Please note that the frame store buffers also collect charge even if there is no operation with the CCD. This is due to dark current which can also flow into the frame store buffer elements. Thus, the frame store buffer should also be cleared (erased) regularly if there is no acquisition and readout within 100ms.

6. Temperature sensor

There are two temperature sensors on the IC, one on each side of the pixel array. They are turned off by default and can be turned on through I2C (see Table 18). The temperature sensors just provide raw values which are off by an offset ($OFFSET_{TEMP}$) and a gain ($GAIN_{TEMP}$) from the measured absolute temperature value. Thus calibration is mandatory to enable absolute temperature measurements. Calibration can take place during manufacturing of the system by applying one or two reference temperature/s and storing the calibration value in a non-volatile memory e.g. in the µC.

The digitized output of the temperature sensors can be read through the I2C interface registers TEMP_SENSE* (refer to Table 15 … Table 18). As soon as one of these addresses is read, the update of these registers with new temperature values is blocked until all four registers are read. The sequence in which these registers are read, is not important.

7. Power-down mode

The chip can be forced into power-down mode to reduce the power consumption.

PWR_DOWN	Description
L	Operation
H	Power-down mode activated

If the chip is forced to power-down while frames are still stored on the IC, these frames are lost with power-down. When PWR_DOWN is asserted during an acquisition or transmission, the current operation is finished before the chip goes to power-down. When the power-down mode is de-activated, the IC typically needs T_{PWR_UP} to be back in functional mode. When PWR_DOWN goes to low state, the pixel array is it automatically flushed. In the power-down mode, no charge is collected by the CCD.

8. Chip reset

The digital control unit of the epc901 IC can be reset by the following mechanisms:

- Disconnecting and reconnecting the power supply
- Reset command through I2C (software reset)

9. Measuring the internal oscillator clock frequency

The epc901 chip has an internal oscillator which controls the operation of the chip. The typical frequency is approx. 35MHz but it has a significant tolerance (refer to chapter 3.5, Timing parameters), as well as a temperature drift. To measure this frequency in order to apply an optimized timing, the following procedure can be used:

1. Apply CLR_DATA
2. Apply SHUTTER for longer than T_{FLUSH}, e.g. 1µs
3. Measure the time from the falling edge of SHUTTER until the rising edge of DATA_RDY (T_{SHIFT})

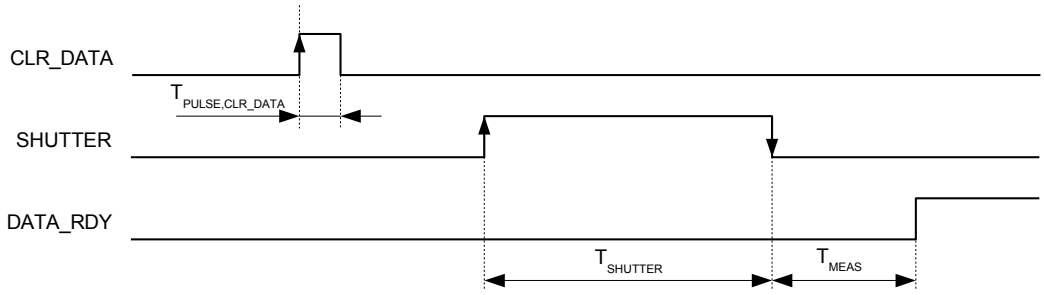


Figure 11: Sequence to measure internal clock frequency

Since T_{SHIFT} needs 24 to 26 clock cycles (n * ClockCycles), the frequency of the internal oscillator can be calculated according to the following formula:

$$F_{OSC} = \frac{n * ClockCycles}{T_{MEAS}}$$

E.g. if the measured time is 600ns, the oscillator frequency is between 40 and 43.3MHz. If the clock frequency shall be acquired more accurate, multiple measurements of T_{MEAS} shall be acquired and the average of these samples shall be used in the above formula. The clock frequency can be trimmed by setting a configuration register according to the description in Table 11 and 12.

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10. I2C interface

The epc901 supports the following functions by using the I2C interface:

- Fast I2C (400 kBit/s)
- 7-bit addressing
- Slave (epc901 is always the slave)
- Supported functions are software reset, read, write, read the device address

Clock stretching and other uses of I2C bus are not supported. The register list which can be accessed by the I2C interface are listed in section 10.3. All registers can be accessed directly except the test mode registers.

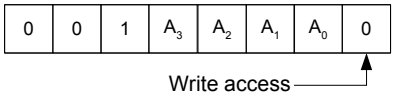
10.1. I2C communication

10.1.1. Device addressing

The MSBs of the device address are fixed to '001' internally, the LSBs A_3 to A_0 can be set by the two ternary input pins CS0 and CS1.

		CS0		
		L	M	H
CS1	L	0000	0001	0011
	M	0100	0101	0111
	H	1100	1101	1111

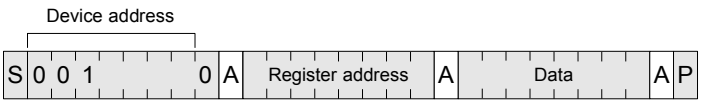
The LSB of the device addressing is used to select the communication direction:



The bus protocol in the following sections uses the following notation:

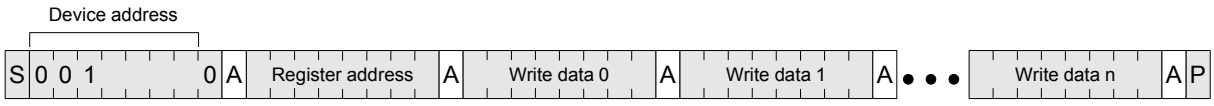
Symbol	Function
S	START
P	STOP
A	ACK
N	NACK
Shaded	Master
Unshaded	Slave (epc901

10.1.2. Single-byte write



10.1.3. Multi-byte write

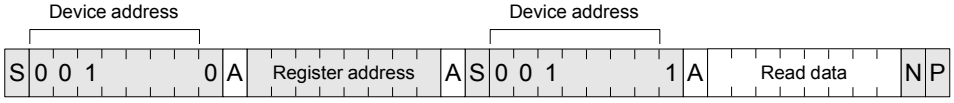
During a multi-byte write operation the master transmits the device address and the address of the first register to be written. All subsequent bytes until STOP are interpreted as write data packets.



Registers reside in a non-consecutive address space. Writing to a unused address will fail silently (no error feedback).

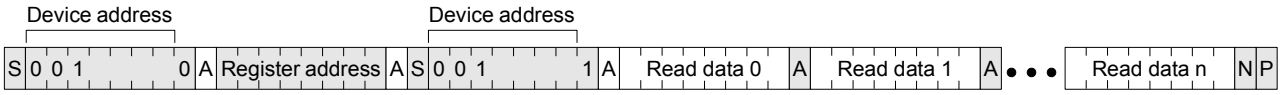
10.1.4. Single-byte read

During a single-byte read, only one register is read. After the device address is transmitted, the master has to transmit the register address. After addressing the epc901 IC with a read-command, it transmits the read data. The access is terminated with a NACK and a STOP by the master.



10.1.5. Multi-byte read

During a multi-byte read operation the master transmits the device address and the address of the first register to be read. Afterwards, the epc901 is addressed with a read command. It then transmits data bytes until the master applies NACK and a STOP.



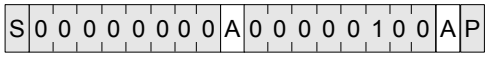
Registers reside in a non-consecutive address space. Reading to a unused address will return no useful data.

10.1.6. Software reset



A software reset has the same effect like a power-up reset. E.g. the chip uses the configuration as given by the configuration pins. Also, all trimming parameters are reset to the initial values.

10.1.7. Re-sampling the device address



By applying this command, the pins CS0 and CS1 are read and updated in the internal address register.

10.2. Setup latency

The new register value becomes active with the falling edge of the last bit transmitted.

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10.3. I2C register description

Address	Register name	Ref.	Description
Configuration			
0x00	ACQ_TX_CONF_I2C	Table 6	Acquisition and transmission configuration Use this register to overwrite the values set by the corresponding configuration pins (see Table 2 or Table 3). Make sure RD_CONF_CTRL is set to 1. In this case ACQ_TX_CONF_I2C is copied to ACQ_TX_CONF_EFF at the rising edge of Read Pulse.
0x01	BW_VIDEO_CONF_IC2	Table 7	Bandwidth control of the video amplifier Use this register address to overwrite the values set by the corresponding configuration pins (see Table 2 or Table 3). Make sure RD_CONF_CTRL is set to 1. In this case BW_VIDEO_CONF_IC2 is copied to BW_VIDEO_CONF_EFF at the rising edge of Read Pulse.
0x02	MISC_CONF	Table 8	Miscellaneous configuration
0x03	ACQ_TX_CONF_EFF	Table 6	Acquisition and transmission configuration (effective register) The values for this register are read in from the configuration pins as long as RD_CONF_CTRL is set to 0 Do not write to this register through I2C, use ACQ_TX_CONF_I2C instead.
0x04	BW_VIDEO_CONF_EFF	Table 7	Bandwidth control of the video amplifier (effective register) The values for this register are read in from the configuration pins as long as RD_CONF_CTRL is set to 0 Do not write to this register through I2C, use BW_VIDEO_CONF_IC2 instead.
Trimming			
0x90	OSC_TRIM_REG	Table 11	Oscillator trimming
0x91 … 0x93	reserved	n/a	
0x94	VIDEO_GBW_SEL_REG	Table 13	Tuning of the gain-bandwidth product of video amp
Temperature sensors			
0xA0	TEMP_SENS_L_LSB	Table 15	Least-significant byte of left sensor's raw temperature value
0xA1	TEMP_SENS_L_MSB	Table 16	Most-significant byte of left sensor's raw temperature value
0xA2	TEMP_SENS_R_LSB	Table 17	Least-significant byte of right sensor's raw temperature value
0xA3	TEMP_SENS_R_MSB	Table 18	Most-significant byte of right sensor's raw temperature value
0xA4	TEMP_SENS_CONF	Table 19	Configure behavior of temperature sensor
Error indicators (read-only)			
0xB0	I2C_ERROR_IND	Table 22	Error indicator of the I2C interface
Analog test mode registers (see also section 15.)			
0xD0	ANA_TEST_MODE_EN_0	n/a	Enable register for analog test mode
0xD1	ANA_TEST_MODE_EN_1	n/a	Enable register for analog test mode
0xD2	ANA_TEST_CTRL	n/a	Test mode control register
0xD3	ANA_TEST_CONF	n/a	Configuration for the analog test modes
0xD4	ANA_TEST_MUX_0_SEL	n/a	Selection register for MUX on pin ANA_TEST_0
0xD5	ANA_TEST_MUX_1_SEL	n/a	Selection register for MUX on pin ANA_TEST_1
0xD6	FORCE_ANA_CTRL_SIGS	Table 23	Force power-down of charge pump and pixel bias voltage regulator
0xD7	OSC_TRIM_RANGE_REG	Table 10	Oscillator trimming - set oscillator trim range (available from chip revision number 0x14 i.e. epc901_020)
Debug read-only registers			
0xF0 … 0xFE	reserved	n/a	
0xFF	CHIP_REV_NO_REG	Table 25	Identifier register for chip revision number

Table 5: Register map accessible by the I2C interface

In the tables below, the operations defined are:

R Read

W Write

WP Writeable with protection

C Automatic synchronous clear operation after read access

ACQ_TX_CONF_I2C / ACQ_TX_CONF_EFF								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	HOR_BIN		GAIN		ROI_SEL	RD_DIR
Operation	n/a	n/a	R/W		R/W		R/W	R/W
Default	n/a	n/a	0x1		0x1		0	0

Table 6: Description of register ACQ_TX_CONF_I2C, ACQ_TX_CONF_EFF

HOR_BIN: Horizontal binning of the pixels:

00: Binning 2 pixels (in differential mode only, not applicable in single ended mode)

01: No binning

10 or 11: Binning 4 pixels

GAIN: Video amplifier voltage gain

00: 2

01: 1

10 or 11: 4

ROI_SEL: Region of interest

0: All pixels (0 to 1023)

1: Inner half of the pixels (256 to 767)

RD_DIR: Read direction

0: From 0 to 1023

1: From 1023 to 0

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BW_VIDEO_CONF_I2C / BW_VIDEO_CONF_EFF								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	BW_VIDEO_1		BW_VIDEO_0	
Operation	n/a	n/a	n/a	n/a	R/W		R/W	
Default	n/a	n/a	n/a	n/a	0x1		0x1	

Table 7: Description of register BW_VIDEO_CONF_I2C, BW_VIDEO_CONF_EFF

BW_VIDEO_1, BW_VIDEO_0:	1000 or 1100:	Low video bandwidth (referred to as 4 MHz, see section 4.4.)
	1010 or 1111:	Min. video bandwidth (referred to as 1 MHz, see section 4.4.)
	0101 or others:	**Max. video bandwidth (referred to as 16 MHz, see section 4.4.)**
	0010 or 0011:	High video bandwidth (referred to as 8 MHz, see section 4.4.)

MISC_CONF								
Bit no.	7	6	5	4	3	2	1	0
Bit name	SC_CMFB_EN	n/a	n/a	n/a	n/a	VIDEO_AMP_PD_OVR_EN	VIDEO_AMP_PD_OVR	RD_CONF_CTRL
Operation	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default for versions < -032 Default from version -032	0 1	0 0	0 0	1 1	1 1	0 0	0 0	0 0

Table 8: Description of register MISC_CONF

Register Name	Description	1	0
SC_CMFB_EN	Disabled: Video amplifier to use continuous-time common-mode feedback Enabled: Video amplifier to use switched-capacitor common-mode feedback Note: This bit has to be enabled in conjunction with enabling bit AMP_PHY_IDLE_EN in register FORCE_ANA_CTRL_SIGS (see Table 23)	enabled	**disabled**
n/a	n/a; do not change	n/a	**default**
n/a	n/a; do not change	n/a	**default**
n/a	n/a; do not change	**enabled**	disabled
n/a	n/a; do not change	**enabled**	disabled
VIDEO_AMP_PD_OVR_EN	Enable/disable whether the register bit VIDEO_AMP_PD_OVR is effective	enabled	**disabled**
VIDEO_AMP_PD_OVR	Video amplifier power down. This bit is only effective if register bit VIDEO_AMP_PD_OVR_EN is set	Video amp off	**Video amp on**
RD_CONF_CTRL	Selects the control of the configuration	Use configuration registers	**Use configuration pins**

Table 9: Description of register setting MISC_CONF

OSC_TRIM_RANGE_REG								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	OSC_TRIM_RANGE_UP
Operation	n/a	n/a	n/a	n/a	n/a	n/a	n/a	R/W
Default	n/a	n/a	n/a	n/a	n/a	n/a	n/a	0

Table 10: Description of register OSC_TRIM_RANGE_REG (available from revision number 0x14)

OSC_TRIM_RANGE_UP Defines oscillator trim range:

0: default oscillator trim range (as on chip revisions epc901_018 and epc901_019)

1: oscillator frequency increased by 25%

The bit OSC_TRIM_RANGE_UP can be regarded as an additional oscillator trim bit providing a course frequency trim step of +25%. For fine trimming use the bits OSC_TRIM as described hereafter.

OSC_TRIM_REG								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	OSC_TRIM			
Operation	n/a	n/a	n/a	n/a	R/W			
Default	n/a	n/a	n/a	n/a	0x0			

Table 11: Description of register OSC_TRIM_REG

The trim range of OSC_TRIM is approx. 1.2MHz per step:

Bit no.				Trim Value (MHz)
3	**2**	**1**	**0**	
1	0	0	0	-9.6
1	0	0	1	-8.4
1	0	1	0	-7.2
1	0	1	1	-6.0
1	1	0	0	-4.8
1	1	0	1	-3.6
1	1	1	0	-2.4
1	1	1	1	-1.2
0	**0**	**0**	**0**	**0 (center frequency)**
0	0	0	1	+1.2
0	0	1	0	+2.4
0	0	1	1	+3.6
0	1	0	0	+4.8
0	1	0	1	+6.0
0	1	1	0	+7.2
0	1	1	1	+8.4

Table 12: Oscillator trimming

VIDEO_GBW_SEL_REG								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	n/a	n/a	GBW_SEL_DI	
Operation	n/a	n/a	n/a	n/a	n/a	n/a	R/W	
Default	n/a	n/a	n/a	n/a	n/a	n/a	0x3	

Table 13: Description of register VIDEO_GBW_SEL_REG

The bandwidth of the video amplifier is tunable in four steps. The goal of a reduction in bandwidth is a lower current consumption. Tuning of the bandwidth can be achieved through the bandwidth selection register in Table 13. The value map of the bandwidth tuning is listed in Table 14.

VIDEO_GBW_SEL	Approximate relative video amplifier bandwidth	Video amplifier bias current [uA]
00	25%	1.25
01	50%	2.50
10	75%	3.75
11	100%	5.00

Table 14: Bandwidth selection and bias current trimming

The temperature sensors measure the change of the temperature with the specified precision P_{TS}.

TEMP_SENSE_L_LSB								
Bit no.	7	6	5	4	3	2	1	0
Bit name	TEMP_L[7:0]							
Operation	R							
Default	0x0							

Table 15: Description of register TEMP_SENSE_L_LSB

TEMP_L: Temperature of the left temperature sensor (LSB), located near pixel 0.

TEMP_SENSE_L_MSB								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	TEMP_L[12:8]				
Operation	n/a	n/a	n/a	R				
Default	n/a	n/a	n/a	0x0				

Table 16: Description of register TEMP_SENSE_L_MSB

TEMP_L: Temperature of the left temperature sensor (MSB), located near pixel 0.

TEMP_SENSE_R_LSB								
Bit no.	7	6	5	4	3	2	1	0
Bit name	TEMP_R[7:0]							
Operation	R							
Default	0x0							

Table 17: Description of register TEMP_SENSE_R_LSB

TEMP_R: Temperature of the right temperature sensor (LSB), located near pixel 1023.

TEMP_SENSE_R_MSB								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	TEMP_R[12:8]				
Operation	n/a	n/a	n/a	R				
Default	n/a	n/a	n/a	0x0				

Table 18: Description of register TEMP_SENSE_R_MSB

TEMP_R: Temperature of the right temperature sensor (MSB), located near pixel 1023.

TEMP_SENS_CONF								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	MEAS_RATE_CONF		ENABLE_R	ENABLE_L	PD_CONF_R	PD_CONF_L
Operation	n/a	n/a	R/W		R/W	R/W	R/W	R/W
Default for versions < -031 Default from version -031 [1]	n/a n/a	n/a n/a	0x0 0x0		1 0 [1]	1 0 [1]	0 1 [1]	0 1 [1]

Table 19: Description of register TEMP_SENS_CONF

Note:
[1] From version 031, the temperature sensors are turned off by default

Register Name	Description	1	0
MEAS_RATE_CONF	Configure the measurement rate of the temperature sensors: **00: 10 measurements per second** 01: 1 measurement per second 10: 1 measurement every 10 seconds **Note:** A change of the measurement rate becomes effective only after the temperature sensor has been disabled and enabled again.		
ENABLE_R	See Table 21		
ENABLE_L			
PD_CONF_R			
PD_CONF_L			

Table 20: Description of register setting TEMP_SENS_CONF

ENABLE_R	ENABLE_L	PD_CONF_R	PD_CONF_L	Description	Comment
0	**0**	**1**	**1**	**Both sensors off**	Default setting from version 031
1	1	0	0	Both sensors on	Default setting up to version 023
1	0	0	1	Only right sensor on	
0	1	1	0	Only left sensor on	

Table 21: Enable/disable temperature sensors

I2C_ERROR_IND								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	I2C_ERR
Operation	n/a	n/a	n/a	n/a	n/a	n/a	n/a	R/C
Default	n/a	n/a	n/a	n/a	n/a	n/a	n/a	0

Table 22: Description of register I2C_ERROR_IND

I2C_ERR Read/clear bit is set when the configuration controller fails to service a register read (or write) operation in due time. When this happens, the affected read operation may return wrong data, and the affected write operation may be ignored.

FORCE_ANA_CTRL_SIGS [1]								
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	AMP_PHY_IDLE_EN	n/a	AMP_OVR_EN	AMP_OVR	VDD5V0_PD	CP_PD
Operation	R/WP	R/WP	R/WP	R/WP	R/WP	R/WP	R/WP	R/WP
Default Default from version 032	0 0	0 0	0 1	0 0	0 0	0 0	0 0	0 0

Table 23: Description of register FORCE_ANA_CTRL_SIGS

Register Name	Description	1	0
AMP_PHY_IDLE_EN [1]	This bit has to be enabled in conjunction with enabling bit SC_CMFB_EN in register MISC_CONF (see Table 8)	enabled	**disabled**
n/a	n/a, do not change	enabled	**disabled**
AMP_OVR_EN [1]	Control the override of the mode selection in the video amplifier by the register bit AMP_OVR	enabled	**disabled**
AMP_OVR [1]	Override of the mode selection in the video amplifier. Takes only effect if register bit AMP_OVR_EN is is high.	Differential mode	**Single-ended mode**
VDD5V0_PD [1]	Force powering down the 5V regulator	Power down	**Regulator running**
CP_PD [1]	Force powering down the charge pump	Power down	**Charge pump running**

Table 24: Description of register setting FORCE_ANA_CTRL_SIGS

Notes:
[1] In order to gain write access to the register FORCE_ANA_CTRL_SIGS, write the following sequence into the chip first:
- Address 0xD0:ANA_TEST_MODE_EN_0 = 0x4a
- Address 0xD1:ANA_TEST_MODE_EN_1 = 0x66

[2] By default, FORCE_ANA_CTRL_SIGS is write-protected.

CHIP_REV_NO_REG								
Bit no.	7	6	5	4	3	2	1	0
Bit name	CHIP_REV_NO							
Operation	R							
Default	see Table 26							

Table 25: Description of register CHIP_REV_NO_REG

Reading this address returns a hard-coded value which is individual for each variant starting from X1023. For X1021, the value is hard-coded to 0x1 for all variants. The value in the config block is automatically read after the reset is released. The read can be forced by writing any data to the register CHIP_REV_NO_REG.

The values assigned are listed in Table 26.

Reticle identifier	Tape-out date	CHIP_REV_NO
X1021	04.12.12	0x1
X1023	15.02.2013	0x07, 0x0E, 0x0F, 0x12
X1024_000	23.12.2013	0x12, 0x13
X1024_001	06.06.2014	0x14, 0x15
X1024_002	24.09.2014	0x16, 0x17
epc901_000	20.03.2015	0x15, 0x1F
epc901_002	12.08.2015/09.10.2015	0x20

Table 26: List of chip identifiers for major revisions of IC

10.4. I2C bus timing

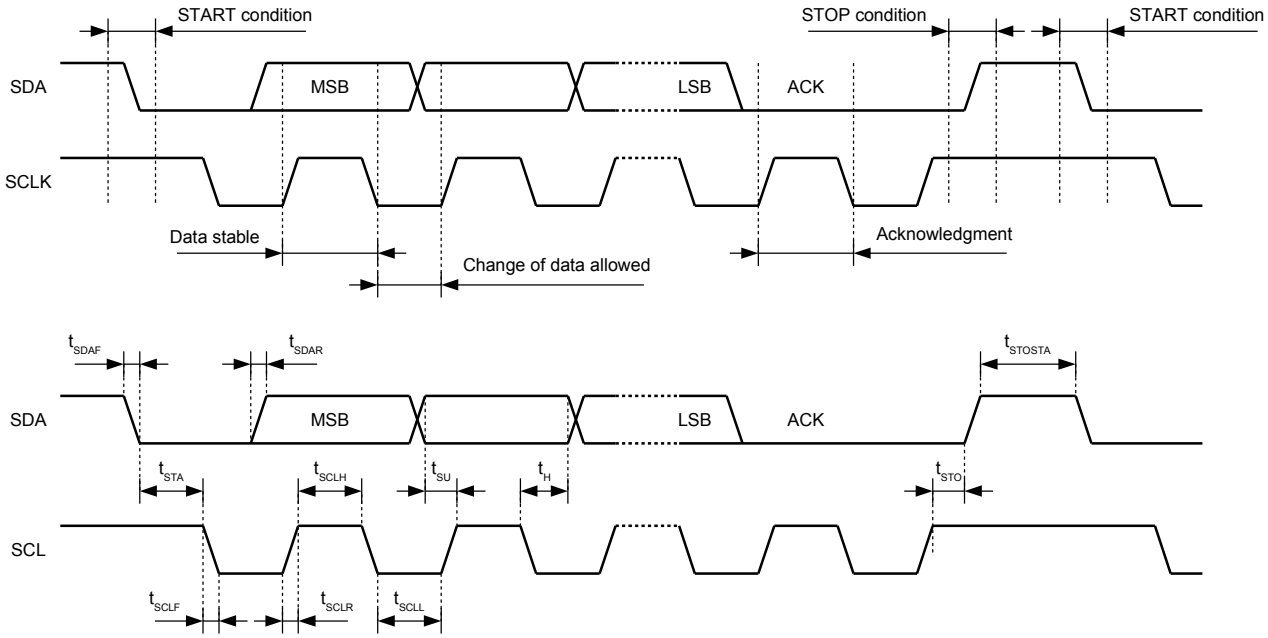


Figure 12: I²C bus timing, top: Basic communication sequence, bottom: Timing parameters

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	I²C data rate		400	kbit/s
t_{SCLL}	SCL clock low time	1.3		µs
t_{SCLH}	SCL clock high time	0.6		µs
t_{SU}	SDA setup time	100		ns
t_H	SDA hold time		0	ns
t_{SDAR} t_{SCLR}	SDA and SCL rise time		300	ns
t_{SDAF} t_{SCLF}	SDA and SCL fall time		300	ns
t_{STA}	Start condition hold time	0.6		µs
t_{STO}	Stop condition setup time	0.6		µs
t_{STOSTA}	Stop to start condition time (bus free)	1.3		µs
C_b	Capacitive load for each bus line		400	pF
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter		50	ns

Table 27: I²C bus timing: Timing parameters (FM+)

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11. Application information

Referring to Figure 13 and Figure 14, please note the following:

- The different GND pins can be connected together, preferably to a plane / star connection. Refer also to section 13.3.1.
- The video amplifier has separate supply pins VDD_OA and GND_OA due to its fast switching currents. It is important to block this power supply pins with low ESR capacitors as close as possible at the chip in order to avoid noise at the video output due to supply voltage bouncing.
- The voltage level applied to VDD_OA must be the same as on pin VDD. Otherwise the IC can be damaged due to latch-up.
- If the pin VIDEO_CM is left open (not connected), the video amplifier operates in differential mode. If this pin is tied to ground, together with the pin VIDEO_N, the video amplifier operates in single ended mode.

Video amplifier operation mode	VIDEO_P	VIDEO_N	VIDEO_CM
Differential	Positive output	Negative output	(not connected)
Single ended	Output	GND	GND

11.1. Circuit for differential mode

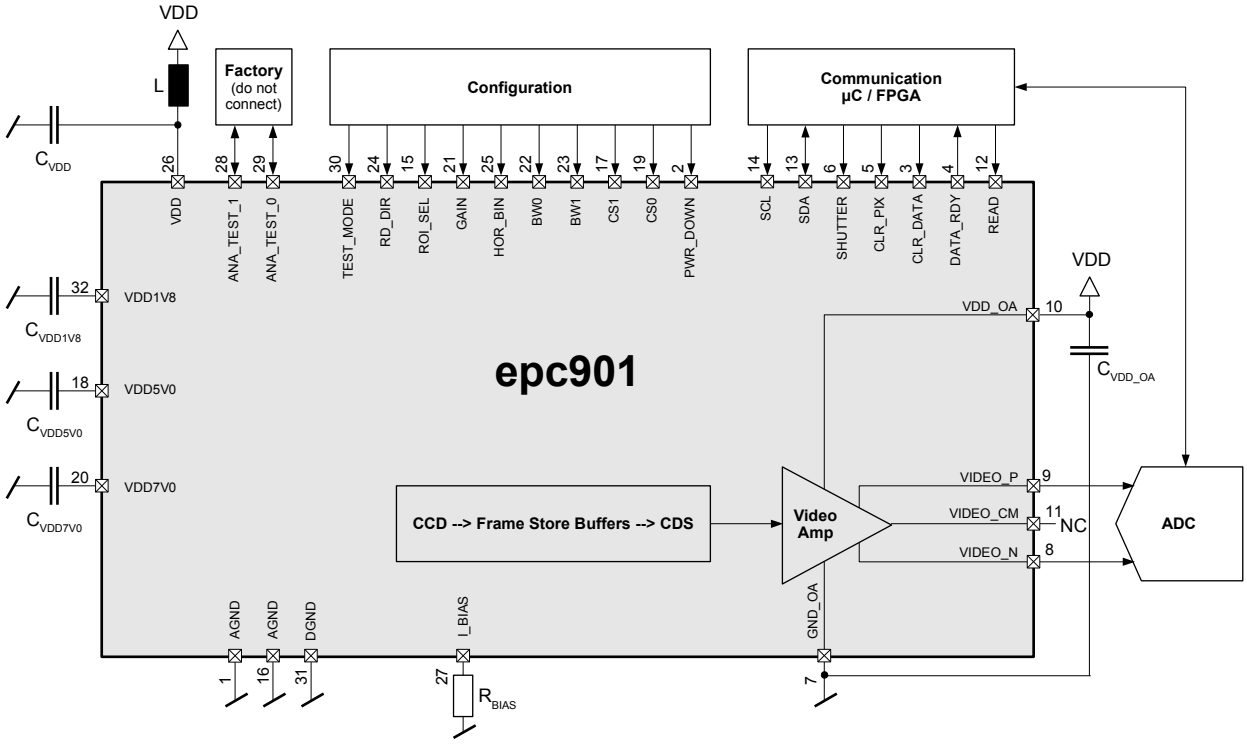


Figure 13: Differential mode application diagram

Please note that pin 11 can be left open in this operating mode. The IC sets this pin to VDD/2 which is the offset voltage of the VIDEO_P and VIDEO_N signal. However, it is possible to apply a voltage source at VIDEO_CM to control the common mode voltage of the output signal. Make sure that this is a low noise/low ripple source and add a 1µF low ESR blocking capacitor as close as possible to pin 11. In addition to that, the voltage at VIDEO_CM must be as defined in the table under section 3.3.Electrical characteristics V_{CM_D}.

Illumination	VIDEO_N	VIDEO_P	VIDEO_P – VIDEO_N (typ.)
Dark voltage	V_{VIDEO_CM} + 0.4V	V_{VIDEO_CM} – 0.4V	-0.8V
Maximum video output	V_{VIDEO_CM} – 0.6V	V_{VIDEO_CM} + 0.6V	1.2

Table 28: Video amplifier output in differential mode

11.2. Circuit for single ended mode

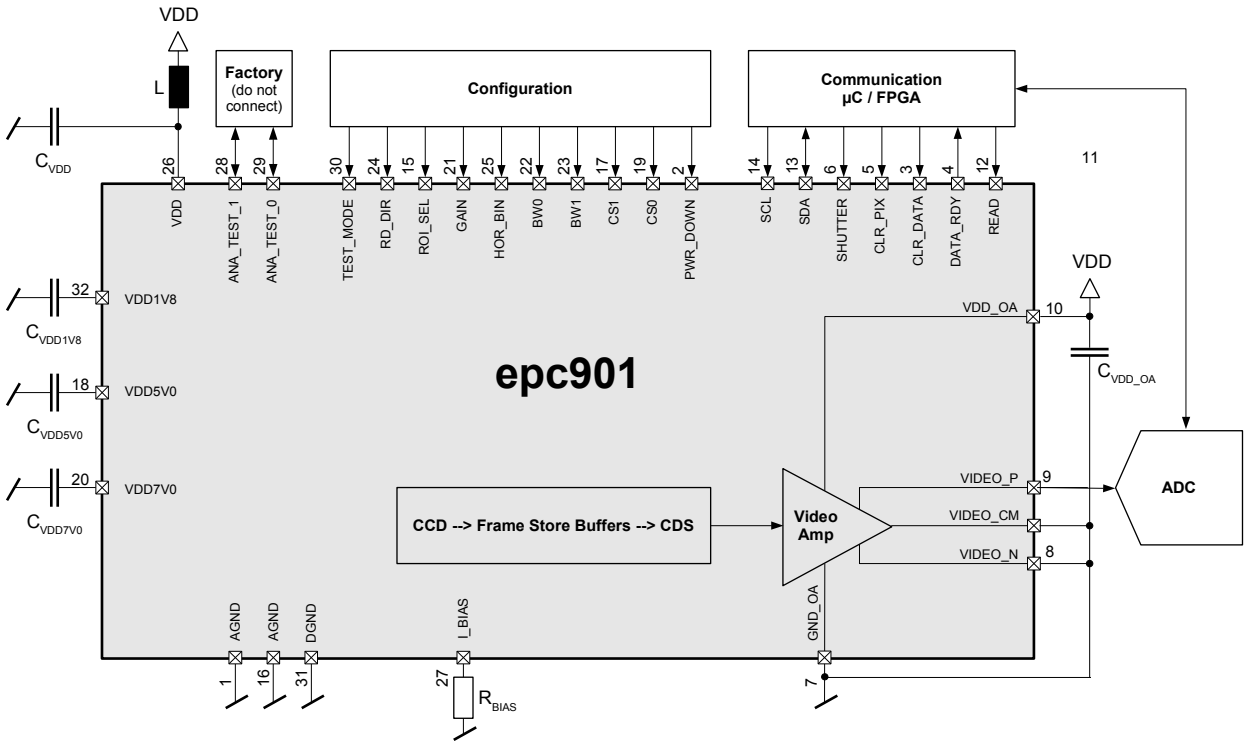


Figure 14: Single ended mode application diagram

In single-ended transmission mode, VIDEO_N and VIDEO_CM must be tied to ground. The output signal is available at VIDEO_P.

Illumination	VIDEO_P (typ.)
Dark voltage	0.4V
Maximum video output	2.0V

Table 29: Video amplifier output in single-ended mode

11.3. External components

The external components in Figure 13 and Figure 14 shall be as follows:

Parameter	Description	Value	Units	Tolerance	Comments
R_{BIAS}	External resistor defining the bias current	56k	kΩ	±1%	Resistance temperature coefficient max. ±100ppm/K
C_{VDD1V8}	Decoupling capacitor for VDD1V8	1.0	µF	±20%	low ESR
C_{VDD5V0}	Decoupling capacitor for VDD5V0	2.2	µF	±20%	low ESR
C_{VDD7V0}	Decoupling capacitor for VDD7V0	2.2	µF	±20%	low ESR
C_{VDD}	Decoupling capacitor for VDD	1.0	µF	±20%	low ESR
C_{VDD_OA}	Decoupling capacitor for VDD_OA	1.0	µF	±20%	low ESR
L	Decoupling inductor	600	Ω		e.g. Taiyo Yuden BK1005HR601-T

11.4. Low noise operation

11.4.1. Charge pump noise

The internal charge pump generates considerable noise, especially in single-ended mode. The noise performance can be optimized by turning off the charge pump and supplying the chip with an external 5V supply. Refer to section 12.2..

11.4.2. Video amplifier noise

Another noise source is the video amplifier which can be used in two different modes. Single ended mode is the lower noise operation mode. Thus, use the chip in single ended mode for low noise applications.

12. Power consumption considerations

12.1. General considerations

There are several options to control the power consumption. However, a tradeoff between performance and power consumption has to be considered. The following section describes the various options. The most power-consuming blocks are

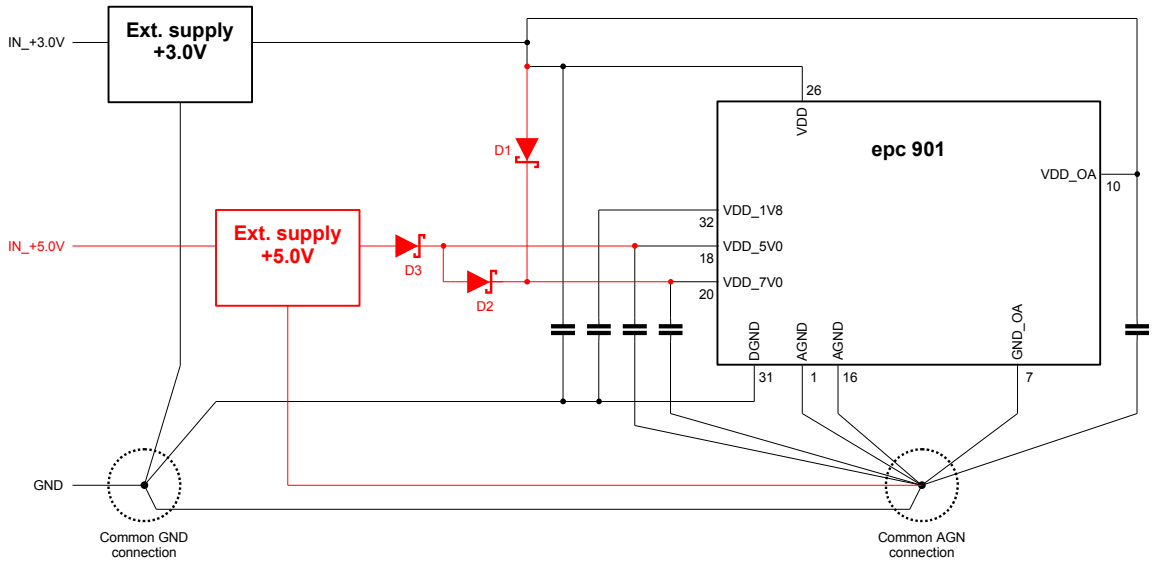
- Temperature sensors (approx. 3mA)
- Video amplifier (approx. 3.5mA)
- Charge pump and 5V regulator (approx. 13.5mA)

The wake-up time of the video amp is typ. 3µs only. Thus, in most applications it can be turned off during illumination in order to reduce the average power consumption.

12.2. Low power operation with external 3V and 5V supply

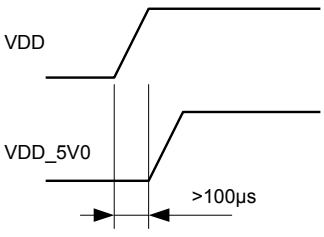
The lowest possible power consumption of the epc901 can be achieved if it is supplied with 3V and 5V since the highest power consumption is the internal charge pump which generates the 5V from VDD. In this case, the chip-internal charge pump and the internal 5V regulator shall be turned off. The power consumption in this configuration is less than 20mW compared to 80mW in the standard mode. The following application information shows how this can be achieved. Follow carefully the instructions in order to avoid damage of the chip.

Use protection diodes according to circuit diagram below. The diodes have to be low voltage Schottky devices with a forward current of at least 100mA (i.e. BAT74).



Make sure that external 5V supply (VDD_5V0) is delayed by at least 100µs to the VDD.

1. Power up VDD (3V)
2. Wait for at least 100µs
3. Power up VDD_5V0



Write the following sequence into the chip:

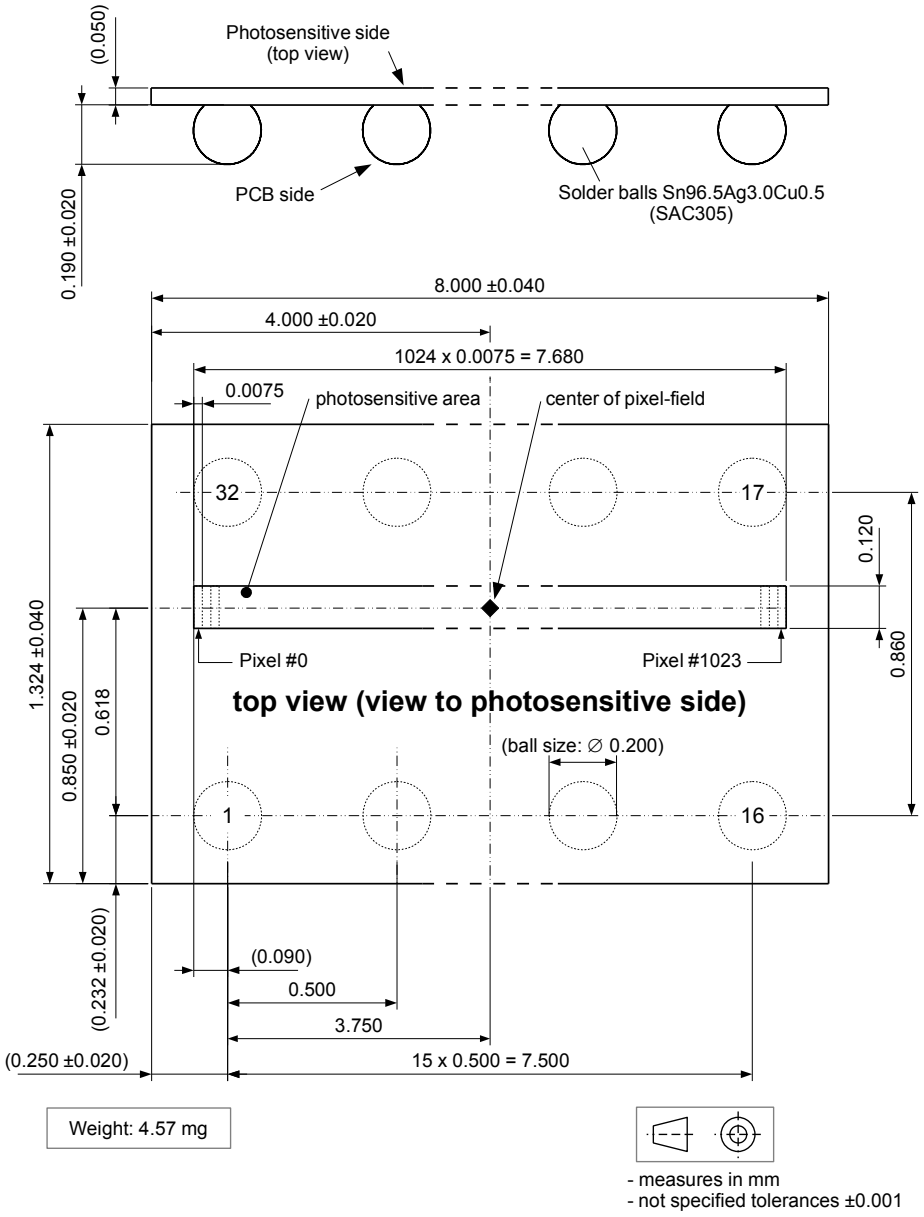
- Address 0xD0: ANA_TEST_MODE_EN_0 = 0x4a //release register write protection
- Address 0xD1: ANA_TEST_MODE_EN_1 = 0x66 //release register write protection
- Address 0xD6: FORCE_ANA_CTRL_SIGS = 0x03 //disable charge pump and 5V regulator

Important Note: The write access – as described above - has to occur as a sequence, no other read or write access is allowed in between (no auto read)!

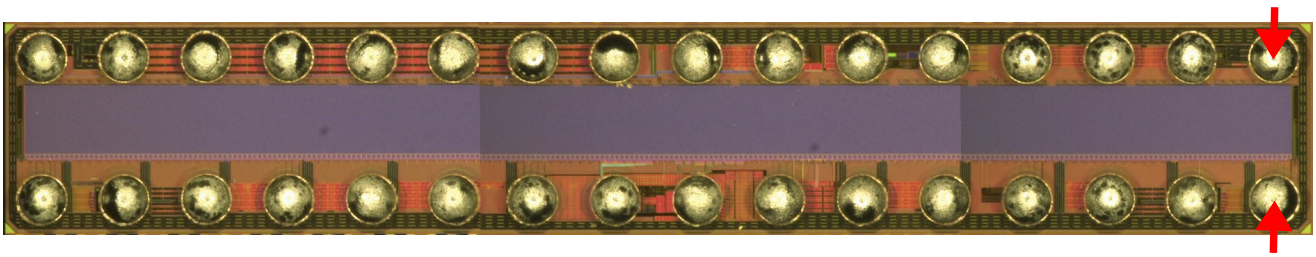
13. Layout and packaging information

13.1. Mechanical dimensions

The packaging technology is a CSP with a uBGA. All measures which do not have an explicit tolerance are meant +/-0.001mm.



The following picture shows the epc901 chip from the bottom side with view to the solder balls. Please note the location of pin 1 and pin 32.



Pin 1

13.2. Location of the photosensitive area

The photosensitive area is not marked neither on the front nor on the backside of the IC. As a visible reference, a metal ring of the IC can be used. From the back side (solder ball side) it is visible. Also from the front side (photosensitive area) it can be seen with a camera which is sensitive in the near infrared wavelength domain (950 .. 1150nm).

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13.3. Layout recommendations

13.3.1. Electrical

The epc901 line imager is a very high sensitivity analog/digital chip. Due to its high conversion gain, just a few electrons collected by coupling to signal lines close to the chip generate a significant voltage at the output. Thus, do not place any signal lines underneath the chip without shielding. It is highly recommended to place a stable AGND plane underneath the epc901 chip (on the top layer of the PCB) and not to place any signal tracks close to the chip.

Also very important is a clean noise-free power supply. Especially decouple the VDD from VDD_OA with capacitor so the output modulation of the video amplifier does not modulate the VDD of the chip. Make sure all the capacitors used for decoupling are low ESR types.

The READ signal line can also be a major source of noise or coupling to the output signal. Figure 15 shows a scope screenshot of such a coupling problem.

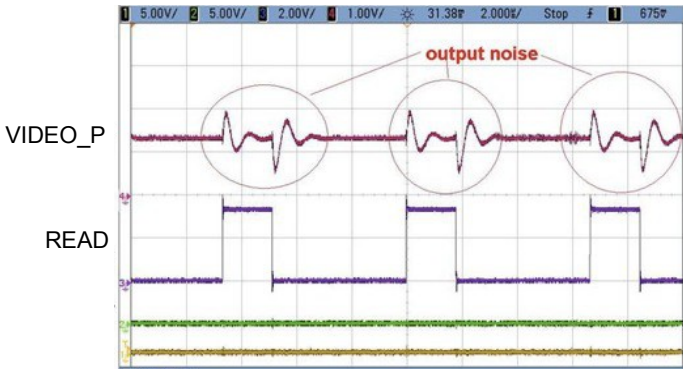


Figure 15: Bad READ signal coupling to the output by a ground loop

The source of such problems is usually a ground loop. Especially if there is a significant distance 'd' as shown in Figure 16 (starting from a few cm only) between the video output of the epc901 chip and the input of the ADC. Care has to be taken that the layout of the GND lines is exactly like shown in Figure 16. **Make sure that the digital GND has a separate track as shown by the blue ground line!**

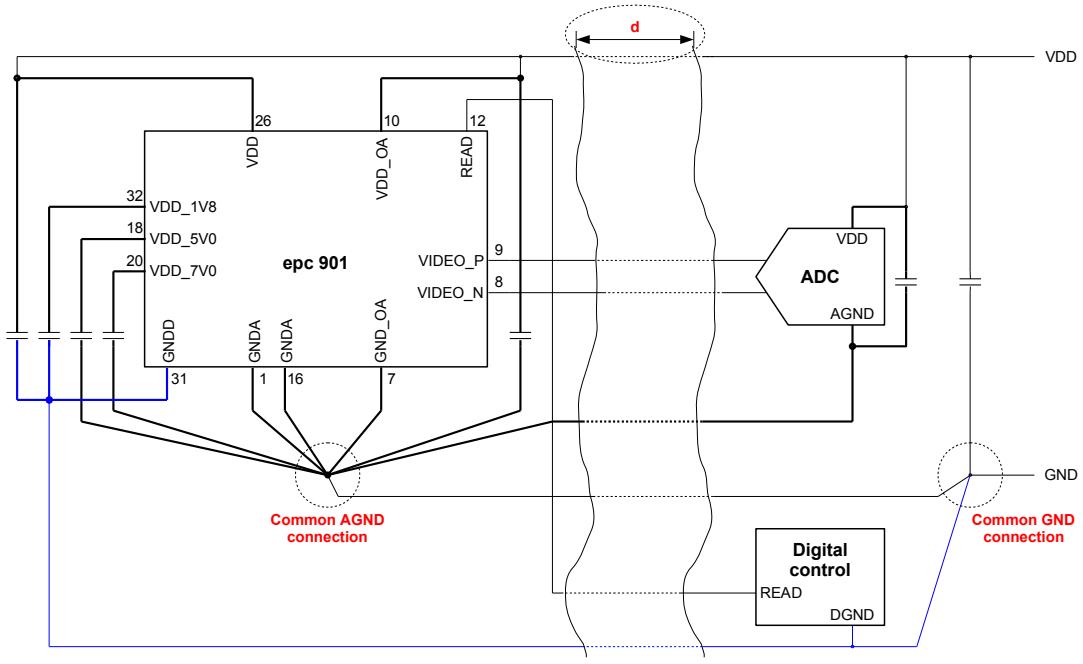


Figure 16: Recommended ground and power supply connections

Make also sure that the thick lines in Figure 16 are as short and as thick as possible.

13.3.2. PCB design and SMD manufacturing process considerations

Since the epc901 chip comes in a very small 32 pin chip scale package, the PCB layout should be made with special care. Since the silicon chip is small and light weight compared to the solder balls, it is highly recommended that all tracks to the chip should come straight from the side. A consequent symmetrical design is therefore highly recommended to achieve high production yield.

The pads and the tracks should also have exactly the same width and shall be covered by a solder resist mask in order to avoid drain of the solder tin alloy to the track.

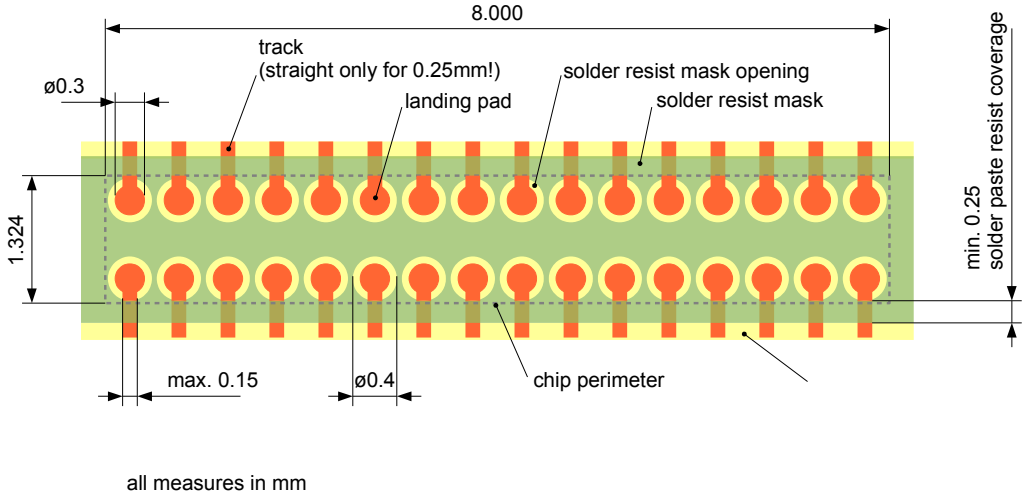


Figure 17: Recommended PCB layout

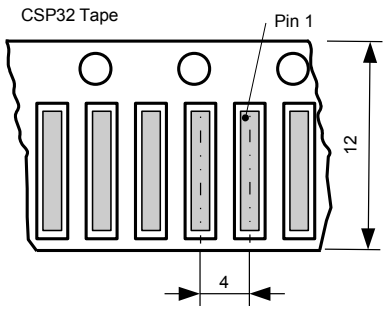
Underfill of the components reduces stress to the solder pads caused by e.g. temperature cycling or mechanical bending.The thermal and mechanical fatigue will be reduced and the longterm reliability will be increased. Underfill and underfill selection is application specific. It shall follow JEDEC-STD JEP150: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface- Mount Components.

Please also refer to the application note AN04 - Assembly of Wafer Level Chip Scale (WL-CSP) Packages - which can be downloaded from the ESPROS website at www.espros.com/application-notes. Obeying the recommendations in the applications AN04, a high manufacturing yield can be achieved.

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14. Tape & Reel Information

The devices are mounted on embossed tape for automatic placement systems. The tape is wound on 178 mm (7 inch) or 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate data sheet and indicate the tape sizes for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.



epc does not guarantee that there are no empty cavities. Thus, the pick-and-place machine should check the presence of a chip during picking.

14.1. Soldering and IC handling

Since the chip is only 50µm thick and has a high aspect ratio (length to width), a careful handling during the surface mount assembly process shall be taken in order to avoid mechanical damage. In addition to that, careful PCB layout is needed in order to achieve reliable assembly results with a high yield. Please refer to the application note AN04 from epc which contains comprehensive information to these topics. This application note can be downloaded at www.espros.com/application-notes.

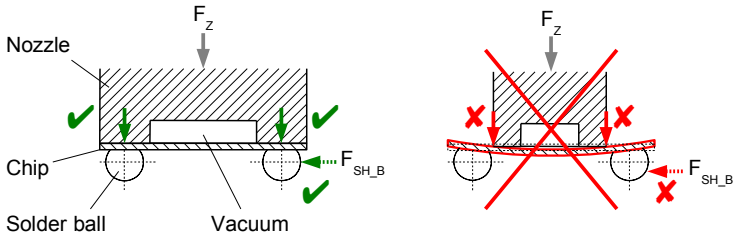
Item	Description
Solder balls: Alloy	Sn96.5Ag3.0Cu0.5 (SAC305)
Soldering profile	For infrared or conventional soldering, the solder profile has to follow the recommendations of IPC/JEDEC J-STD020C (revision C and later) for lead-free assembly.
Soldering lead temperature	T_L = 260 °C for 4s with a maximum gradient of 6 °C/s
Allowed cleaning agents	Isopropanol
Packaging technology	Bare-die CSP with underfill
Pick and place	 *Figure 18: Pick & place; left: good nozzle, good picking; right: bad nozzle, bad picking* The nozzle needs a flat surface. It must not touch the pixel-field area. It should not have any flashes where it touches the chip. The chip can get damaged. The nozzle has to bring the F_Z force evenly distributed in a vertical way to the center of the solder balls during picking and placing. Refer to Figure 18, left picture. It means that it should be large enough so that it picks the chip not just in the middle of the part but in the area above the solder balls. Bending of the chip is not allowed. Refer toFigure 18, right picture Keep attention having no shear forces to the solder balls during picking the chip from the tape pocket and/or placing. Maximum vertical force F_Z per chip: ≤ 0.8 N. Maximum shear force F_{SH_B} per ball: ≤ 0.5 N. Preferred is forceless picking with vacuum only. It is also highly recommended to use a „kiss-and-goodbye“ concept to place the component. It means that the nozzle should blow the part away when it does the placing.

Table 30: IC handling specification

15. Self-test mode by fill-and-spill

Instead of generating charge in the CCD by photo-electrical conversion, charge can also be generated electrically by the as-called fill-and-spill circuitry. To use the fill-and-spill circuitry, the IC has to be forced into test mode.

The basic behavior of the IC by the fill-and-spill circuitry is exactly the same as when the IC is illuminated. I.e. also when fill-and-spill is used, the acquisition is controlled by SHUTTER, the internal flush and shift operation are similar and the signal DATA_RDY is asserted at the end of the internal shift operation.

If the CCD is stimulated by the fill-and-spill circuitry, the on-chip test controller coordinates the operation of the fill-and-spill circuitry and the CCD. The following features of fill-and-spill can be controlled:

- number of electrons that are injected into the CCD per fill-and-spill cycle (pins ANA_TEST_*)
- number of fill-and-spill cycles per acquisition (register ANA_TEST_CONF)
- selection of which pixels are stimulated by fill-and-spill (register ANA_TEST_CONF)

The number of electrons that are injected into each pixel of the CCD during each fill-and-spill cycle depends on the voltages V_{IN} and V_{DC}. The two voltage levels V_{IN} and V_{DC} are provided through the analog test pads ANA_TEST*.

Q_{FILL_SPILL}	V_{IN} - V_{DC}
0	< 0
20k	0.44
40k	0.60
60k	0.72
80k	0.84
100k	0.95
120k	1.06
140k	1.16
160k	1.27
180k	1.37
200k	1.46

Q_{FILL_SPILL}	V_{IN} - V_{DC}
220k	1.56
240k	1.65
260k	1.75
280k	1.85
300k	1.95
320k	2.06
340k	2.17
360k	2.27
380k	2.36
400k	2.54
-	-

The number of fill-and-spill cycles per acquisition can be configured by NUM_FILL_SPILL_CYC in register ANA_TEST_CONF (see Table 32). The duration of one fill-and-spill cycle is $T_{CYC,FILL_SPILL}$ (see Table 31). In order to allow the full fill-and-spill operation to terminate the complete fill-and-spill operation, SHUTTER has to remain asserted for at least NUM_FILL_SPILL_CYC * $T_{CYC,FILL_SPILL}$ after the end of the internal flush operation (see Figure 19).

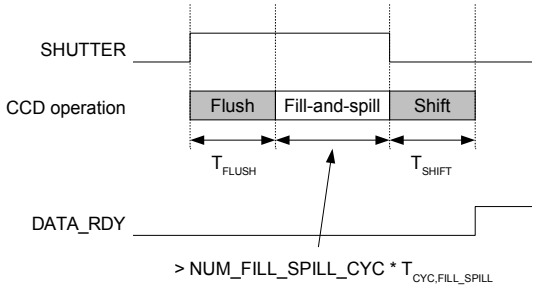


Figure 19: Timing diagram of a fill-and-spill operation of the CCD

Parameter	Description	Min	Typ	Max	Unit
V_{IN}	Voltage range of fill_spill_vin_packet_AI	1.5		5	V
V_{DC}	Voltage range of fill_spill_vdc_AI		2		V
$T_{CYC,FILL_SPILL}$	Duration of one fill-and-spill cycle		175		ns

Table 31: Parameters for the fill-and-spill operation

Register bits 3 to 6 of ANA_TEST_CONF are used in fill-and-spill test mode to configure into which pixels charge shall be spilled (see Table 32).

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Bit select	Description
7	not used
6	Selection for fill-and-spill: all odd pixels
5	Selection for fill-and-spill: pixels 2, 6, 10 etc.
4	Selection for fill-and-spill: pixels 4, 12, 20 etc
3	Selection for fill-and-spill: pixels 0, 8, 16 etc.
2:0	NUM_FILL_SPILL_CYC

Table 32: Bit select description of register ANA_TEST_CONF in fill-and-spill test mode

Fill-and-spill procedure:

1. Force the chip into test mode by applying the following voltages:
   TEST_MODE = VDD
   ROI_SEL = 0V or VDD
   RD_DIR = 0V or VDD
2. Open the access to the test mode configuration registers by the following two write operations. The two accesses must occur as a sequence, no other read or write access is allowed in between them in order to enable writing to the test registers. Once enabled, the write access remains available until the next time the IC is reset.
   ANA_TEST_MODE_EN_0: 0x4A
   ANA_TEST_MODE_EN_1: 0x66
3. Configure IC into fill-and-spill test mode by the following write access
   ANA_TEST_CTRL: 0x02
4. Select V_{IN} and V_{DC} to be connected to the test pins ANA_TEST_*
   ANA_TEST_MUX_0_SEL: 0x20
   ANA_TEST_MUX_1_SEL: 0x21
5. Configure the number of fill-and-spill cycles and select the pattern of pixels to be stimulated by writing to register ANA_TEST_CONF (see Table 32)
6. Connect the external voltage sources to supply V_{DC} and V_{IN} to the two test pins:
   ANA_TEST_0: V_{DC}
   ANA_TEST_1: V_{IN}
7. Wait for 10 µs
8. Acquire a frame by operating the SHUTTER input as described in section 5.5. and Figure 19.
9. Read-out the frame as described in section 5.4.
10. Disconnect external voltage sources from pads ANA_TEST_*
11. Configure test mode registers to their initial values
    ANA_TEST_MUX_0_SEL: 0x00
    ANA_TEST_MUX_1_SEL: 0x01
    ANA_TEST_CTRL: 0x0
    ANA_TEST_CONF: 0x0
12. Leave test mode by applying the following voltages:
    TEST_MODE = 0V
    ROI_SEL → application dependent
    RD_DIR → application dependent

15.1. Important notes to fill-and-spill

- In test mode the IC can behave in an unexpected way if the procedure described above is not strictly followed.
- The voltages V_{IN} - V_{DC} in the table above are theoretical values and for reference only. These values may have a significant deviation to the theoretical value. In addition to that, the voltage will vary over the pixel field.
- The pins ANA_TEST* are bi-directional. By default, they are outputs, i.e. the two voltages V_{IN} and V_{DC} may only be forced externally when the IC is in fill-and-spill test mode. Otherwise, the chip can get damaged!

16. Ordering Information

Part Number	Part Name	Package	RoHS compliance	Packaging Method
P100 360	epc901-CSP32	CSP32	Yes	Reel
P100 208	epc901 Evaluation Board V2	PCB 70.00 x 65.00 mm	Yes	Anti static bag
P100 209	epc901 Chip Carrier Board V2	PCB 36.00 x 42.75 mm	Yes	Anti static bag

Table 33: Ordering information

17. Note to various chip releases

The following is a list of notes and deviations of the effective chip performance to the data in this data sheet.

17.1. epc901-007 up to -016, -018, -020, -021, -022, -023

- The chips with these version numbers do not go into the power-down mode as long as processes are active, e.g. if the temperature sensor is activated, the power-down mode is ignored. Since the temperature sensors are turned on by default, the chips will never go into power-down without turning the temperature sensors off by the I2C command.
- Video amplifier instability for higher gain-bandwidth product settings: Use only lowest gain-bandwidth product setting (VIDEO_GBW_SEL_REG = 0x00).
- Read direction from 0 to 1023 (RD_DIR = 0) not working.
- The chips with these version numbers are not suitable for usage with a 1.8V ADC for following reasons:
  - When the video amplifier is idle, the outputs VIDEO_P and VIDEO_N go to the VDDOA rails i.e. 0V and 3V typical. This typically violates the maximum input voltage of 1.8V ADCs. From version -031, VIDEO_P and VIDEO_N go to the common-mode during idle.
  - The video amplifier does not work reliably at VIDEO_CM = 0.9V plus/minus a tolerance, typically the common-mode level used for 1.8V ADCs
- Voltage difference between VIDEO_P and VIDEO_N resp. voltage on VIDEO_P (see Figure 13 and Figure 14 for reference)

Mode	Illumination	VIDEO_N (typ.)	VIDEO_P(typ.)	Voltage difference between VIDEO_P and VIDEO_N (typ.)
single ended	Dark voltage	n/a	0.2	n/a
	Maximum video output	n/a	2.0	n/a
differential	Dark voltage	V_{VIDEO_CM} + 0.45V	V_{VIDEO_CM} – 0.45V	-0.9
	Maximum video output	V_{VIDEO_CM} – 0.7V	V_{VIDEO_CM} + 0.7V	1.4

- The solder balls on the solder pads have a diameter of 270 ±20 µm.

17.2. epc901-007 up to -016, -018, -020, -021, -022

- Single-ended mode does not start-up properly.

17.3. epc901-016

- The output bandwidth is limited to approx. 4MHz.

17.4. epc901-007 up to and including -018, -020, -022

- Use the the chip only according to section 12.2., Low power operation with external 3V and 5V supply. The charge pump does not work properly for these versions.

17.5. epc901-031

- The default settings for the video amplifier common-mode feedback (register bits SC_CMFB_EN and AMP_PHY_IDLE_EN) are not valid. The settings have to be changed to SC_CMFB_EN = 1, AMP_PHY_IDLE_EN = 1 prior the first read-out (registers MISC_CONF and FORCE_ANA_CTRL_SIGS).
- The solder balls on the solder pads have a diameter of 270 ±20 µm.

17.6. epc901-007 up to and including -016

Description	Conditions	
ESD rating	all pins except VDD7V0 vs. VDD1V8, SCL vs. GND, SCL vs. VDD3V3:	HBM class 2 (2kV to <4kV, JEDEC)
	Pins VDD7V0 vs. VDD1V8, SCL vs. GND, SCL vs. VDD3V3:	HBM class 1B (500V to <1kV, JEDEC)

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