YAMAHA LSI

YSS215

AVSP

Audio & Visual Surround Processor

■ OUTLINE

YSS215 is digital sound field processor with Dolby Pro Logic decoder based on Digital Signal Processing technology.

The LSI has A/D & D/A Converter and uses digital signal processing for almost all functions needed in Pro Logic. This allows construction of highly reliable decoder with small quantity of components. It also has original sound field simulation circuit with 29 digital delay line (370 ms at max.), so you can design 2in-4out surround system easily.

■ FEATURES

- Highly accurate signal processing with internal operation word length of 32 bits.
- Adaptive matrix, noise generator, 7 kHz low pass filter, modified B-type N.R. decoder and A/D & D/A converter are built-in.
- Auto Input Balance circuit is built-in. (ON/OFF)
- Capable of mixing 8 taps with delay time up to 370 ms at surround channel in Dolby Pro Logic mode.
- Capable of noise control.
- Original simulation surround using digital delay (maximum delay time: 370 ms, 29 taps (L+R, L−R), low pass filter (ON/OFF)).
- External 256k PSRAM interface for 16 bits linear digital delay.
- Serial interface with microprocessor for parameter control.
- Analog signal processing for the front three channels (L, R, C).
- Master clock frequency: 11.2896 MHz, sampling frequency: 44.1 kHz.
- 5V single power supply, silicon gate CMOS, 64 pin QFP package. (YSS215-F)
- Dolby reference operate level: 300 mVr.m.s.

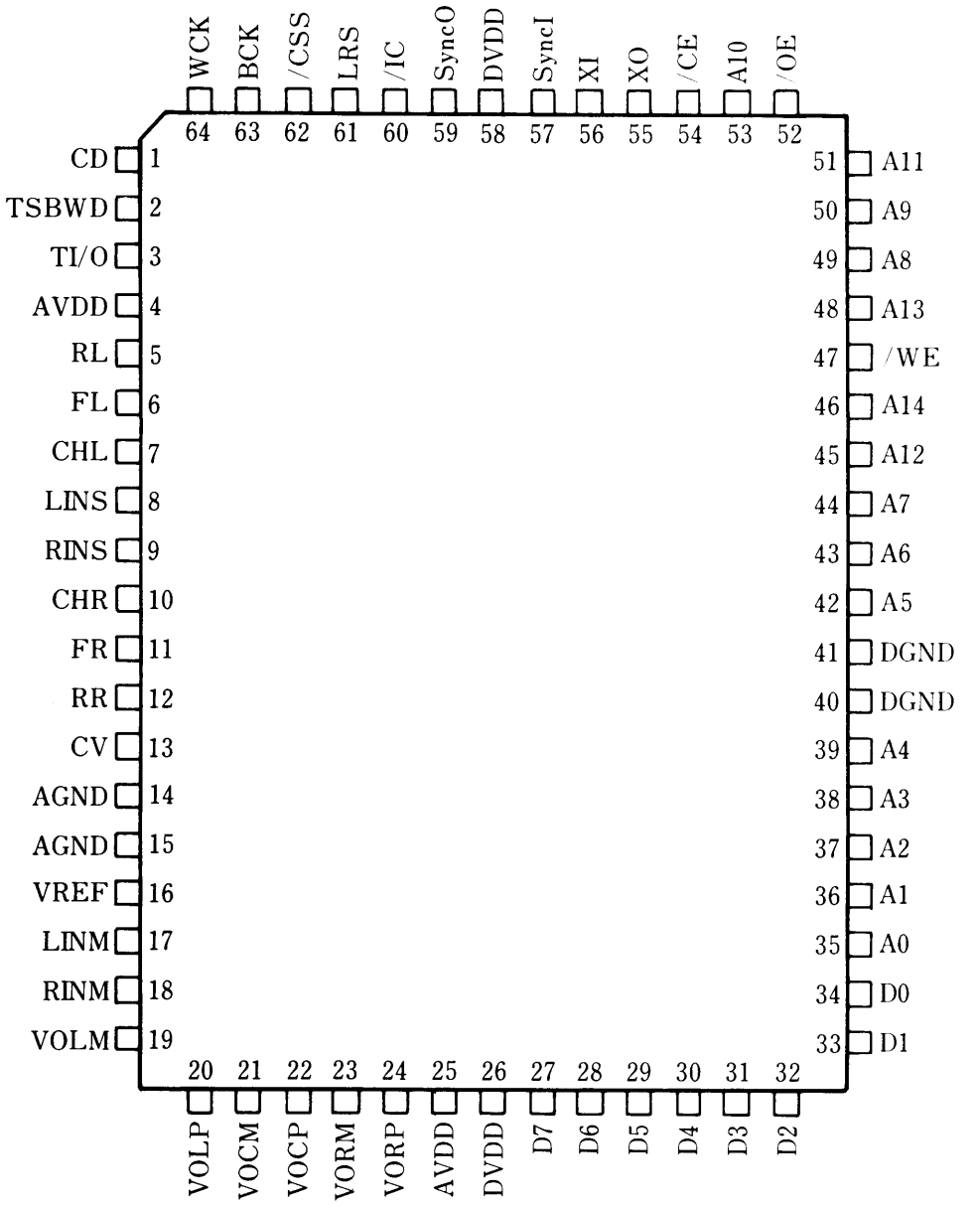
(Note)

"Dolby Pro Logic" is a trademark of Dolby Laboratories Licensing Corporation. This LSI is available only to licensees of Dolby Laboratories Licensing Corp.

YAMAHA CORPORATION

YSS215 CATALOG
CATALOG No. : LSI-4SS2152
1995. 5

■ PIN CONFIGURATION



64pin QFP TOP VIEW

■ PIN DESCRIPTIONS

Pin No.	I/O	Pin name	Description
1	Its	CD	Serial data for parameter data input
2	Ic	TSBWD	LSI test terminal, to be usually connected to DVDD
3	Ic	TI/O	LSI test terminal, to be usually connected to DVDD
4	A–	AVDD	+5V power supply (for D/A & A/D converter)
5	AO	RL	RL channel, D/A output
6	AO	FL	FL channel, D/A output
7	A–	CHL	Sample/hold capacitor terminal for LINS input
8	AI	LINS	L channel, A/D input
9	AI	RINS	R channel, A/D input
10	A–	CHR	Sample/hold capacitor terminal for RINS input
11	AO	FR	FR channel, D/A output
12	AO	RR	RR channel, D/A output
13	AO	CV	Center voltage of A/D, multiplying DAC
14	A–	AGND	Ground (for D/A & A/D converter)
15	A–	AGND	Ground (for multiplying DAC)
16	AI	VREF	Reference voltage input of multiplying DAC
17	AI	LINM	L channel, multiplying DAC input
18	AI	RINM	R channel, multiplying DAC input
19	AO	VOLM	Connected to L channel, operational amplifier, – terminal
20	AO	VOLP	Connected to L channel, operational amplifier, + terminal
21	AO	VOCM	Connected to C channel, operational amplifier, – terminal
22	AO	VOCP	Connected to C channel, operational amplifier, + terminal
23	AO	VORM	Connected to R channel, operational amplifier, – terminal
24	AO	VORP	Connected to R channel, operational amplifier, + terminal
25	A–	AVDD	+5V power supply (for multiplying DAC)
26	—	DVDD	+5V power supply (for digital circuit)
27	I/Ot	D7	Data 7 for external delay RAM
28	I/Ot	D6	Data 6 for external delay RAM
29	I/Ot	D5	Data 5 for external delay RAM
30	I/Ot	D4	Data 4 for external delay RAM
31	I/Ot	D3	Data 3 for external delay RAM
32	I/Ot	D2	Data 2 for external delay RAM
33	I/Ot	D1	Data 1 for external delay RAM
34	I/Ot	D0	Data 0 for external delay RAM
35	O	A0	Address 0 for external delay RAM
36	O	A1	Address 1 for external delay RAM
37	O	A2	Address 2 for external delay RAM
38	O	A3	Address 3 for external delay RAM
39	O	A4	Address 4 for external delay RAM
40	—	DGND	Ground (for digital circuit)
41	—	DGND	Ground (for digital circuit)
42	O	A5	Address 5 for external delay RAM

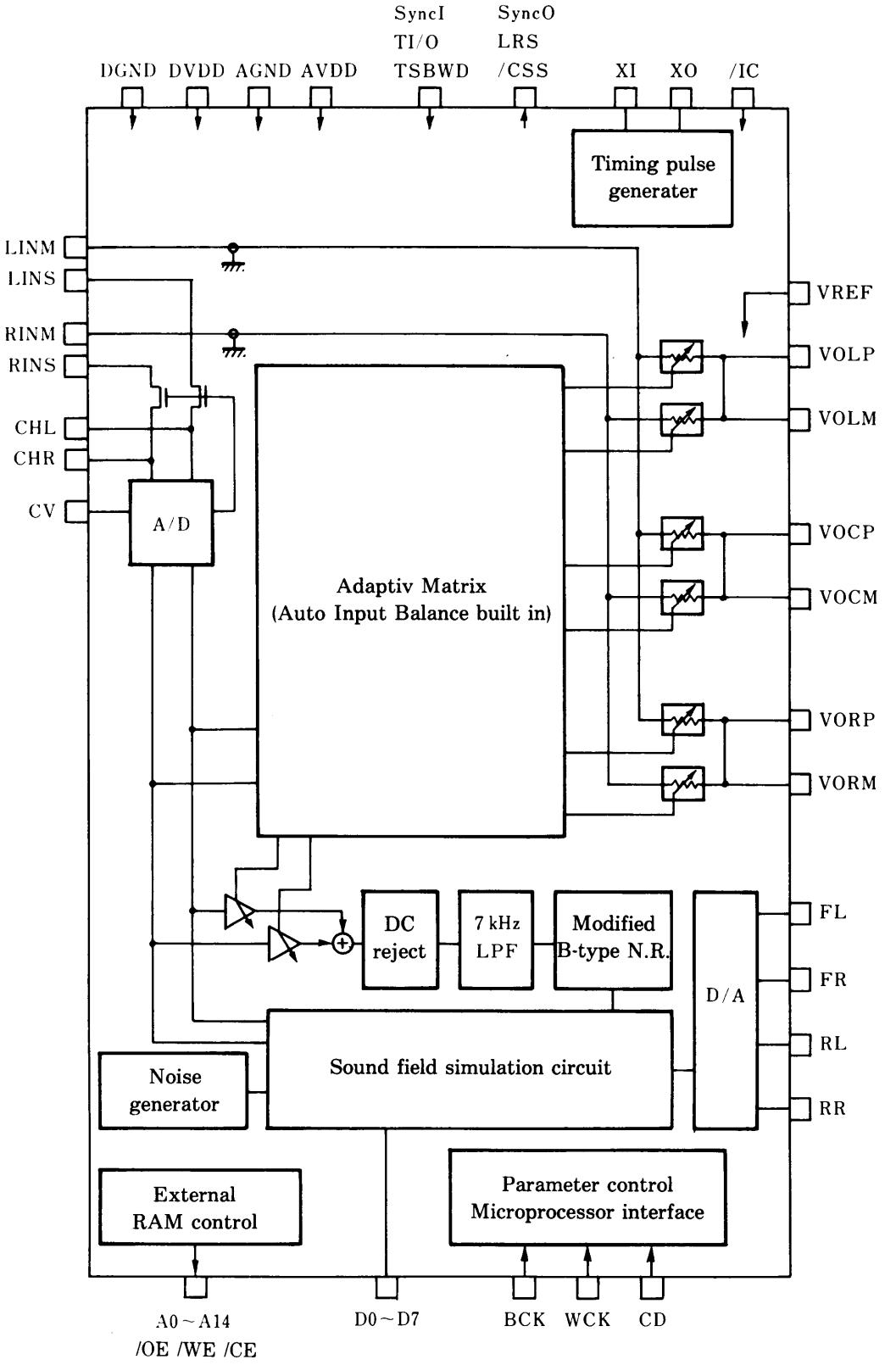
Pin No.	I/O	Pin name	Description
43	O	A6	Address 6 for external delay RAM
44	O	A7	Address 7 for external delay RAM
45	O	A12	Address 12 for external delay RAM
46	O	A14	Address 14 for external delay RAM
47	O	/WE	WE for external delay RAM, write enable terminal
48	O	A13	Address 13 for external delay RAM
49	O	A8	Address 8 for external delay RAM
50	O	A9	Address 9 for external delay RAM
51	O	A11	Address 11 for external delay RAM
52	O	/OE	OE for external delay RAM, output enable terminal
53	O	A10	Address 10 for external delay RAM
54	O	/CE	CE for external delay RAM, chip enable terminal
55	O	XO	X'tal oscillator terminal
56	I	XI	X'tal oscillator terminal (11.2896 MHz)
57	It	SYNCI	Test terminal, to be usually connected to DVDD
58	—	DVDD	+5V power supply (for digital circuit)
59	O	SYNCO	Test terminal, usually without connection
60	Ics	/IC	Initial clear terminal (Power-on resetting is required.)
61	O	LRS	Terminal for external Auto Input Balance circuit, usually without connection
62	O	/CSS	Terminal for external Auto Input Balance circuit, usually without connection
63	Its	BCK	Bit clock for parameter data input
64	Its	WCK	Word clock for parameter data input

Note) Meanings of the symbols at the column I/O:

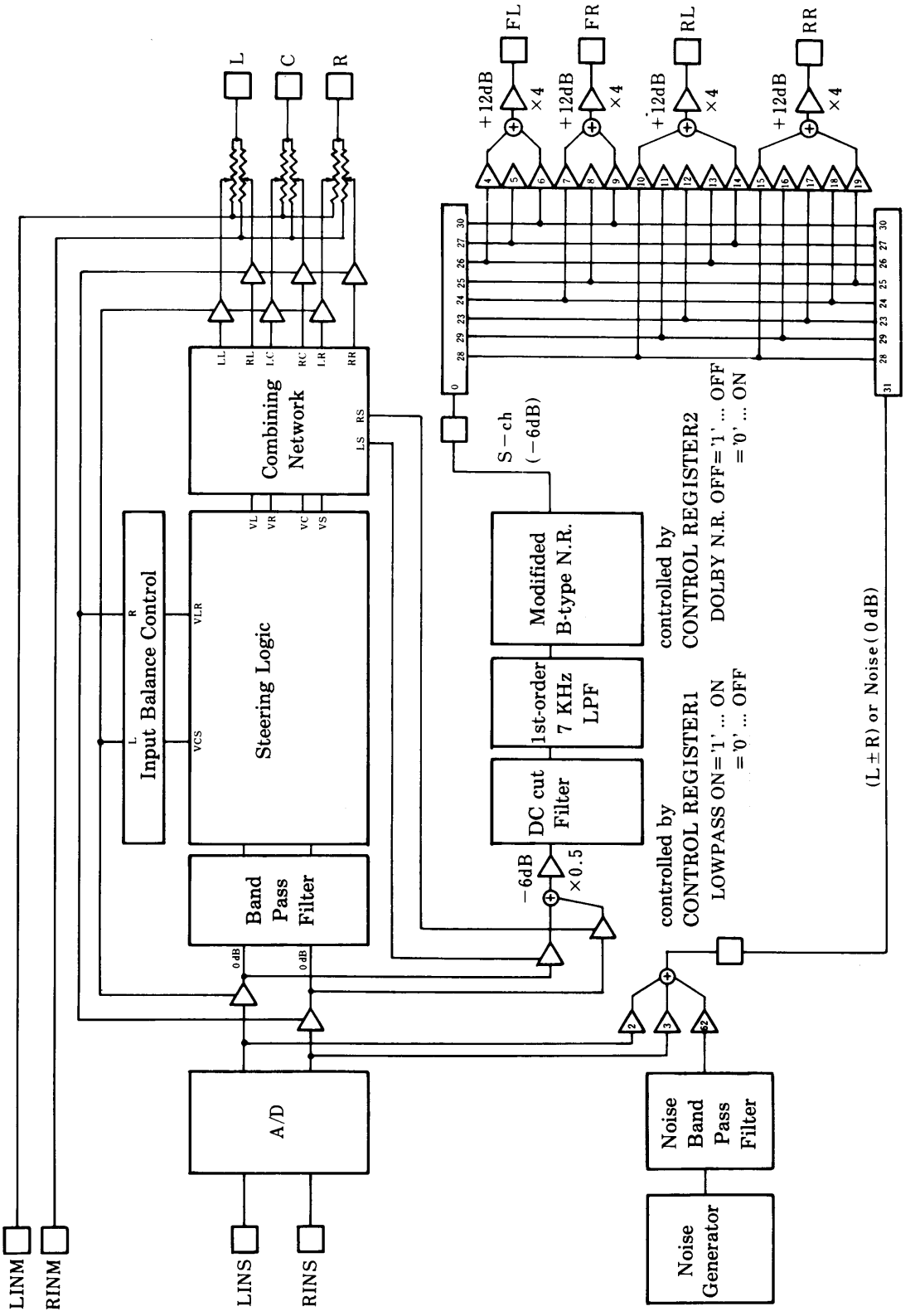
I: Input terminal O: Output terminal A: Analog terminal

t: TTL level c: CMOS level s: Schmidt input

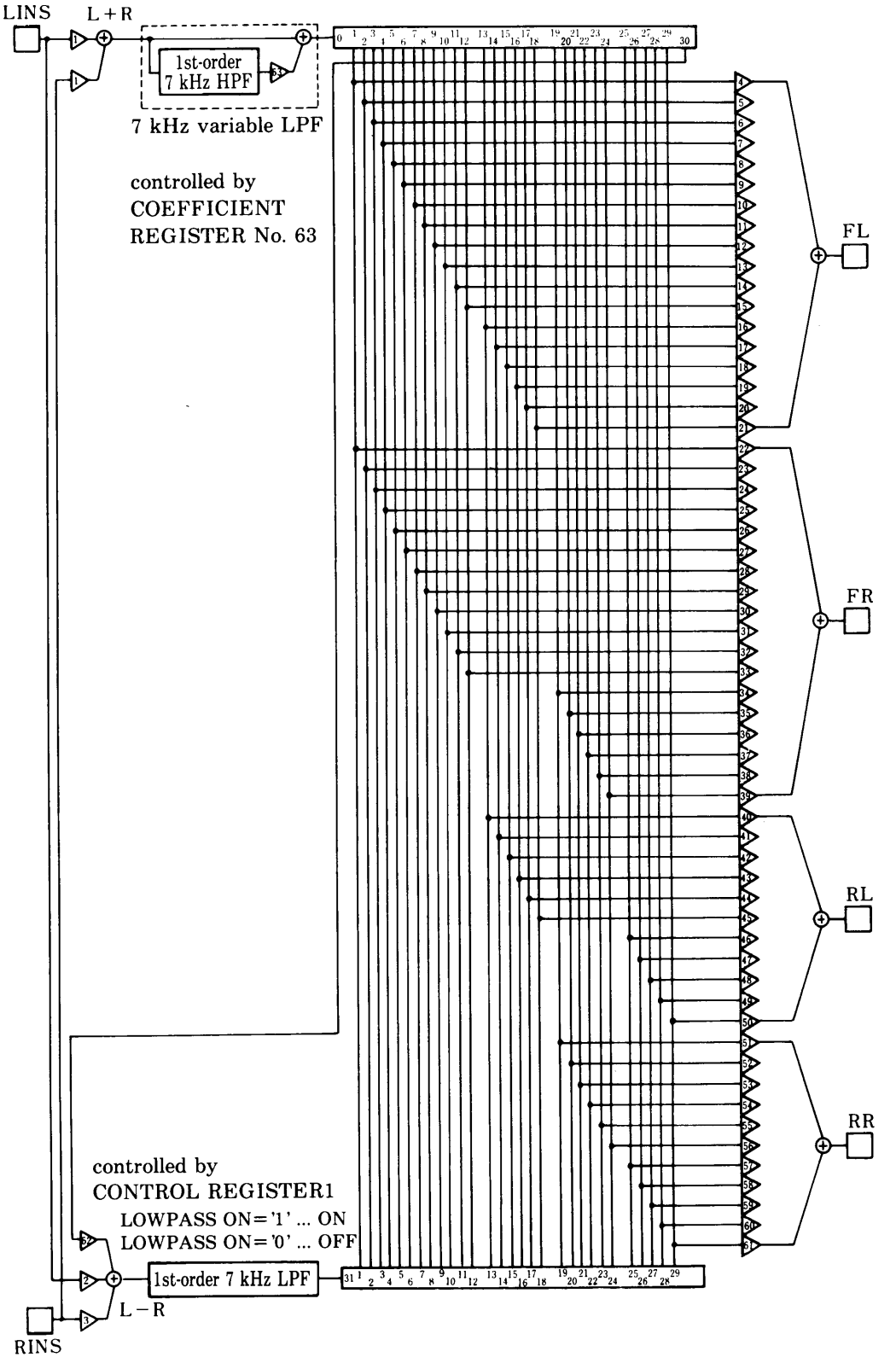
■ BLOCK DIAGRAM



■ Dolby Pro Logic BLOCK DIAGRAM



■ DSP BLOCK DIAGRAM



■ EXTERNAL DATA RAM INTERFACE

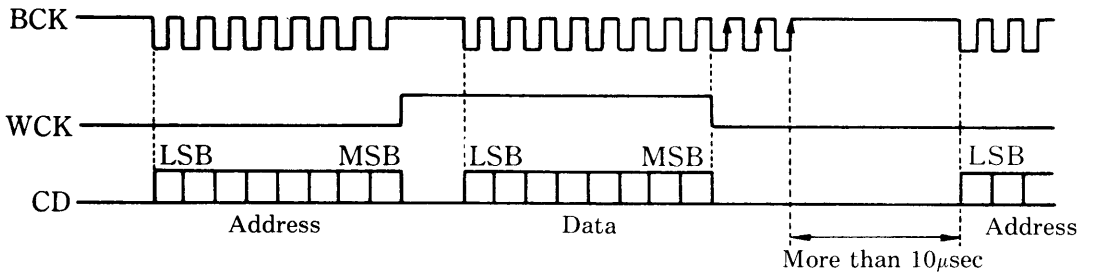
External RAM interface reads and writes a 256 Kbit Pseudo Static RAM. The LSI accesses eight-bit data from D0 to D7 twice to obtain 16 bit data.

Please use a PSRAM with access-time of 100nsec.

■ MICROPROCESSOR INTERFACE

MICROPROCESSOR INTERFACE writes parameters to Control Registers using BCK, WCK and CD. The timing is shown below.

(1) TIMING CHART



Note 1) More than three BCK rises are required after the MSB of data is input and WCK falls. For writing to Coefficient Register (address: $81 to $BF) and Address Register (address: $C0 to $FF), at least 10μs is required between the third BCK rise and the next CD input.

Note 2) CD data without a WCK rise or fall, and data of addresses $04, $08 to $0F, $10 to $3F, $80 and $C0 are ineffective.

(2) CONTROL REGISTER MAP

ADDR HEX	NAME	BIT ASSIGNMENT LSB	1	2	3	4	5	6	MSB
00	MASTER CONTROL REGISTER	IC	CL MUTE	×	×	×	×	×	×
01	CONTROL REGISTER 1	DOLBY ON	CENTER OFF	STEERING OFF	SURROUND STEERING OFF	PHANTOM ON	MMIX ON	LOWPASS ON	AUTO BALANCE ON
02	CONTROL REGISTER 2	NOISE ON	EXTERNAL RAM OFF	DOLBY N.R. OFF	×	×	×	×	×
03	STEERING GAIN	(Do not write, reset with Initial clear)							
05 06 07	TESTT TEST1 TEST2								
40 : 7F	MAIN CHANNEL MANUAL MIX CONTROL								
81 : BF	COEFFICIENT REGISTER								
C1 : FF	DELAY TIME REGISTER								

- ×; Don't Care
- Don't write to the other Address

(3) DATA DESCRIPTION

• MASTER CONTROL REGISTER

IC	'1'=Initial clear (initializes internal circuit)
CL MUTE	'1'=Initial data clear (Sound data in external RAM and internal filter RAM can be cleared to '0'.)

Note 1) Internal IC and external /IC have same functions, but MASTER CONTROL REGISTER is reset to '0' with external /IC.

Note 2) CL MUTE resets all processing sound data to '0'. Note that it needs 370 ms to clear all data in external PSRAM.

• CONTROL REGISTER 1

DOLBY ON	'1'=Dolby Pro Logic mode '0'=Simulation surround mode (set to '1' with IC)
CENTER OFF	'1'=Center channel off '0'=Center channel on (set to '0' with IC)
STEERING OFF	'1'=Steering off for all channels '0'=Steering on for all channels It must be set to '1' for Simulation surround mode or '0' for Dolby Pro Logic mode. (set to '0' with IC)
SURROUND STEERING OFF	'1'=Steering off for surround channel '0'=Steering on for surround channel When this bit is set to '1', steering is not passed to surround channel. This bit must be set to '1' for 3 channel logic. (set to '0' with IC)
PHANTOM ON	'1'=Phantom on, '0'=Phantom off PHANTOM ON='1' must be used with CENTER OFF='1'. (set to '0' with IC)
MMIX ON	'1'=Data of multiplying DACs are set with the microprocessor. '0'=Data of multiplying DACs are controlled by Steering circuit. It must be set to '0' for Dolby Pro Logic mode. (set to '0' with IC)
LOWPASS ON	'1'=7kHz low pass filter on, '0'=7kHz low pass filter off In simulation surround mode, data of L, R and tap NO. 30 are input to this LPF. (see DSP BLOCK DIAGRAM) (set to '0' with IC)
AUTO BALANCE ON	'1'=Auto Input Balance on '0'=Auto Input Balance off (set to '0' with IC)

Note 1) When DOLBY ON='1', the multiplying DAC's values of front 3 channels can be set with MMIX ON='1'.
But the steering of surround channel is still controlled by Steering circuit.

Note 2) LOWPASS ON ('0' or '1') is effective when DOLBY ON='1' as well as when DOLBY ON='0'.

• CONTROL REGISTER 2

NOISE ON	'0'=Noise generator off '1'=Noise generator on (set to '0' with IC)
EXTERNAL RAM OFF	'0'=External PSRAM interface on '1'=External PSRAM interface off (set to '0' with IC)
DOLBY N.R. OFF	'0'=Dolby Noise Reduction on '1'=Dolby Noise Reduction off (set to '0' with IC)

Note 1) NOISE ON is a reset signal of M-sequence noise generator.
Noise output is '0' when it is set to '0'.

Note 2) When EXTERNAL RAM OFF='1', external PSRAM can be removed.
This bit should be set to '0' in normal use.

Note 3) When DOLBY N.R. OFF='1', sliding band filter in N.R. circuit can be stopped.
And then • TSBWD=1 → Noise Reduction off
• TSBWD=0 → Noise Reduction max.
Please connect TSBWD (pin No.2) to DVDD in normal use.

• MAIN CHANNEL MANUAL MIX CONTROL

It sets the mixing gains of main channels. D0 to D10 are the data for multiplying DACs.

Address								Data								Channel
MSB	6	5	4	3	2	1	LSB	MSB	6	5	4	3	2	1	LSB	
0	1	D2	D1	D0	0	0	0	D10	D9	D8	D7	D6	D5	D4	D3	L input → L output
0	1	D2	D1	D0	0	0	1	D10	D9	D8	D7	D6	D5	D4	D3	R input → L output
0	1	D2	D1	D0	0	1	0	D10	D9	D8	D7	D6	D5	D4	D3	L input → R output
0	1	D2	D1	D0	0	1	1	D10	D9	D8	D7	D6	D5	D4	D3	R input → R output
0	1	D2	D1	D0	1	0	0	D10	D9	D8	D7	D6	D5	D4	D3	L input → C output
0	1	D2	D1	D0	1	0	1	D10	D9	D8	D7	D6	D5	D4	D3	R input → C output

Note 1) Data are 11 bits in sign-magnitude form. D10 represents sign and D9 to D0 represent magnitude (0 to 1023).

Note 2) These registers are effective when MMIX ON='1'.

Note 3) Two multiplying DACs connected to one output (for example, L input → L output and R input → L output) cannot have negative values at a time.

• COEFFICIENT REGISTER

Address								Coefficient NO.	Data							
MSB	6	5	4	3	2	1	LSB		MSB	6	5	4	3	2	1	LSB
1	0	0	0	0	0	0	1	1	Max. 127 to Min. −128 2's complement form							
			↓					↓								
1	0	1	1	1	1	1	1	63								

Note 1) Data are 8 bits in 2's complement form.

Note 2) Coefficient numbers correspond to those in DOLBY PRO LOGIC BLOCK DIAGRAM and DSP BLOCK DIAGRAM.

• DELAY TIME REGISTER

Address								Tap NO.	Data (Delay-time data)							
MSB	6	5	4	3	2	1	LSB		MSB	6	5	4	3	2	1	LSB
1	1	×	0	0	0	0	1	1	1 ~ 255 1.45125msec/DATA							
				≀				≀								
1	1	×	1	1	1	1	1	31								

Note 1) Tap numbers correspond to those in DOLBY PRO LOGIC BLOCK DIAGRAM and DSP BLOCK DIAGRAM.
Delay-time data of tap NO. 31 correspond to address in PSRAM to which sound data are written. (Tap NO. 31 is a output tap to PSRAM.) PSRAM can be divided into two blocks according to delay-time data of tap NO. 31. If delay-time data of a tap are bigger than those of tap NO. 31, the tap reads sound data of tap NO. 31 and sound data are delayed as much as the difference between delay-time data of these taps. If delay-time data of a tap are smaller than those of tap NO. 31, the tap reads sound data of tap NO. 0 and they are delayed as much as the delay-time data of the tap.
Maximum delay is 370 ms with increment of 1.45125 ms.

Note 2) Delay-time data '0' and the same delay-time data as tap NO. 31 should not be used for tap NO. 1 ~ NO. 30. When delay isn't required, let analog signals go through by using MANUAL MIX CONTROL.

Note 3) To be precise, delay of two samplings (about 44 μs) will be added to the delay of FL, FR, RL and RR because of A/D & D/A conversion. And difference by 1 sampling (about 22μs) may be caused due to timing adjustment for reading/writing to external RAM.

Note 4) When DOLBY ON='1', data of only tap NO. 23 to 30 are effective. In order to output surround signals, delay-time data of 15 to 30 ms should be written to at least one of these taps.

■ ELECTRICAL CHARACTERISTICS

• ABSOLUTE MAXIMUM PATINGS

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.5	V
Input current	I_I		10	mA
Operating temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

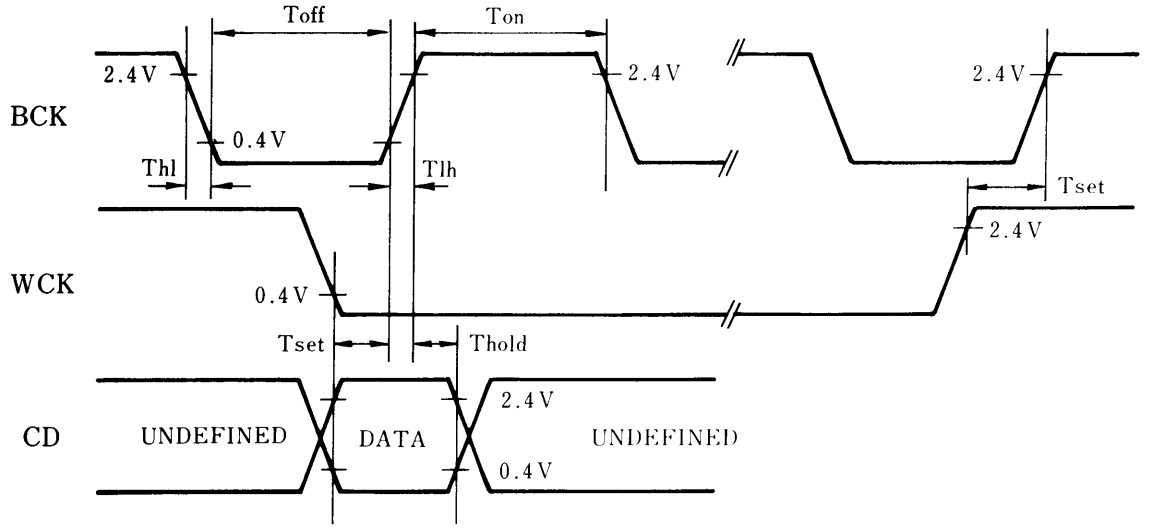
• RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating temperature	Top	0	25	70	°C

• DC CHARACTERISTICS (CONDITIONS: Ta=25°C, V_{DD}=5.0±0.25V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	W	V_{DD}=5.0V		250	400	mW
Input voltage H level	V_{IH}					V
TTL level			2.7		V_{DD}	
CMOS level			3.5		V_{DD}	
Input voltage L level	V_{IL}					V
TTL level			0		0.4	
COMS level			0		1.0	
Input leakage current	I_{IL}				10	μA
Output voltage H level	V_{OH}	I_{OH}=200μA	3.0		V_{DD}	V
Output voltage L level	V_{OL}	I_{OL}=−2mA	0		0.4	V

- **AC CHARACTERISTICS**



Parameter	Symbol	Min.	Typ.	Max.	Unit
BCK max. frequency	XBCK			2.0	MHz
BCK rise time	Thl			50	nsec
BCK fall time	Thl			50	nsec
BCK on time	Ton	200			nsec
BCK off time	Toff	200			nsec
Data set-up time	Tset	50			nsec
Data hold time	Thold	20			nsec
XI frequency	XIN	11.0	11.2896	12.0	MHz
XI clock duty		40	50	60	%

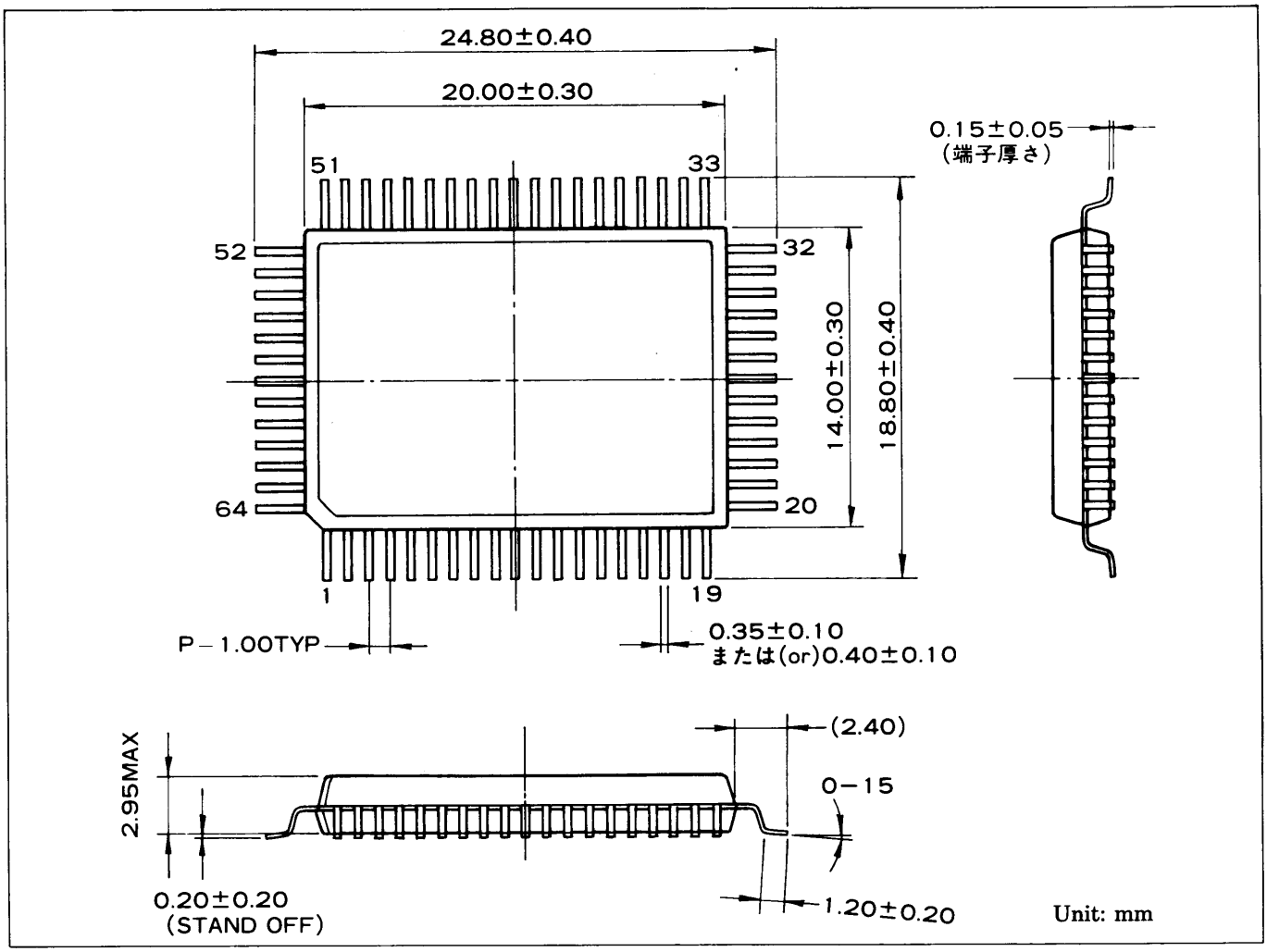
• ANALOG CHARACTERISTICS (CONDITIONS: V_{DD}=+5V, Ta=25°C, X_{IN}=11.2896MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Multiplying DAC impedance	RM		8.0	9.6	11.5	KΩ
Output distortion		Output				
Main channel	Dmmax	300mVr.m.s.		0.03	0.1	%
Surround channel	Dsmax			0.25	0.7	
Output S/N						
Main channel	S/N m		85			
Surround channel		CCIR-ARM				
Dolby Pro Logic mode	S/Nsd	(0dB=300mVr.m.s.)	70	77		dB
Simulation Surround mode *1	S/Nss		65	70		
Frequency response						
Main channel	Frm	50 ~ 20kHz			±0.2	dB
Surround channel	Frs	50 ~ 6kHz			±0.5	
Modified B-type N.R. decoding accuracy	N.R.a	0dB=300mVr.m.s.			±1.0	dB
Noise generator output level	Nout	after Noise BPF		85		mVr.m.s.
Dolby Pro Logic steering separation	STsep			30		dB
Max. input level	Smax	0dB=300mVr.m.s.	15			dB

Note 1) Main Channel indicates L, R, and C channel.
Surround Channel indicates FL, FR, RL, and RR channel.

Note 2) *1 Unity Gain.

■ EXTERNAL DIMENSIONS [YSS215-F]



Note: The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

The specifications of this product are subject to improvement changes without prior notice.

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