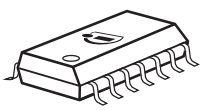
5-V Low Drop Fixed Voltage Regulator

TLE 4278 G

Features

- Output voltage tolerance ≤ ±2%
- Very low current consumption
- Separated reset and watchdog output
- Low-drop voltage
- Watchdog
- Adjustable watchdog activating threshold
- Adjustable reset threshold
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range



P-DSO-14-3, -8, -9, -11, 14

Functional Description

The TLE 4278 is a monolithic integrated low-drop fixed output voltage regulator supplying loads up to 200 mA. The IC is available in a P-DSO-14-8 package. It is designed to supply microprocessor systems under the severe conditions of automotive applications and therefore equipped with additional protection functions against overload, short circuit and overtemperature. The TLE 4278 can also be used in other applications where a stabilized voltage is required.

An input voltage V_I in the range of 5.5 V ≤ V_I ≤ 45 V is regulated to $V_{Q,nom}$ = 5 V with an accuracy of ±2%.

The device operates in the wide temperature range of T_j = -40 to 150 °C.

Two additional features are implemented in the TLE 4278 a load dependent watchdog function as well as a sophisticated reset function including power on reset, under voltage reset, adjustable reset delay time and adjustable reset switching threshold.

The watchdog function monitors the microcontroller, including time base failures. In case of a missing rising edge within a certain pulse repetition time the watchdog output is set

Type	Ordering Code	Package
TLE 4278 G	Q67007-A9291	P-DSO-14-8

to LOW. Programming of the max. repetition time can be done easily by an external reset delay capacitor. To prevent a reset in case of missing pulses, the watchdog output WO is separate from the reset output RO for the TLE 4278. The watchdog output can be used as an interrupt signal for the microcontroller. In any case it is possible to connect pin WO and pin RO externally.

When the controller is set to sleep mode or low power mode its current consumption drops and no watchdog pulses are created. In order to avoid unnecessary wake-up signals due to missing pulses at pin WI the watchdog feature can be disabled as a function of the load current. The switch off threshold is set by an external resistor to pin WADJ. The watchdog function can also be used as a timer, which periodically wakes up the controller. Therefore the pin WADJ has to be connected to the output Q.

The power on reset feature is necessary for a defined start of the microprocessor when switching on the application. The reset signal at pin RO goes high after a certain delay timed t_{rd} when the output voltage of the regulator has surpassed the reset threshold. The delay time is set by the external delay capacitor. An under voltage reset circuit supervises the output voltage. In case V_Q falls below the reset threshold the reset output is set to LOW after a short reset reaction time t_{rr}. The reset LOW signal is generated down to an output voltage V_Q of 1 V. In addition the reset switching threshold can be adjusted by an external voltage divider. This feature is useful with microprocessors which guarantee a safe operation down to voltages below the internally set reset threshold of 4.65 V typical.

P-DSO-14-8

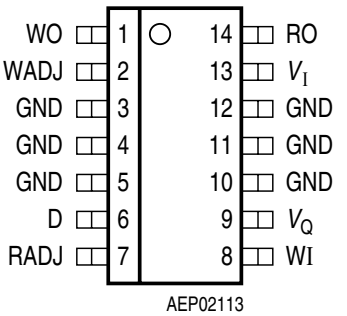


Figure 1 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin	Symbol	Function
1	WO	**Watchdog Output;** the open collector output is connected to the 5 V output via an integrated resistor of 30 kΩ.
2	WADJ	**Watchdog Adjust;** an external resistor to GND determines the watchdog activating threshold.
3, 4, 5, 10, 11, 12	GND	**Ground**
6	D	**Reset Delay;** connect a capacitor to ground for delay time adjustment.
7	RADJ	**Reset Switching Threshold Adjust;** for setting the switching threshold, connect a voltage divider from output to ground. If this input is connected to ground, the reset is triggered at the internal threshold.
8	WI	**Watchdog Input;** rising edge-triggered input for monitoring a microcontroller.
9	Q	**5 V Output Voltage;** block to ground with min. 10 µF capacitor, ESR ≤ 5 Ω.
13	I	**Input Voltage;** block to ground directly on the IC with ceramic capacitor.
14	RO	**Reset Output;** the open collector output is connected to the 5 V output via an integrated resistor of 30 kΩ.

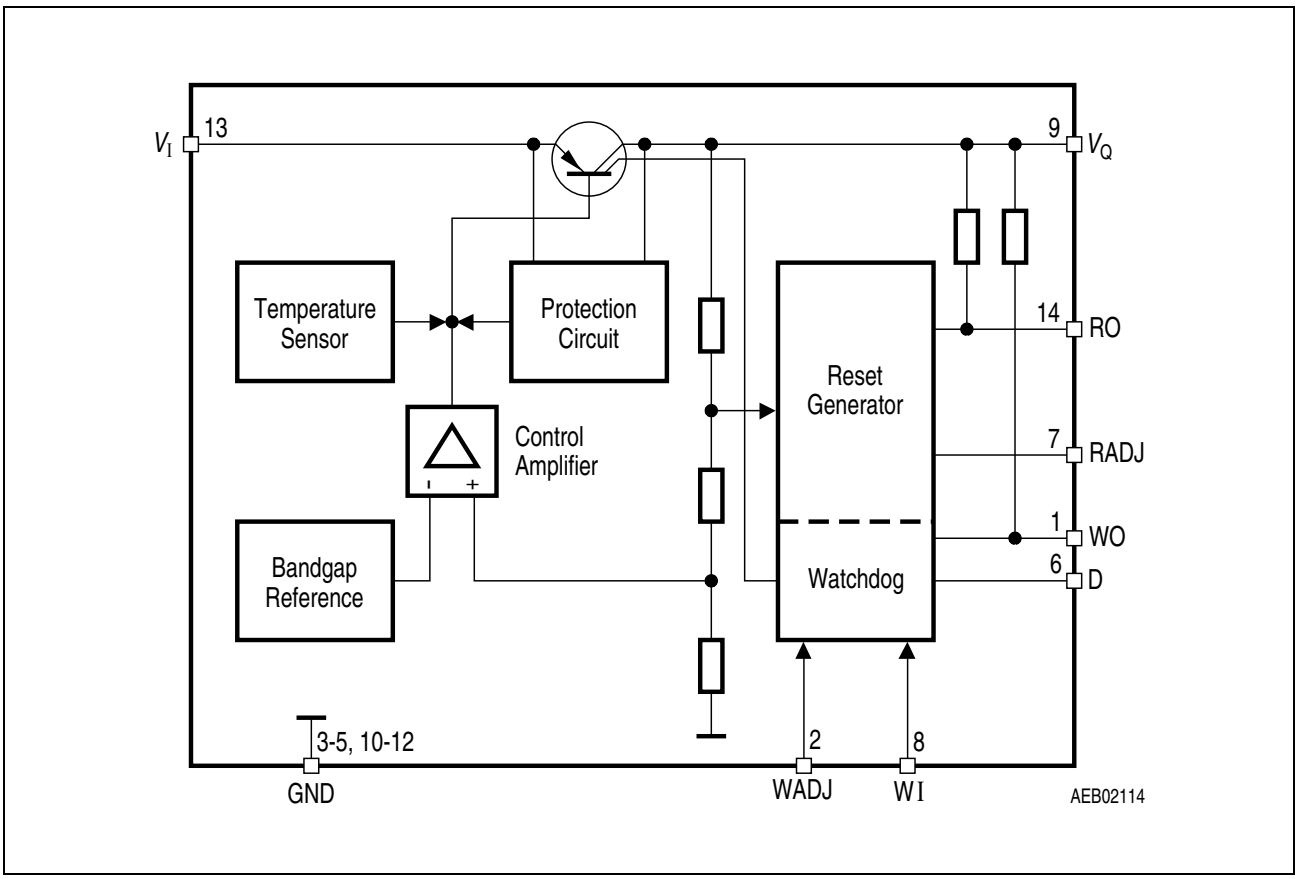


Figure 2 Block Diagram

Table 2 Absolute Maximum Ratings

T_j = -40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input Voltage I					
Voltage	V_I	-42	45	V	–
Current	I_I	–	–	mA	Internally limited
Output Voltage Q					
Voltage	V_Q	-1	25	V	–
Current	I_Q	–	–	mA	Internally limited
Reset Output RO					
Voltage	V_{RO}	-0.3	25	V	–
Current	I_{RO}	-5	5	mA	–
Reset Delay D					
Voltage	V_D	-0.3	7	V	–
Current	I_D	-2	2	mA	–
Reset Switching Threshold Adjust RADJ					
Voltage	V_{RADJ}	-0.3	7	V	–
Current	I_{RADJ}	–	–	mA	Internally limited
Watchdog Input WI					
Voltage	V_{WI}	-0.3	7	V	–
Current	I_{WI}	–	–	mA	Internally limited
Watchdog Output WO					
Voltage	V_{WO}	-0.3	25	V	–
Current	I_{WO}	-5	5	mA	–
Watchdog Adjust WADJ					
Voltage	V_{WADJ}	-0.3	7	V	–
Current	I_{WADJ}	–	–	mA	Internally limited
Ground GND					
Current	I_{GND}	-100	50	mA	–

Table 2 Absolute Maximum Ratings (cont'd)

T_j = -40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Temperatures					
Junction temperature	T_j	-50	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

Note: ESD protection according to MIL Std. 883: ±2 kV.
Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input voltage	V_I	5.5	45	V	–
Junction temperature	T_j	-40	150	°C	–
Thermal Resistance					
Junction ambient	$R_{thj\text{-}a}$	–	80	K/W	1)
Junction pin	$R_{thj\text{-}pin}$	–	30	K/W	Measured to pin 4

1) Package mounted on PCB 80 × 80 × 1.5 mm^3; 35µ Cu; 5µ Sn; Heat Sink Area 6 cm^2; zero airflow.

Note: In the operating range the functions given in the circuit description are fulfilled.

Table 4 Electrical Characteristics

V_I = 13.5 V; -40 °C ≤ T_j ≤ 125 °C (unless otherwise specified)

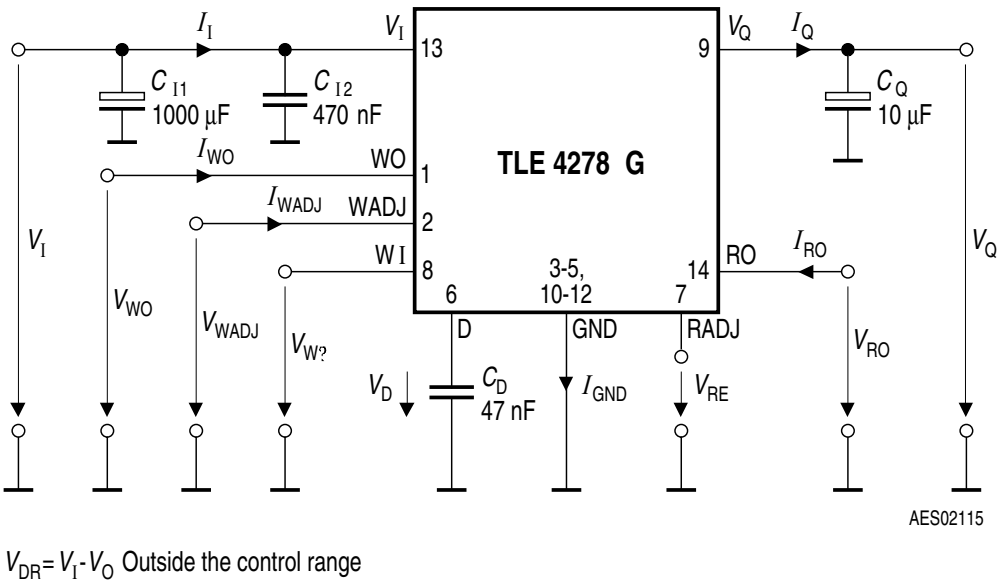
Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Output voltage	V_Q	4.90	5.00	5.10	V	0 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V
Output voltage	V_Q	4.8	5.0	5.2	V	1 mA ≤ I_Q ≤ 50 mA; 28 V ≤ V_I ≤ 45 V
Output current limiting	I_Q	200	400	–	mA	V_Q = 4.8 V
Current consumption $I_q = I_I - I_Q$	$I_{q,o}$	–	180	200	µA	T_j = 25 °C; I_Q = 0 mA
Current consumption $I_q = I_I - I_Q$	$I_{q,o}$	–	210	230	µA	I_Q = 0 mA; T_j = 85 °C
Current consumption $I_q = I_I - I_Q$	$I_{q,150}$	–	5	12	mA	I_Q = 150 mA
Drop voltage $V_{DR} = V_I - V_Q$	V_{dr}	–	0.25	0.5	V	I_Q = 150 mA[1)]
Load regulation	$\Delta V_{Q,lo}$	-30	-5	–	mV	I_Q = 5 to 150 mA; V_I = 6 V
Line regulation	$\Delta V_{Q,li}$	–	5	20	mV	V_I = 6 to 28 V I_Q = 5 mA
Reset Generator						
Reset threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	RADJ connected to GND
Reset headroom	$\Delta V_{Q,rt}$ = ($V_{Q,nom}$ - $V_{Q,rt}$)	180	350	–	mV	I_Q = 10 mA
Reset adjust threshold	$V_{RADJ,th}$	1.28	1.35	1.45	V	V_Q ≥ 3.5 V
Reset low voltage	$V_{RO,l}$	–	0.20	0.40	V	R_{ext} = 10 kΩ to V_Q V_Q ≥ 1 V
Reset high voltage	$V_{RO,h}$	4.5	–	–	V	–
Reset pull-up	R_{RO}	20	30	45	kΩ	Internal connected to V_Q
Charging current	$I_{D,c}$	2	5	8	µA	V_D = 1.0 V

Table 4 Electrical Characteristics (cont'd)

V_I = 13.5 V; -40 °C ≤ T_j ≤ 125 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Upper timing threshold	V_{DU}	1.5	1.9	2.3	V	–
Lower reset timing threshold	V_{DRL}	0.2	0.3	0.4	V	–
Delay time	t_{rd}	12	20	28	ms	C_D = 47 nF
Reset reaction time	t_{rr}	0.4	1.0	2.0	µs	C_D = 47 nF
Watchdog						
Activating threshold	$V_{WADJ,th}$	1.28	1.35	1.45	V	Voltage at WADJ
Current ratio	I_Q/I_{WADJ}	650	720	800	–	I_Q ≤ 10 mA
Slew rate	dV_{WI}/dt	5	–	–	V/µs	From 20% up to 80% V_Q
Watchdog low voltage	V_{WOL}	–	0.2	0.4	V	R_{ext} > 10 kΩ to V_Q
Watchdog high voltage	V_{WOH}	4.5	–	–	V	–
Watchdog pull-up	R_{WO}	20	30	45	kΩ	Internal connected to V_Q
Charge current	$I_{D,wc}$	2	5	8	µA	V_D = 1.0 V
Discharge current	$I_{D,wd}$	0.6	1.3	2.0	µA	V_D = 1.0 V
Upper timing threshold	V_{DU}	1.5	1.9	2.3	V	–
Lower watchdog timing threshold	V_{DWL}	0.5	0.7	0.9	V	–
Watchdog output pulse period	$T_{WD,p}$	42	60	80	ms	C_d = 47 nF
Watchdog output low time	$t_{WD,l}$	7	13	19	ms	V_Q > V_{RT}
Watchdog trigger time	$T_{WI,tr}$	35	47	61	ms	C_d = 47 nF

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value.



$V_{DR} = V_I - V_O$ Outside the control range

Figure 3 Test Circuit

Application Information

Input, Output

The input capacitors C_{I1} and C_{I2} are necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with C_{I1}, the LC circuit of input inductance and input capacitance can be damped. To stabilize the regulation circuit the output capacitor C_Q is necessary. Stability is guaranteed at values $C_Q \geq 10$ µF with an ESR ≤ 5 Ω within the operating temperature range.

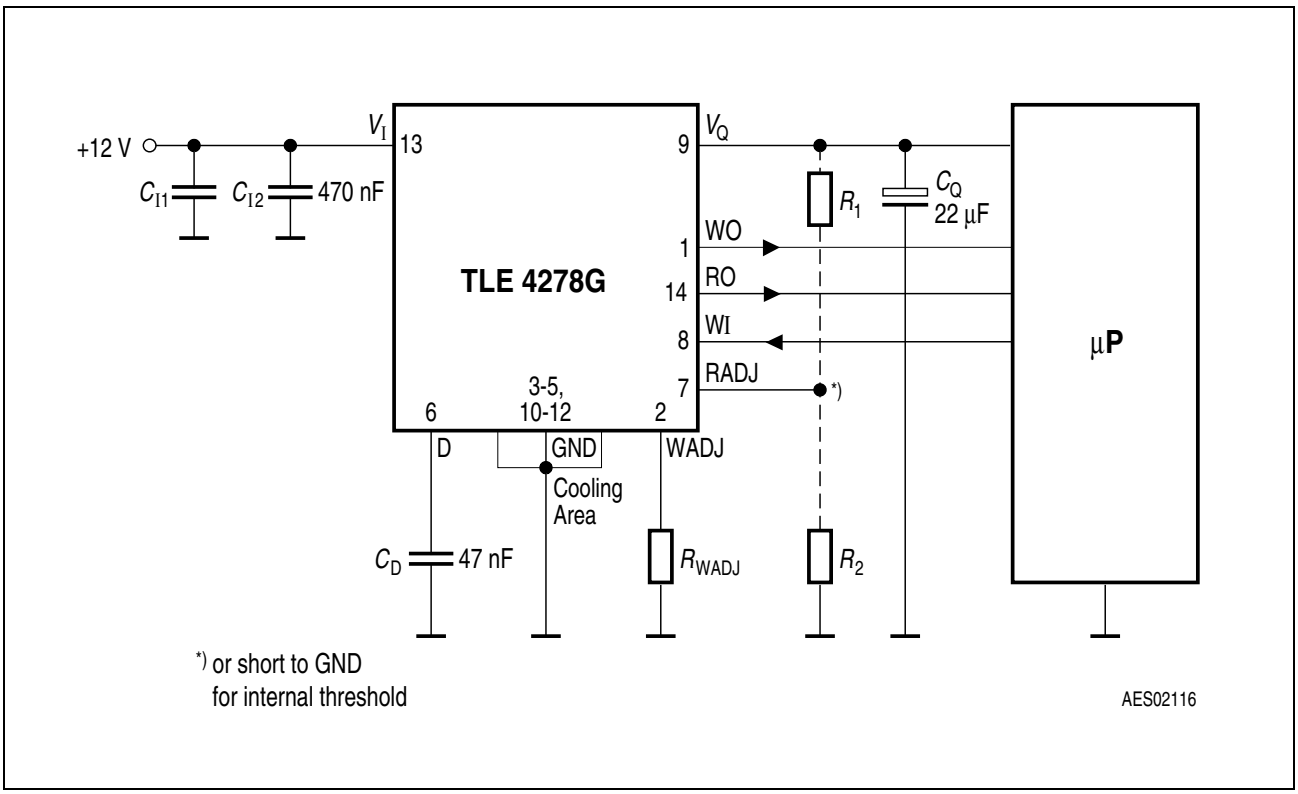


Figure 4 Application Circuit

Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (\Delta t_{rd} \times I_{D,c})/\Delta V \quad (1)$$

Definitions:

- C_D = delay capacitor
- Δt_{rd} = delay time
- $I_{D,c}$ = charge current, typical 5 µA
- $\Delta V = V_{DU}$, typical 1.9 V
- V_{DU} = upper delay switching threshold at C_D for reset delay time

The reset reaction time t_{rr} is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 47 nF. For other values for C_D the reaction time can be estimated using **Equation (2)**:

$$t_{rr} \approx 20\ s/F \times C_D \quad (2)$$

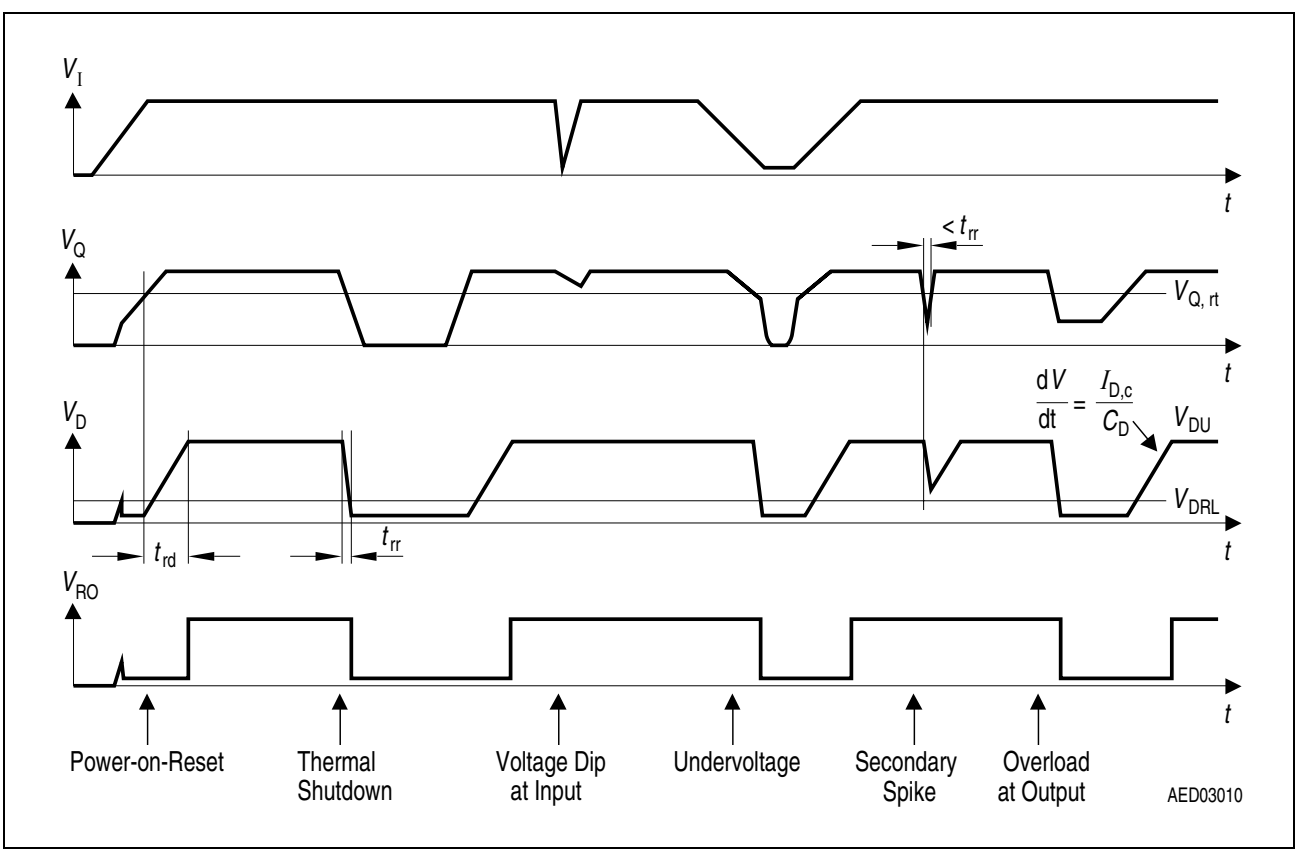


Figure 5 Reset Timing (watchdog disabled)

Reset Switching Threshold

The present default value is 4.65 V. When using the TLE 4278 the reset threshold can be set to 3.5 V < $V_{Q,rt}$ < 4.6 V by connecting an external voltage divider to pin RADJ. The calculation can be easily done since the reset adjust input current can be neglected. If this feature is not needed, the pin has to be connected to GND.

$$V_{Q,rt} = V_{ref} \times (1 + R_1/R_2) \quad (3)$$

Definitions:

- $V_{Q,rt}$ = Reset threshold
- V_{ref} = comparator reference voltage, typical 1.35 V
  (Reset adjust input current ≈ 50 nA)

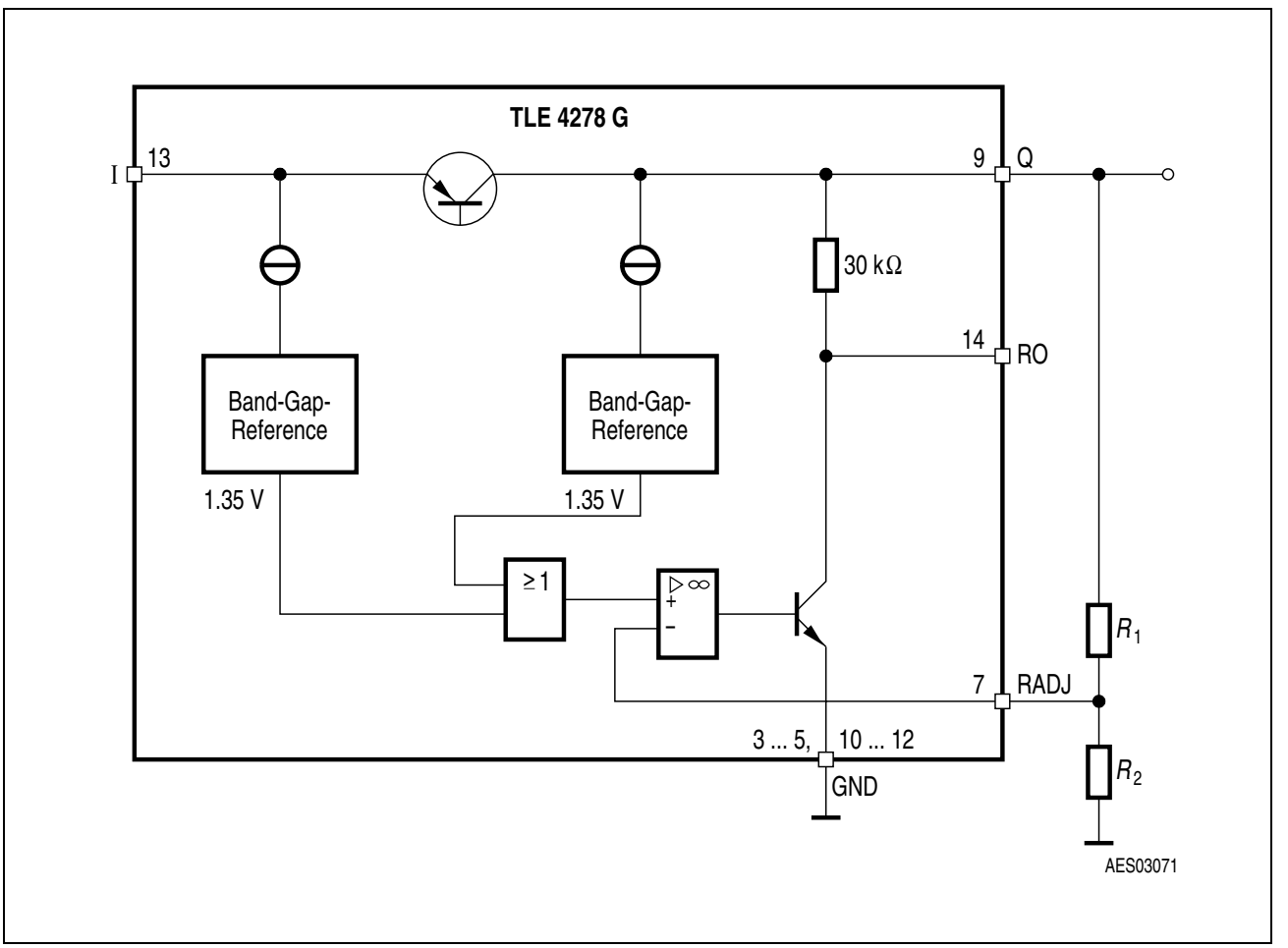


Figure 6

The reset output pin is internally connected to the 5 V output Q via a 30 kΩ pull-up resistor. Down to an output voltage V_Q of typical 1 V the reset LOW signal at pin RO is generated.

For the timing of the reset feature please refer to **Figure 5**.

Watchdog Activating

The calculation of the external resistor which adjusts the watchdog switch off threshold can be done by **Equation (4)**:

$$R_{WADJ} = V_{WADJ,th} \times (I_Q/I_{WADJ})/I_{Q,act} \quad (4)$$

Definitions:

- $V_{WADJ,th}$ = switch off threshold, typical 1.35 V
- I_Q/I_{WADJ} = current ratio, typical 720
- $I_{Q,act}$ = switch off load current

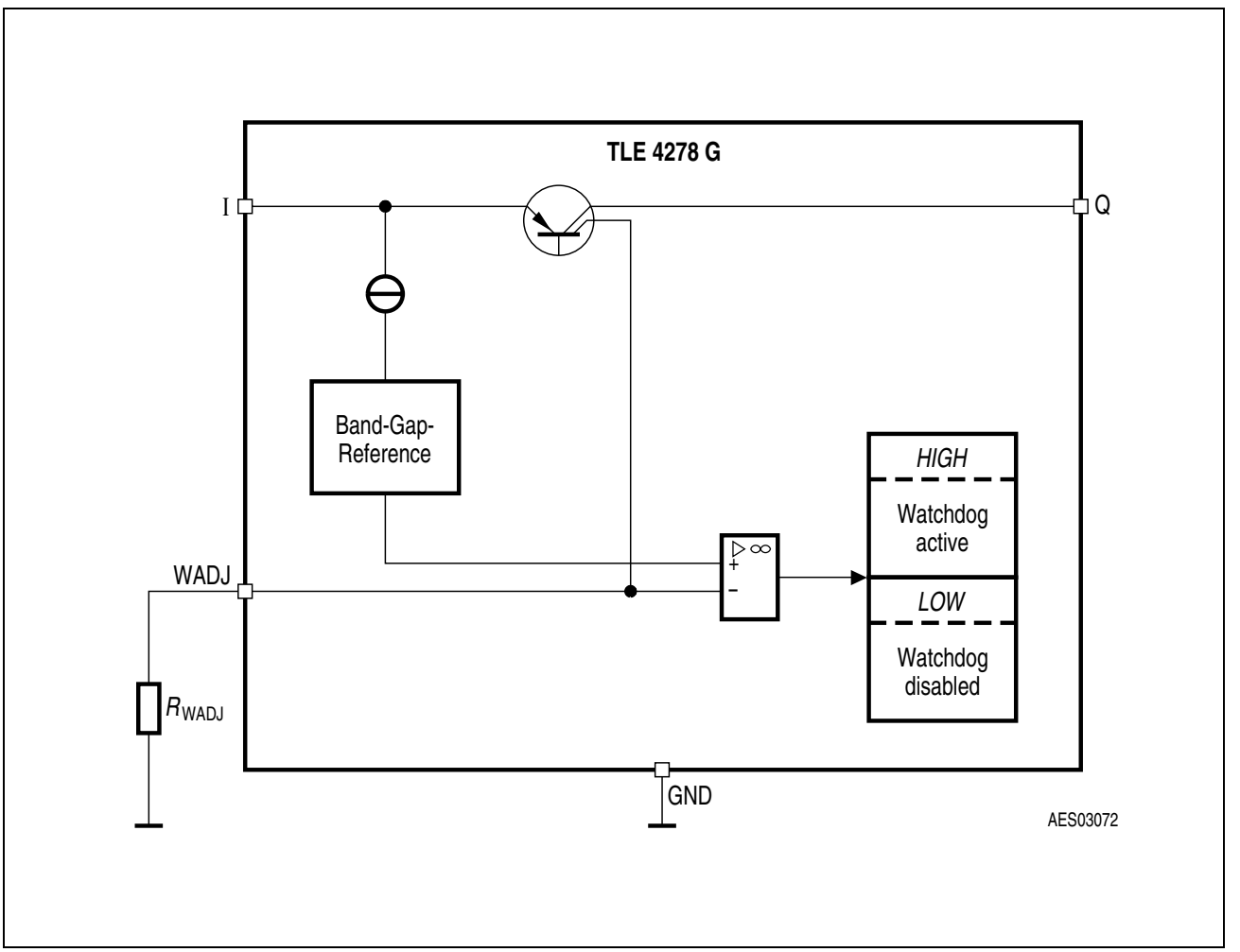


Figure 7

Watchdog Timing

The frequency of the watchdog pulses has to be higher than the minimum pulse sequence which is set by the external reset delay capacitor C_D. Calculation can be done according to the formulas given in **Figure 8**.

The watchdog output is internally connected to the output Q via a 30 kΩ pull-up resistor. To generate a watchdog created reset signal for the microcontroller the pin WO can be connected to the reset input of the microcontroller. It is also allowed to parallel the watchdog out to the reset out.

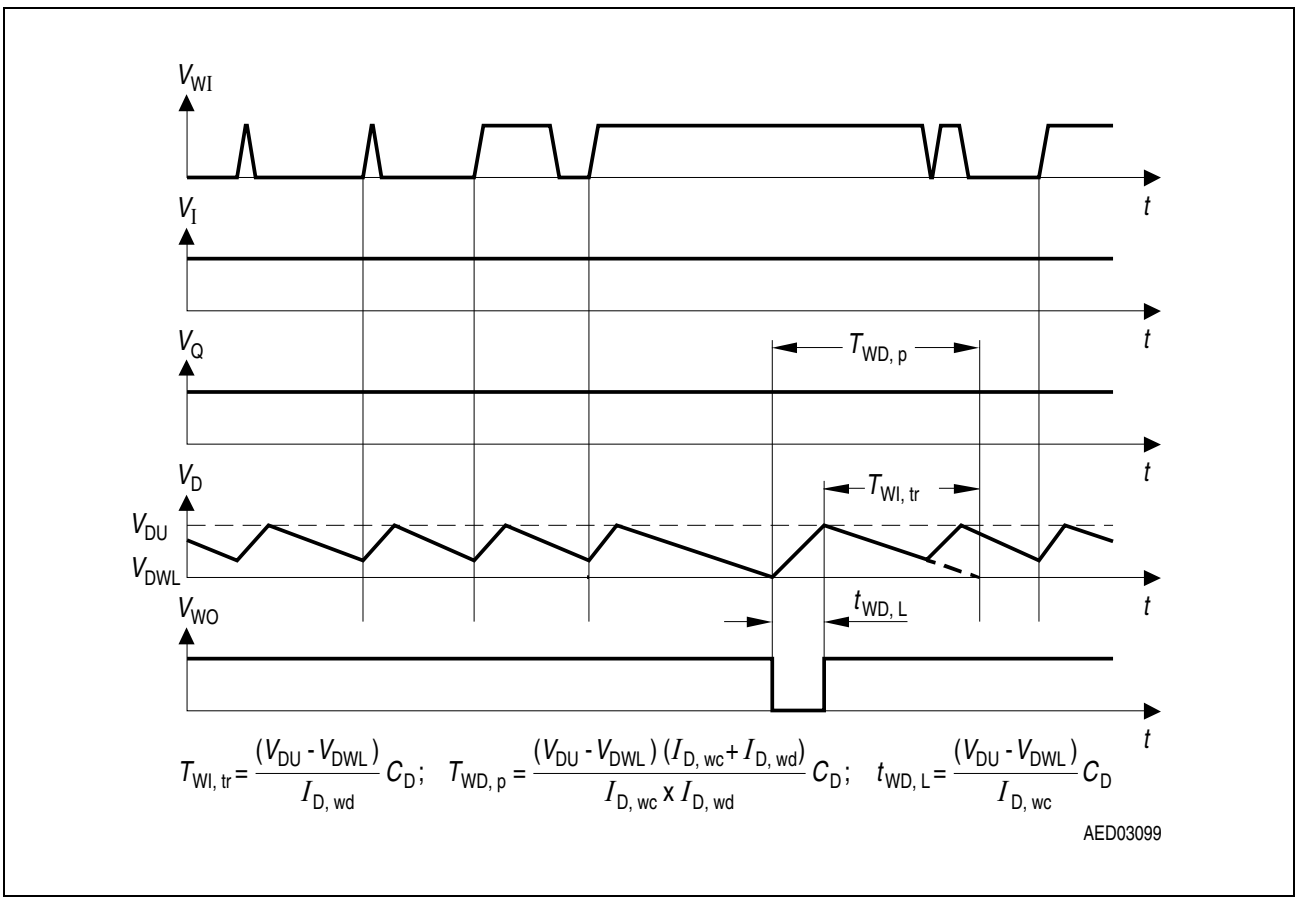
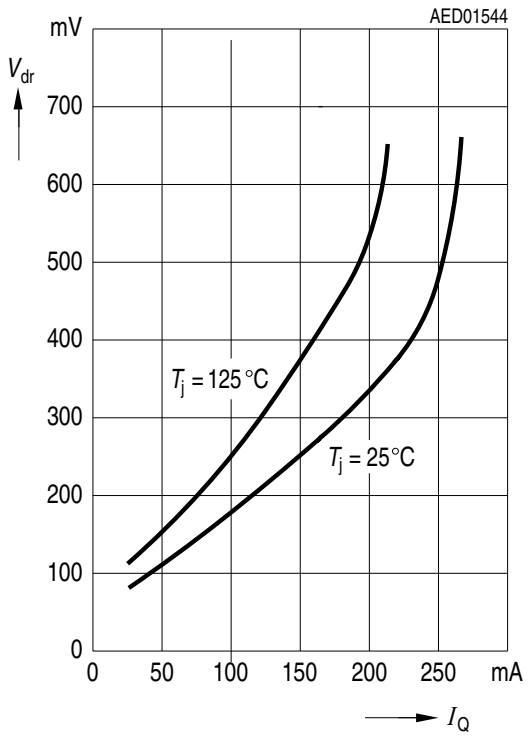


Figure 8 Timing of the Watchdog Function

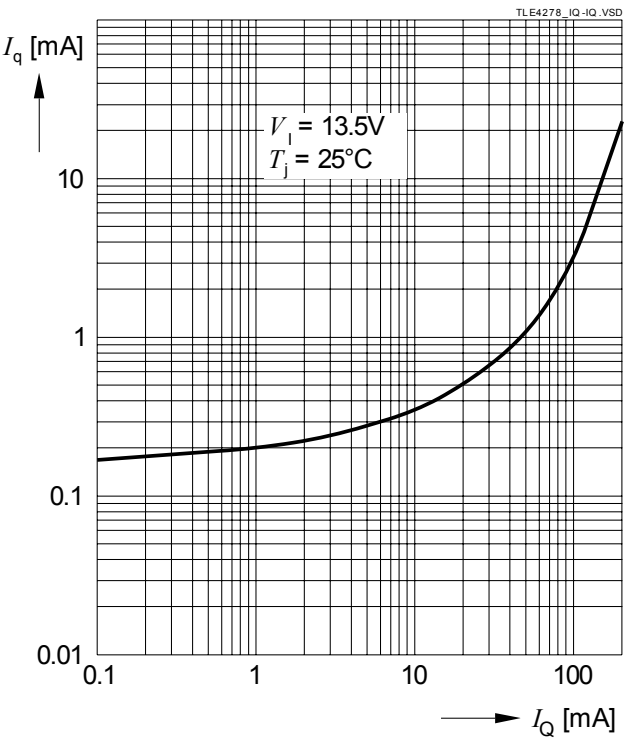
Table 5 Hints for Unused Pins

Symbol	Function	Connect to
RO	Reset output	open
D	Reset delay	open or to output Q
RADJ	Reset switching threshold adjust	GND
WI	Watchdog input	GND
WO	Watchdog output	open
WADJ	Watchdog adjust	[1] to output Q via a 270 kΩ resistor: Watchdog always active [2] to GND: Watchdog disabled

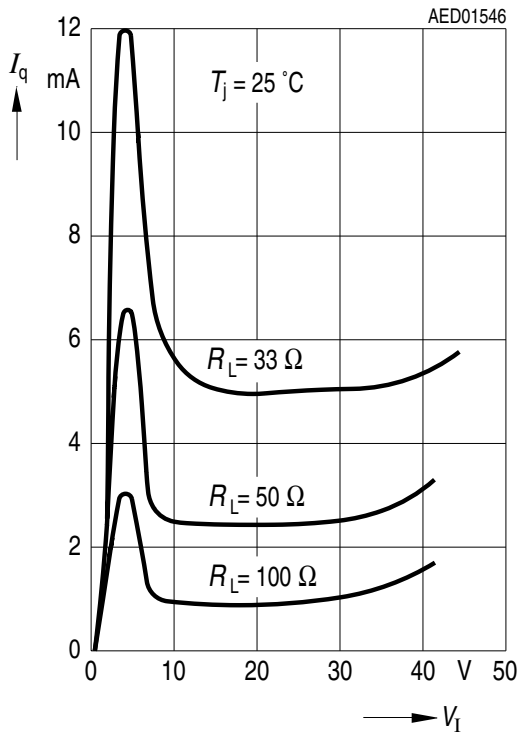
Drop Voltage V_{dr} versus Output Current I_Q



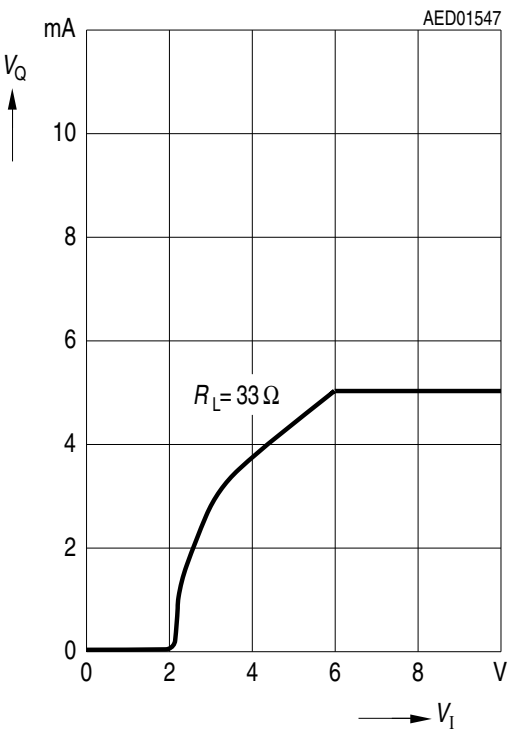
Current Consumption I_q versus Output Current I_Q



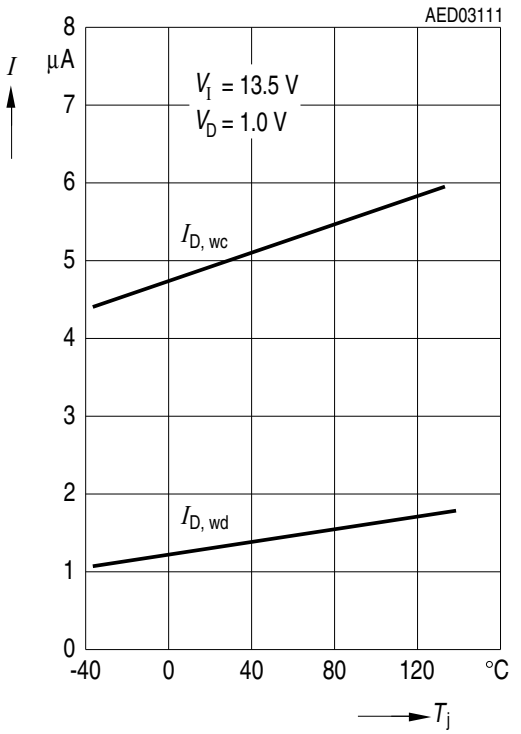
Current Consumption I_q versus Input Voltage V_I



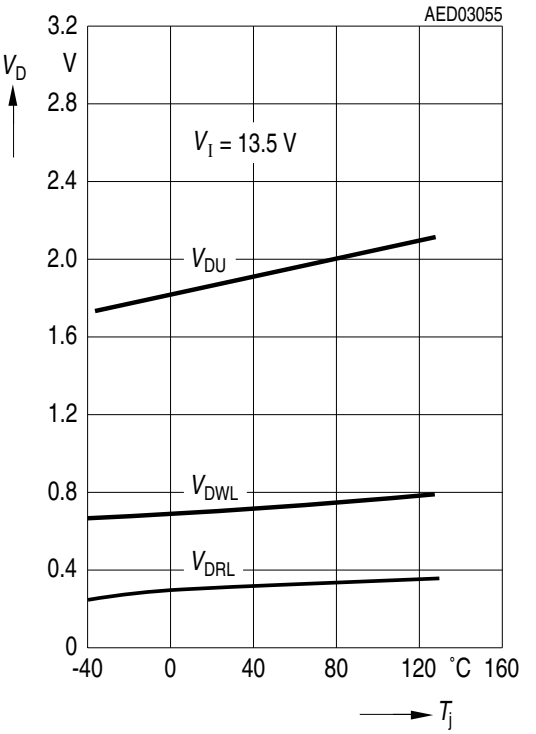
Output Voltage V_Q versus Input Voltage V_I



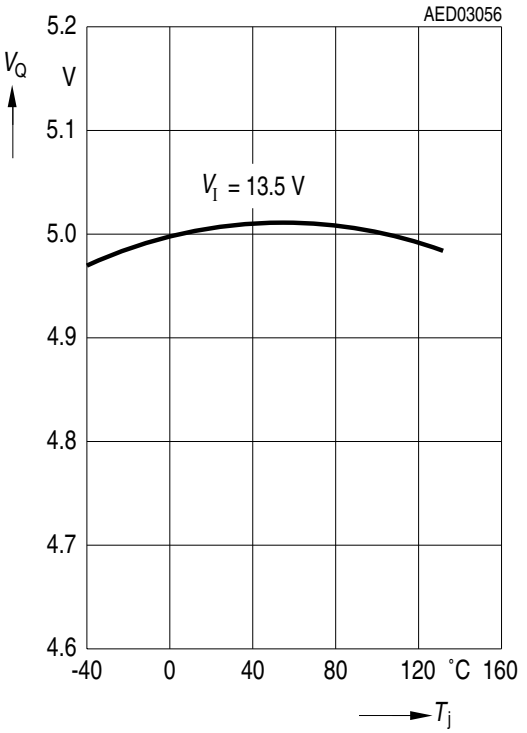
Charge Current $I_{D,wc}$ and Discharge Current $I_{D,wd}$ versus Temperature T_j



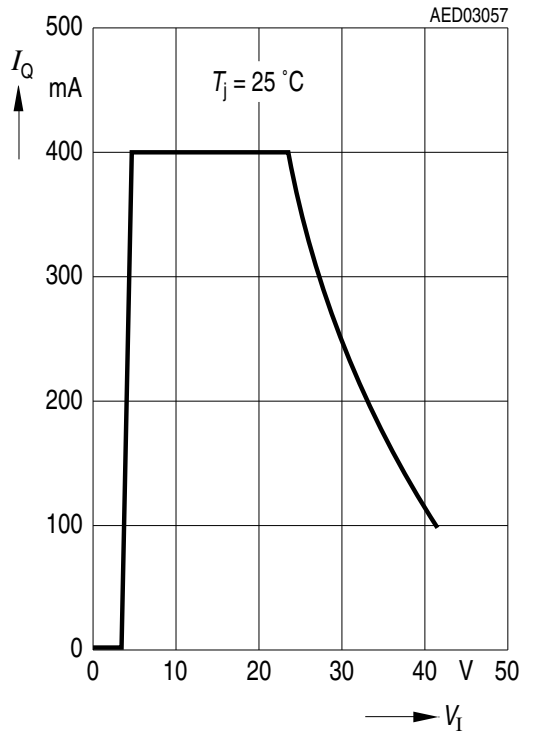
Switching Voltage V_{DU}, V_{DWL} and V_{DRL} versus Temperature T_j



Output Voltage V_Q versus Temperature T_j



Output Current Limit I_Q versus Input Voltage V_I



Package Outlines

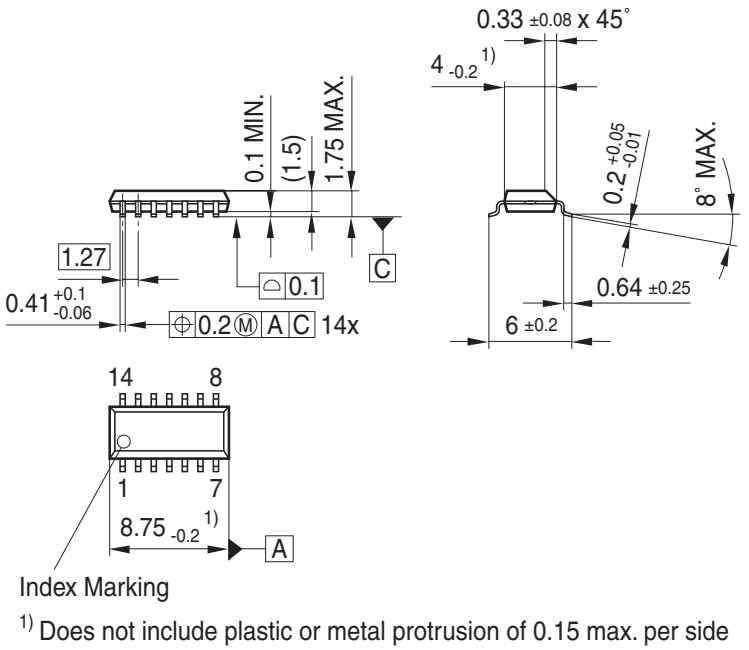


Figure 9 **P-DSO-14-8** (Plastic Dual Small Outline)

Revision History

Version	Date	Changes
Rev. 1.2	2004-01-01	Final Data Sheet
Rev. 1.3	2005-04-29	* Typ. Perf. Char. Graph “Iq vs. IQ”: Replaced by a logarithmic graph in order to precise at low IQ. * Order number typo corrected

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SMD = Surface Mounted Device

Dimensions in mm

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