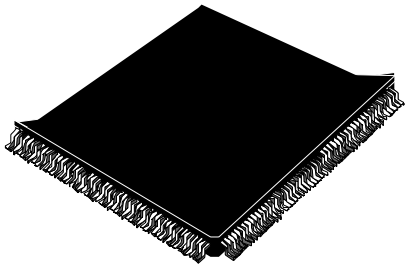
ADE3000 ADE3050 ADE3100 ADE3200 ADE3250 ADE3300

LCD Display Engines with Integrated DVI, ADC and YUV Ports

The ADE3xxx is a family of highly integrated display engine ICs, enabling the most advanced, flexible, and cost-effective system-on-chip solutions for LCD display applications. The ADE3xxx line-up covers the full range of applications from XGA analog only to dual SXGA Smart Panel designs. All twelve ADE3xxx devices are pin-to-pin compatible and use a common software platform.

Feature Overview

- Programmable Context Sensitive™ Scaling
- High-quality up-scaling and down-scaling
- Dual Input: DVI / VGA
- Integrated 9-bit ADC/PLL
- Integrated DVI-Rx
- IQSync™ AutoSetup
- Integrated programmable timing controller
- Integrated Pattern generator
- Perfect Picture™ Technology
- sRGB 3D Color Warp
- Integrated OSD
- Advanced EMI reduction features
- Framelock operation with Safety Mode™
- Serial I²C interface
- Low power 0.18 µm process technology



208-pin PQFP Package

Product Selector

Product	Input Interface Support			Output Format Support	
	Analog	DVI	YUV	Resolution	TCON
ADE3000	***X***		***X***	Up to XGA 75Hz	
ADE3000T	***X***		***X***	Up to XGA 75Hz	***X***
ADE3000SX	***X***		***X***	Up to SXGA 75Hz	
ADE3000SXT	***X***		***X***	Up to SXGA 75Hz	***X***
ADE3050		***X***	***X***	Up to XGA 75Hz	
ADE3050T		***X***	***X***	Up to XGA 75Hz	***X***
ADE3050SX		***X***	***X***	Up to SXGA 75Hz	
ADE3050SXT		***X***	***X***	Up to SXGA 75Hz	***X***
ADE3100	***X***	***X***	***X***	Up to XGA 75Hz	
ADE3200	***X***	***X***	***X***	Up to XGA 75Hz	***X***
ADE3250	***X***	***X***	***X***	Up to SXGA 75Hz	***X***
ADE3300	***X***	***X***	***X***	Up to SXGA 75Hz	

Third Generation Context Sensitive™ Scaler

- Sharper text with Edge Enhancement
- RAM based coefficients for unique customization
- 5:1 upscale and 2:1 downscale
- Independent X - Y axis zoom and shrink
- Bob de-interlacing eliminates jaggies and motion artifacts

Analog RGB input

- 140MHz 9-bit ADC
- Ultra low jitter digital linelock PLL
- Composite Sync and Sync on Green support

Secure DVI™ Receiver

- Single Link DVI receiver
- Input Pixel Rate from 25 to140 MHz
- Low power mode with activity detection
- Compatibility with all DVI compliant transmitters

Digital TV Video Input

- VESA VIP 1.1, 2.0 and CCIR656 compliant
- 25 to 75 MHz input clock

IQsync™ AutoSetup

- AutoSetup configures phase, clock, level, and position
- Supports continuous calibration for reduced user intervention
- Detects activity on all inputs and selects the active source
- Compatible with all standard VESA and GTF modes

Perfect Picture™ Technology

- Video & Picture highlight zoning
- Supports up to 7 different windows
- Independent window controls for contrast brightness, sharpness, and color

Perfect Color™ Technology

- Programmable 3D color warp
- Digital brightness, contrast, hue, and saturation gamma controls for all inputs
- Simple white point control
- Compatible with sRGB standard
- True color dithering for 12- and 18-bit panels
- Temporal and spatial dithering
- 30-bit programmable gamma table

OSD Engine

- 256 RAM based 12x18 characters
- 1 and 4-bit per pixel color characters
- Bordering, shadowing, transparency, fade-in, and fade-out
- Supports font rotation
- Up to 4 sub windows
- 32 entry TrueColor LUT

Programmable Timing Controller (TCON)

- Highly-programmable support for XGA, TTL and RSDS SmartPanels
- Dual function TTL and RSDS outputs
- Advanced flicker detection and reduction
- 12 programmable timing signals for row/ column control
- Wide range of drivers & TCON compatibility
- Simulation tools for easy programming
- Supports complex polarity generation for IPS panels

Advanced EMI Reduction Features

- Flexible data inversion / transition minimization, single, dual, and separate
- Per pin delay, 0 to 6ns in 0.4ns increments
- Adaptive Slew Rate control outputs
- Supports 18/24/36/48-bit RSDS outputs
- Differential clock
- Spread spectrum -programmable digital FM modulation of the output clock with no external components

Output Format

- Supports resolutions up to SXGA @ 75Hz
- Supports 6 or 8-bit Panels
- Support double or single pixel wide formats

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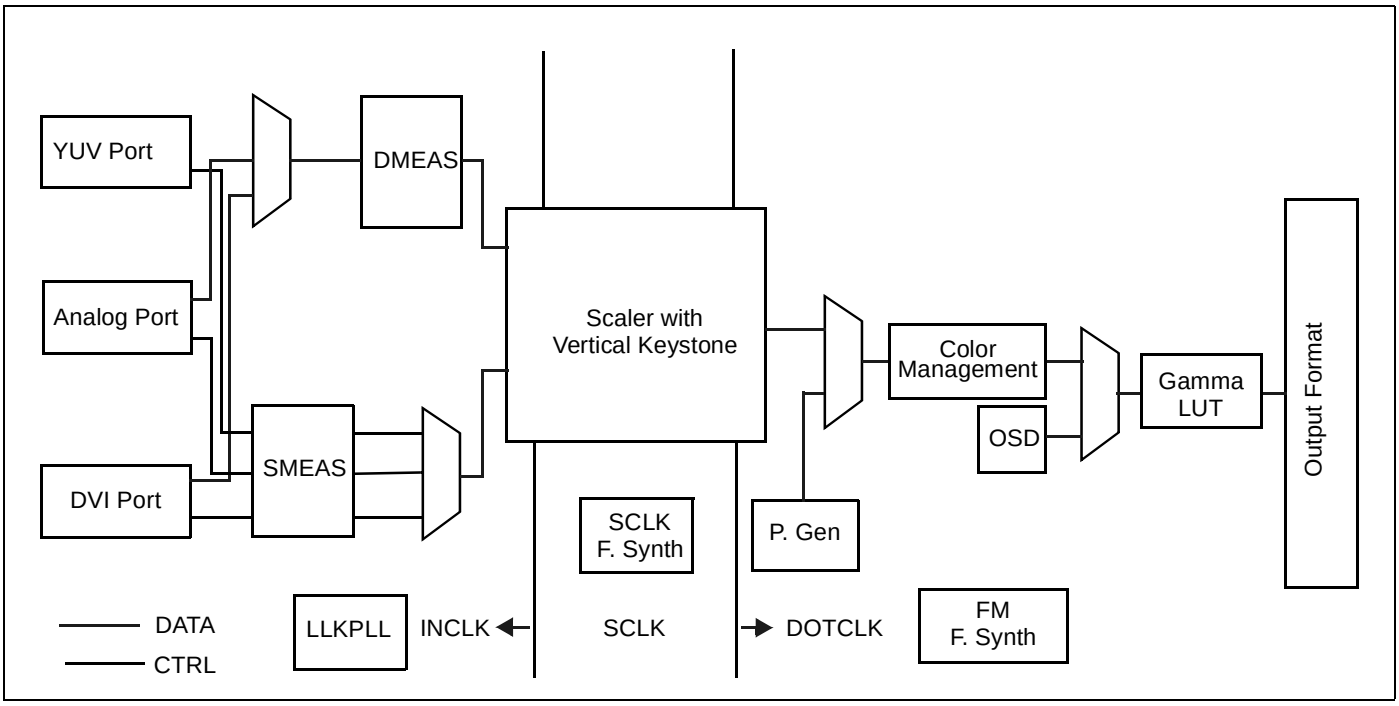
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1 General Description

Figure 1: ADE3XXX Block Diagram



The ADE3XXX family of devices is capable of implementing all of the advanced features of today's LCD monitor products. For maximum flexibility, an external microcontroller (MCU) is used for controlling the ADE3XXX and other monitor functions.

The ADE3XXX architecture unburdens the MCU from all data-intensive pixel manipulations, providing an optimal blend of feature and code customization without incurring the cost of a 16-bit processor or memory. The key interactions between the monitor MCU and the ADE3XXX can be broken down into the features shown in the table below.

Table 1: ADE3xxx Features (Sheet 1 of 2)

Feature	Description of ADE3XXX Operation	Blocks Used	Pages
Power Up / Initialize	When power is first applied, the ADE3XXX is asynchronously reset from a pin. The MCU typically programs the ADE3XXX with a number of default values and sets up the ADE3XXX to identify activity on any of the input pins. All preconfigured values and RAMs, such as DVI settings, line-lock PLL settings, video input modes (YUV), OSD characters, LCD timing values (output sequencer), scale kernels, gamma curves, sRGB color warp, APC dithering, output pin configuration (OMUX), etc. can be preloaded into the ADE3XXX. The typical end state is that the ADE3XXX is initialized into a low power mode, ready to turn active once the power button is pressed.	GLBL SMEAS DVI LLK ADC YUV OSD SCALER GAMMA SRGB OUTSEQ TCON APC OMUX	13 32 22 19 18 29 66 49 74 64 52 55 74 75
Activity Detect	When the monitor has been powered on, the inputs can be monitored for active video sources. Based on the activity monitors, the MCU chooses an input or power down state.	SMEAS	32

Table 1: ADE3xxx Features (Sheet 2 of 2)

Feature	Description of ADE3XXX Operation	Blocks Used	Pages
Sync / Timing Measurement	Once an input source is selected, all available information on frequencies and line/pixel counts is measured for the selected source and made available to the MCU.	SMEAS	32
Mode Set	Once the MCU has determined the matching video mode or calculated a video mode using a GTF algorithm, the datapath is programmed to drive the flat panel. Clock frequencies for the internal memory and datapath are also set at this time.	GLBL LLK SRT DMUX SMUX SCALER PNL	13 19 30 42 40 49 48
Autotune	When the MCU calls for an autotune, the MCU sets up an iterative loop to search for the best phase, gain, offset, etc. At each step of the loop, the MCU kicks off a test in which the ADE3XXX which performs extensive statistical analysis of the incoming data stream. The results of the analysis are made available to the MCU which is responsible for the optimization algorithm.	DMEAS LLK ADC SMUX SRT	47 19 18 40 30
Digital Contrast / Brightness	In response to user OSD control, the MCU can program single 8b registers that set brightness and contrast for each color channel independently.	SRGB	64
White Point Control	In response to user OSD control, the MCU can program three 8b registers that set the white point for the output.	SRGB	64
Gamma Adjustment	The MCU can program the gamma RAMs to implement 10b accurate color transformations.	GAMMA	74
SRGB Control	The SRGB block allows simple, intuitive color control with just a few registers.	SRGB	64
Pattern Generation	For production testing, the ADE3XXX can be programmed by the MCU to output a wide set of test patterns.	PGEN	60
Flicker Reduction	For smart panel applications, the MCU can set up the flicker detection block to report any correlation with the polarity inversion signal. The MCU can then change the polarity inversion to a non-correlating pattern to eliminate flicker.	FLICKER TCON	72 55
HDCP	The ADE3XXX contains the BlockCipher and Decryption functions - interactions over DDC are managed by the MCU for maximum flexibility. The MCU models the slow (frame rate, e.g. 60 Hz) authentication handshaking and state machine whereas the ADE3XXX handles the fast (line rate, e.g. 50 kHz) decryption state machine.	HDCP	27
Backlight Control	The ADE3XXX provides two PWM outputs for direct control of the power components in a typical backlight. The MCU sets up the registers and enables the function.	PWM	77
Low Power State	To enter a low power state, the MCU can gate of most of the clocks and put the analog blocks into a low power standby state. The DVI block will still report activity in standby, allowing "wake on connection" operation.	GLBL	13

1.1 Pin Description

Table 2: Pin Description (Sheet 1 of 7)

Pin #	Name	Type	Description
1	YUV6	Input	TV Video Input Port: Data 6
2	YUV5	Input	TV Video Input Port: Data 5
3	YUV4	Input	TV Video Input Port: Data 4
4	YUV3	Input	TV Video Input Port: Data 3
5	YUV2	Input	TV Video Input Port: Data 2

Table 2: Pin Description (Sheet 2 of 7)

Pin #	Name	Type	Description
6	YUV1	Input	TV Video Input Port: Data 1
7	YUV0	Input	TV Video Input Port: Data 0
8	YUVCLK	Input	TV Video Input Port: Clock
9	DVDD18	Power	Digital 1.8V VDD
10	DGND	Power	Digital Ground
11	DVDD18	Power	Digital 1.8V VDD
12	DGND	Power	Digital Ground
13	AGND	Power	Analog Ground
14	AVDD18	Power	Analog 1.8V VDD
15	AVDD33	Power	Analog 3.3V VDD
16	RX2M	Input	DVI Receiver Channel 2 MINUS input (RED)
17	RX2P	Input	DVI Receiver Channel 2 PLUS input (RED)
18	AGND	Power	Analog Ground
19	AVDD33	Power	Analog 3.3V VDD
20	RX1M	Input	DVI Receiver Channel 1 MINUS input (GREEN)
21	RX1P	Input	DVI Receiver Channel 1 PLUS input (GREEN)
22	AVDD33	Power	Analog 3.3V VDD
23	RX0M	Input	DVI Receiver Channel 0 MINUS input (BLUE)
24	RX0P	Input	DVI Receiver Channel 0 PLUS input (BLUE)
25	AVDD33	Power	Analog 3.3V VDD
26	AGND	Power	Analog Ground
27	RXCP	Input	DVI Receiver Clock Channel PLUS input
28	RXCM	Input	DVI Receiver Clock Channel MINUS input
29	AVDD33	Power	Analog 3.3V VDD
30	REXT	Passive	1% 475 Ohm resistor to Analog 3.3V VDD
31	AVDD33	Power	Analog 3.3V VDD
32	AVDD33	Power	Analog 3.3V VDD
33	AGND	Power	Analog Ground
34	AGND	Power	Analog Ground
35	AGND	Power	Analog Ground
36	RBIAS	Passive	1% 2.0 kOhm resistor to Analog Ground
37	AGND	Power	Analog Ground
38	AVDD18	Power	Analog 1.8V VDD
39	AGND	Power	Analog Ground
40	AVDD33	Power	Analog 3.3V VDD
41	AGND	Power	Analog Ground
42	AVDD18	Power	Analog 1.8V VDD
43	AGND	Power	Analog Ground
44	AVDD18	Power	Analog 1.8V VDD

Table 2: Pin Description (Sheet 3 of 7)

Pin #	Name	Type	Description
45	AGND	Power	Analog Ground
46	AVDD18	Power	Analog 1.8V VDD
47	XGND	Power	Crystal Oscillator Ground
48	XTAL_IN	Input	Crystal Oscillator Input
49	XTAL_OUT	Output	Crystal Oscillator Output
50	XVDD18	Power	Crystal Oscillator 1.8V VDD
51	LVDD18	Power	Line Lock PLL 1.8V VDD
52	LGND	Power	Line Lock PLL Ground
53	CSYNC	Input	Composite Sync Input - for Sync On Green
54	VSYNC	Input	Vertical Sync Input
55	HSYNC	Input	Horizontal (or Composite) Sync Input
56	AGND	Power	Analog Ground
57	AGND	Power	Analog Ground
58	AVDD33	Power	Analog 3.3V VDD
59	AVDD33	Power	Analog 3.3V VDD
60	AGND	Power	Analog Ground
61	AVDD18	Power	Analog 1.8V VDD
62	AGND	Power	Analog Ground
63	REFB	Passive	1% 15.0 kOhm resistor to Analog Ground
64	REFMB	Passive	Connect to Analog Ground
65	REFPB	Passive	470nF capacitor to Analog Ground
66	AGND	Power	Analog Ground
67	AGND	Power	Analog Ground
68	INB	Input	Analog Video Port: Blue Channel input
69	AVDD33	Power	Analog 3.3V VDD
70	AVDD33	Power	Analog 3.3V VDD
71	REFCB	Passive	100nF capacitor to Analog Ground
72	AGND	Power	Analog Ground
73	AVDD18	Power	Analog 1.8V VDD
74	AVDD18	Power	Analog 1.8V VDD
75	REFG	Passive	1% 15.0 kOhm resistor to Analog Ground
76	REFMG	Passive	Connect to Analog Ground
77	REFPG	Passive	470nF capacitor to Analog Ground
78	AGND	Power	Analog Ground
79	AGND	Power	Analog Ground
80	ING	Input	Analog Video Port: Green Channel input
81	AVDD33	Power	Analog 3.3V VDD
82	AVDD33	Power	Analog 3.3V VDD
83	REFCG	Passive	100nF capacitor to Analog Ground

Table 2: Pin Description (Sheet 4 of 7)

Pin #	Name	Type	Description
84	AGND	Power	Analog Ground
85	AVDD18	Power	Analog 1.8V VDD
86	AVDD18	Power	Analog 1.8V VDD
87	REFR	Passive	1% 15.0 kOhm resistor to Analog Ground
88	REFMR	Passive	Connect to Analog Ground
89	REFPR	Passive	470nF capacitor to Analog Ground
90	AGND	Power	Analog Ground
91	AGND	Power	Analog Ground
92	INR	Input	Analog Video Port: Red Channel input
93	AVDD33	Power	Analog 3.3V VDD
94	AVDD33	Power	Analog 3.3V VDD
95	REFCR	Passive	100nF capacitor to Analog Ground
96	AGND	Power	Analog Ground
97	AVDD18	Power	Analog 1.8V VDD
98	AVDD18	Power	Analog 1.8V VDD
99	TST_SCAN	Input	Connect to Digital Ground
100	DGND	Power	Digital Ground
101	DVDD33	Power	Digital 3.3V VDD
102	OBA7	Output	Output Port A: Blue Data 7
103	OBA6	Output	Output Port A: Blue Data 6
104	OBA5	Output	Output Port A: Blue Data 5
105	DGND	Power	Digital Ground
106	OBA4	Output	Output Port A: Blue Data 4
107	OBA3	Output	Output Port A: Blue Data 3
108	OBA2	Output	Output Port A: Blue Data 2
109	OBA1	Output	Output Port A: Blue Data 1
110	OBA0	Output	Output Port A: Blue Data 0
111	DVDD33	Power	Digital 3.3V VDD
112	DGND	Power	Digital Ground
113	OGA7	Output	Output Port A: Green Data 7
114	OGA6	Output	Output Port A: Green Data 6
115	OGA5	Output	Output Port A: Green Data 5
116	OGA4	Output	Output Port A: Green Data 4
117	OGA3	Output	Output Port A: Green Data 3
118	OGA2	Output	Output Port A: Green Data 2
119	OGA1	Output	Output Port A: Green Data 1
120	OGA0	Output	Output Port A: Green Data 0
121	DVDD18	Power	Digital 1.8V VDD
122	DGND	Power	Digital Ground

Table 2: Pin Description (Sheet 5 of 7)

Pin #	Name	Type	Description
123	DVDD18	Power	Digital 1.8V VDD
124	DGND	Power	Digital Ground
125	DVDD33	Power	Digital 3.3V VDD
126	ORA7	Output	Output Port A: Red Data 7
127	ORA6	Output	Output Port A: Red Data 6
128	ORA5	Output	Output Port A: Red Data 5
129	ORA4	Output	Output Port A: Red Data 4
130	ORA3	Output	Output Port A: Red Data 3
131	ORA2	Output	Output Port A: Red Data 2
132	ORA1	Output	Output Port A: Red Data 1
133	ORA0	Output	Output Port A: Red Data 0
134	DVDD33	Power	Digital 3.3V VDD
135	DGND	Power	Digital Ground
136	ODE	Output	Output Data Enable
137	OHS	Output	Output Horizontal Sync
138	OCLK	Output	Output Clock
139	OVS	Output	Output Vertical Sync
140	DVDD18	Power	Digital 1.8V VDD
141	DGND	Power	Digital Ground
142	DVDD18	Power	Digital 1.8V VDD
143	DGND	Power	Digital Ground
144	OBB7	Output	Output Port B: Blue Data 7
145	OBB6	Output	Output Port B: Blue Data 6
146	OBB5	Output	Output Port B: Blue Data 5
147	OBB4	Output	Output Port B: Blue Data 4
148	DVDD33	Power	Digital 3.3V VDD
149	DGND	Power	Digital Ground
150	OBB3	Output	Output Port B: Blue Data 3
151	OBB2	Output	Output Port B: Blue Data 2
152	OBB1	Output	Output Port B: Blue Data 1
153	OBB0	Output	Output Port B: Blue Data 0
154	OGB7	Output	Output Port B: Green Data 7
155	OGB6	Output	Output Port B: Green Data 6
156	OGB5	Output	Output Port B: Green Data 5
157	OGB4	Output	Output Port B: Green Data 4
158	DVDD33	Power	Digital 3.3V VDD
159	DGND	Power	Digital Ground
160	OGB3	Output	Output Port B: Green Data 3
161	OGB2	Output	Output Port B: Green Data 2

Table 2: Pin Description (Sheet 6 of 7)

Pin #	Name	Type	Description
162	OGB1	Output	Output Port B: Green Data 1
163	OGB0	Output	Output Port B: Green Data 0
164	DVDD18	Power	Digital 1.8V VDD
165	DGND	Power	Digital Ground
166	DVDD18	Power	Digital 1.8V VDD
167	DGND	Power	Digital Ground
168	ORB7	Output	Output Port B: Red Data 7
169	ORB6	Output	Output Port B: Red Data 6
170	ORB5	Output	Output Port B: Red Data 5
171	ORB4	Output	Output Port B: Red Data 4
172	DVDD33	Power	Digital 3.3V VDD
173	DGND	Power	Digital Ground
174	ORB3	Output	Output Port B: Red Data 3
175	ORB2	Output	Output Port B: Red Data 2
176	ORB1	Output	Output Port B: Red Data 1
177	ORB0	Output	Output Port B: Red Data 0
178	DVDD18	Power	Digital 1.8V VDD
179	DGND	Power	Digital Ground
180	DVDD18	Power	Digital 1.8V VDD
181	DGND	Power	Digital Ground
182	CLKOUT	Output	Not to be connected - Reserved
183	CLKIN	Input	To be connected to Digital Ground - Reserved
184	TCON_IN	Input	TCON input
185	DVDD33	Power	Digital 3.3V VDD
186	DGND	Power	Digital Ground
187	TCON7	Input/Output	TCON Output 7/YUV Input 15
188	TCON6	Input/Output	TCON Output 6/YUV Input 14
189	TCON5	Input/Output	TCON Output 5/YUV Input 13
190	TCON4	Input/Output	TCON Output 4/YUV Input 12
191	DVDD18	Power	Digital 1.8V VDD
192	DGND	Power	Digital Ground
193	DVDD18	Power	Digital 1.8V VDD
194	DGND	Power	Digital Ground
195	TCON3	Input/Output	TCON Output 3/YUV Input 11
196	TCON2	Input/Output	TCON Output 2/YUV Input 10
197	TCON1	Input/Output	TCON Output 1/YUV Input 9
198	TCON0	Input/Output	TCON Output 0/YUV Input 8
199	DVDD18	Power	Digital 1.8V VDD
200	DGND	Power	Digital Ground

Table 2: Pin Description (Sheet 7 of 7)

Pin #	Name	Type	Description
201	DVDD18	Power	Digital 1.8V VDD
202	DGND	Power	Digital Ground
203	SCL	Input	I2C Clock
204	SDA	Open Drain I/O	I2C Data
205	XCLK	Output	Crystal Clock Buffered Output
206	XCLK_EN	Input	Crystal Clock Output Enable 0: XCLK output disabled 1: XCLK output active
207	$\overline{\text{RESETN}}$	Input	Reset input (Active Low)
208	YUV7	Input	TV Video Input Port: Data 7

2 ADE3XXX Functional Description

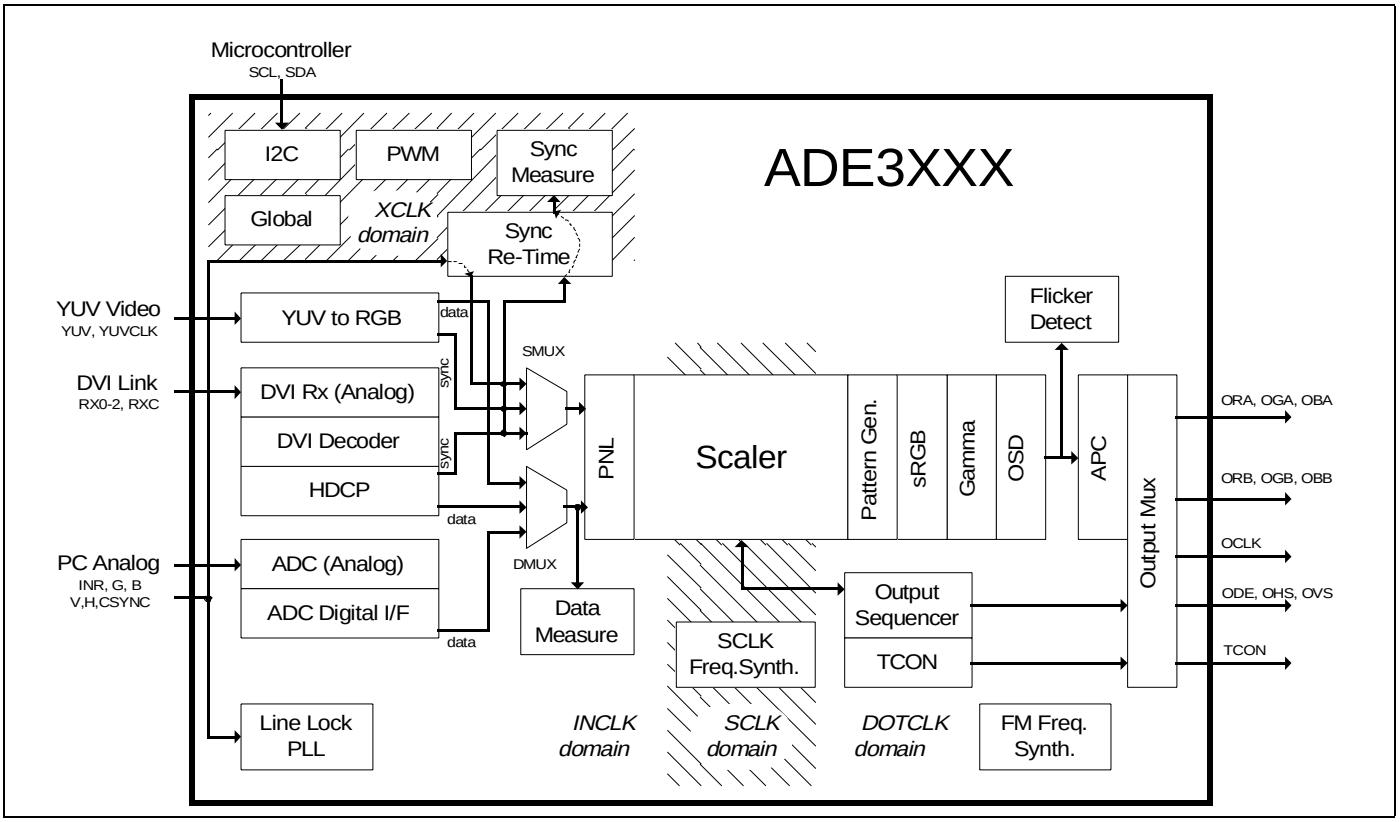
2.1 Global Control Block

The global control block is responsible for:

- Selecting Clock Sources
- Power Control
- I²C Control
- SCLK Frequency Synthesizer Control
- Block-by-Block Synchronous Reset Generation

The global control block runs on the XCLK clock domain which is required to be active for programming. The clock domains of all other blocks are set in the Global Control Block. For I²C access, the requested block must be driven with a valid clock above 10 MHz. Clock domains are shown in Figure 2.

Figure 2: Clock Domains



To program the SCLK frequency synthesizer to a desired frequency (fout, in MHz), the following equations apply:

Table 3: SCLK Frequency Ranges

Frequency Range	SDIV
$f_{OUT} < 8 \times f_{XCLK}$ AND $f_{OUT} \geq 4 \times f_{XCLK}$	0
$f_{OUT} < 4 \times f_{XCLK}$ AND $f_{OUT} \geq 2 \times f_{XCLK}$	1
$f_{OUT} < 2 \times f_{XCLK}$ AND $f_{OUT} \geq f_{XCLK}$	2

Table 3: SCLK Frequency Ranges (Continued)

Frequency Range	SDIV
$f_{OUT} < f_{XCLK}$ AND $f_{OUT} \geq f_{XCLK}/2$	3
$f_{OUT} < f_{XCLK}/2$ AND $f_{OUT} \geq f_{XCLK}/4$	4
$f_{OUT} < f_{XCLK}/4$ AND $f_{OUT} \geq f_{XCLK}/8$	5
$f_{OUT} < f_{XCLK}/8$ AND $f_{OUT} \geq f_{XCLK}/16$	6
$f_{OUT} < f_{XCLK}/16$ AND $f_{OUT} \geq f_{XCLK}/32$	7

$$MD = INT(f_{XCLK} \times (2^{(6 + NDIV - SDIV)}) / f_{OUT})$$

$$PE = INT((2^{15}) \times (MD + 1 - f_{XCLK} \times (2^{(6 + NDIV - SDIV)}) / f_{OUT}))$$

where f_{XCLK} is the external crystal frequency in MHz (typically 27). The maximum SCLK frequency generated by this block is $f_{XTAL} \times 2^{(2+NDIV)}$.

For lower power operation, set all clock sources to the “zero” setting and also set the analog power disables. In this condition, only the crystal clock domain (XCLK) runs and blocks in INCLK or DOTCLK domains are not accessible by I2C.

To detect a DVI plug event and wake from a low power state, program the DVI detection clock source select to the DVI detect clock and enable the analog power control for the DVI detect clock. All other clock sources are set to zero.

Table 4: Global Registers (Sheet 1 of 4)

Register Name	Addr.	Mode	Bits	Default	Description
GLBL_NULL_ADDR	0x0000	R/W	[7:0]	0x0	Chip Revision ID
GLBL_CLK_SRC_SEL_0	0x0001		[7]	0x0	Reserved
		R/W	[6:4]	0x5	DOTCLK source 0x0: YUVCLK pin 0x1: SCLK freq synth 0x2: FM freq synth (normal) 0x3: INCLK 0x4: CLKIN pin 0x5: crystal clock 0x6: 0 0x7: Reserved
		R/W	[3:0]	0xA	INCLK source 0x0: YUVCLK pin (YUV Input) 0x1: DVI_PLLCLK (DVI Input) 0x2: ADCclock red 0x3: ADCclock green 0x4: ADC clock blue 0x5: SCLK freq synth 0x6: DVI detect clock 0x7: LLK PLL (ADC Input) 0x8: CLKIN pin 0x9: FM freq synth 0xA: crystal clock 0xB: 0 0xC - 0xF: Reserved

Table 4: Global Registers (Sheet 2 of 4)

Register Name	Addr.	Mode	Bits	Default	Description
GLBL_CLK_SRC_SEL_2	0x0002		[7]	0x0	Reserved
		R/W	[6:4]	0x4	LLK CTRL CLK source 0x0: YUVCLK pin 0x1: SCLK freq synth 0x2: LLKPLL control clock (normal) 0x3: CLKIN pin 0x4: crystal clock 0x5: 0 0x6 - 0x7: Reserved
			[3]		Reserved
		R/W	[2:0]	0x4	LLK ZERO CLK source 0x0: YUVCLK pin 0x1: SCLK freq synth 0x2: LLKPLL zero clock (normal) 0x3: CLKIN pin 0x4: crystal clock 0x5: 0 0x6 - 0x7: Reserved
GLBL_CLK_INV	0x0003		[7]	0x0	Reserved
		R/W	[6]	0x0	Invert YUV clock
		R/W	[5]	0x0	Invert DVI detect clock
		R/W	[4]	0x0	Invert ADC clock
		R/W	[3]	0x0	Invert LLPLL zero clock
		R/W	[2]	0x0	Invert LLPLL ctrl clock
		R/W	[1]	0x0	Invert DOT clock
		R/W	[0]	0x0	Invert input clock
GLBL_ANA_PWR	0x0005		[7:5]	0x0	Reserved
		R/W	[4]	0x1	Blue ADC power down
		R/W	[3]	0x1	Green ADC power down
		R/W	[2]	0x1	Red ADC power down
		R/W	[1]	0x1	DVI detect clock power down
		R/W	[0]	0x1	DVI PLL power down
GLBL_XK_SRST	0x0006		[7:3]	0x0	Reserved
		R/W	[2]	0x0	SMEAS block reset, synchronous to XCLK
		R/W	[1]	0x0	SRT block reset, synchronous to XCLK
		R/W	[0]	0x0	Frame sync block reset, synchronous to XCLK
GLBL_I2C_CTRL	0x0007		[7:3]	0x0	Reserved
		R/W	[2]	0x0	Disable I2C auto increment
		R/W	[1]	0x0	SDA PMOS enable
		R/W	[0]	0x0	Bypass I2C filter
GLBL_XTAL_CTRL	0x0008		[7:1]	0x0	Reserved
		R/W	[0]	0x1	Crystal Oscillator Enable

Table 4: Global Registers (Sheet 3 of 4)

Register Name	Addr.	Mode	Bits	Default	Description
GLBL_SCLK_SYNTH_CTRL	0x0009		[7:5]	0x0	Reserved
		R/W	[4:3]	0x0	XTAL frequency multiplier NDIV 0x0: f_{XCLK} = 54MHz 0x1: f_{XCLK} = 27MHz (normal) 0x2: f_{XCLK} = 13.5MHz 0x3: Reserved
		R/W	[2]	0x0	SCLK frequency synthesizer EXT_PLL (normal operation = 0)
		R/W	[1]	0x0	SCLK frequency synthesizer PLL_SEL (normal operation = 1)
		R/W	[0]	0x1	SCLK freq synth control disable (normal operation = 0)
GLBL_SCLK_MD_SD	0x000A	R/W	[7:3]	0x0	SCLK frequency synthesizer MD, range is [16,31]
		R/W	[2:0]	0x0	SCLK frequency synthesizer SDIV, range is [0,7]
GLBL_SCLK_PE_L	0x000B	R/W	[7:0]	0x0	SCLK frequency synthesizer PE, range is [0, 32767]
GLBL_SCLK_PE_H	0x000C	R/W	[7:0]		
GLBL_TST_CTRL	0x000D		[7:1]	0x0	Reserved
		R/W	[0]	0x0	Functional Test Mode Enable
GLBL_ADC_CLK_SRC_SEL			[7:3]		Reserved
		R/W	[2:0]	0x5	ADC Sample Clock Source 0x0: YUVCLK pin 0x1: LLK_PLL (normal) 0x2: SCLK freq synth 0x3: CLKIN pin 0x4: FM freq synth 0x5: Crystal Clock 0x6: 0 0x7: Reserved
GLBL_SCLK_CTRL	0x0010		[7:5]	0x0	Reserved
		R/W	[4]	0x0	Invert SCLK
			[3]		Reserved
		R/W	[2:0]	0x0	SCLK source select 0x0: YUVCLK pin 0x1: SCLK freq synth 0x2: FM freq synth (normal) 0x3: inclk source 0x4: CLKIN pin 0x5: crystal clock 0x6: 0 0x7: Reserved
GLBL_TCON_BPAD_EN	0x0011	R/W	[7:0]	0x0	For each bit n (0 to 7), 0: TCON[n] pin is TCON output 1: TCON[n] pin is input into TVI block

Table 4: Global Registers (Sheet 4 of 4)

Register Name	Addr.	Mode	Bits	Default	Description
GLBL_CLK_SRC_SEL_3	0x0012		[7]		Reserved
		R/W	[6:4]	0x4	YUV clock source 0x0: YUVCLK pin 0x1: SCLK freq synth 0x2: YUVCLK pin (normal) 0x3: CLKIN pin 0x4: crystal clock 0x5: 0 0x6 - 0x7: Reserved
			[3]		Reserved
		R/W	[2:0]	0x4	DVI detection clock source 0x0: YUVCLK pin 0x1: SCLK freq synth 0x2: DVI detect clock (normal) 0x3: CLKIN pin 0x4: crystal clock 0x5: 0 0x6 - 0x7: Reserved
GLBL_IK_SRST	0x0020	R/W	[7]	0x0	HDCP block reset synchronous to INCLK
		R/W	[6]	0x0	DFT block reset synchronous to INCLK
		R/W	[5]	0x0	ADC block reset synchronous to INCLK
		R/W	[4]	0x0	SCALER block reset synchronous to INCLK
		R/W	[3]	0x0	YUV block reset synchronous to INCLK
		R/W	[2]	0x0	DVI block reset synchronous to INCLK
		R/W	[1]	0x0	DMEAS block reset synchronous to INCLK
		R/W	[0]	0x0	SMUX block reset synchronous to INCLK
GLBL_DK_SRST	0x0040		[7]	0x0	Reserved
		R/W	[6]	0x0	PGEN block reset synchronous to DOTCLK
		R/W	[5]	0x0	OMUX block reset synchronous to DOTCLK
		R/W	[4]	0x0	APC block reset synchronous to DOTCLK
		R/W	[3]	0x0	OSD block reset synchronous to DOTCLK
		R/W	[2]	0x0	GAMMA block reset synchronous to DOTCLK
		R/W	[1]	0x0	OSQ block reset synchronous to DOTCLK
		R/W	[0]	0x0	SCALE block reset synchronous to DOTCLK

2.2 FM Frequency Synthesizer

The FM frequency synthesizer creates a clock equivalent to up to eight times the crystal input clock, using a digital frequency synthesizer. The modulation period and amplitude are directly controlled by I2C registers. The I2C interface runs in the LLK_CTRL clock domain, which must be active for access.

The output frequency (f_{OUT}) is related to the 32-bit PHASE_RATE and crystal frequency (f_{XCLK}) as follows:

$$f_{OUT} = f_{XCLK} \times 2^{27+NDIV} / PHASE_RATE$$

where f_{OUT} and f_{XCLK} are in MHz.

The maximum output frequency of the fm frequency synthesizer is $f_{XTAL} \times 2^{(2+NDIV)}$.

Note that native duty cycle of the fm frequency synthesizer is not 50/50. We recommend to either enable the divide-by-two in the fm synthesizer block for frequencies up to $f_{XCLK} \times 2^{(1+NDIV)}$ (typically 108 MHz) or set the output mux to a double wide output mode for pixel clocks above $f_{XCLK} \times 2^{(1+NDIV)}$. This will ensure a 50% duty clock on the output.

Table 5: FM Frequency Synthesizer Registers

Register Name	Addr	Mode	Bits	Default	Description
FM_FS_CTRL	0x0830		[7:4]		Reserved
		R/W	[3]	0x0	Clear the FM synthesizer
		R/W	[2]	0x0	Clear the FS accumulator
		R/W	[1]	0x0	Activate the frequency modulation
		R/W	[0]	0x0	Divide the output by 2
FM_FS_PR_0	0x0831	R/W	[7:0]	0x8000000	Phase Rate
FM_FS_PR_1	0x0832	R/W	[7:0]		
FM_FS_PR_2	0x0833	R/W	[7:0]		
FM_FS_PR_3	0x0834	R/W	[7:0]		
FM_FS_AMPLITUDE	0x0835	R/W	[7:0]	0x0	LSB = 72 ps
FM_FS_PERIODX64	0x0836	R/W	[7:0]	0x80	LSB = 1.185 µs

2.3 ADC Block

The analog port consists of three 9-bit RGB ADCs with preamp, gain/offset adjustment and digital filtering. The I2C interface for the ADC block is in the INCLK clock domain which must be active for programming.

Input voltage, gain and offset register settings are approximately related to the output code. In this equation, the output code (OUTPUT_CODE_8B) is equal to:

$$457 \times \text{offset} / 2^8 + 181 \times \text{gain} \times \text{input_mV} / 2^{16} - 125 \times \text{gain} \times \text{offset} / 2^{16} - 219$$

Table 6: ADC Registers

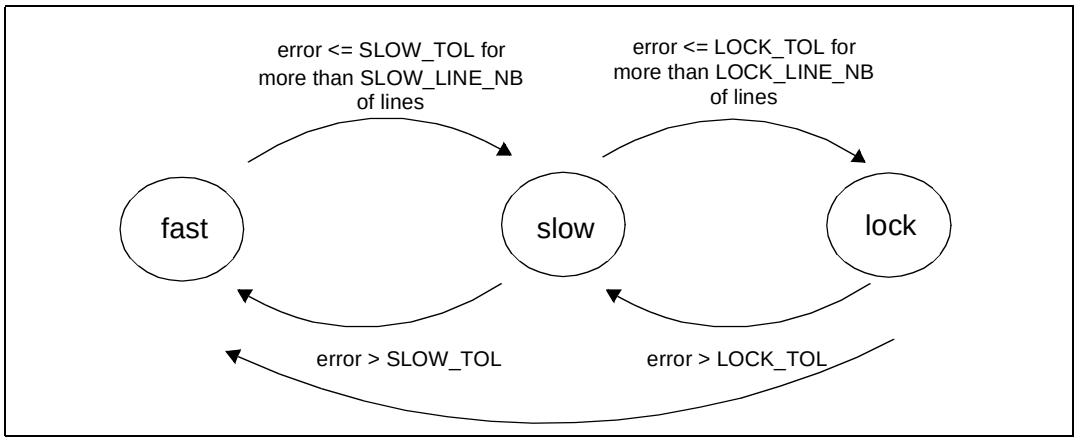
Register	Addr.	Mode	Bits	Default	Description
ADC_DITHER	0x0324		[7]		Reserved
		R/W	[6]	0x0	Dither Horizontally
		R/W	[5]	0x0	Dither Vertically
		R/W	[4]	0x0	Dither Temporally
		R/W	[3]	0x0	Force Dither High
		R/W	[2]	0x0	Enable Dither
			[1:0]		Reserved
ADC_OFFSET_R	0x0326	R/W	[7:0]	0x0	Offset Control, Red Channel
ADC_OFFSET_G	0x0328	R/W	[7:0]	0x0	Offset Control, Green Channel
ADC_OFFSET_B	0x0329	R/W	[7:0]	0x0	Offset Control, Blue Channel
ADC_GAIN_R	0x032A	R/W	[7:0]	0x0	Gain Control, Red Channel
ADC_GAIN_G	0x032B	R/W	[7:0]	0x0	Gain Control, Green Channel
ADC_GAIN_B	0x032C	R/W	[7:0]	0x0	Gain Control, Blue Channel

2.4 Line Lock PLL Block

The line lock PLL recovers a sample clock from an incoming hsync source. The response characteristics of the line lock PLL are adjustable for optimimum response time and jitter filtering. The phase of the sample clock is digitally adjustable by steps of 289 ps (with a 27-MHz crystal). The I2C interface of the line lock PLL is in the LLK_CTRL clock domain which must be active for programming.

The PLL loop filter has three ranges with independent filter parameters. When the phase detector error remains below a programmable threshold for a programmable number of input lines, the loop filter coefficients change. Any phase detector error above the programmed threshold reverts the filter to the appropriate level in one line. The operation is represented in Figure 3.

Figure 3: Line Lock PLL State Diagram



The digital loop filter is controlled by three parameters: MFACTOR, A and B. M_FACTOR is the desired number of clocks per input line. The A and B parameters control the response of the 2nd order digital filter. A and B are composed of a linear and exponential component designated by the L and E suffix, respectively. These numbers are related to the classic 2nd order damping and natural frequency as follows:

$$\text{Damping} = AL \times 2^{(AE-12)} \times \text{SQRT}(5 \times M_FACTOR / (BL \times 2^{BE}))$$

$$\text{Natural Frequency} = \text{SQRT}(M_FACTOR \times 5 \times BL \times 2^{(BE-34)})$$

Table 7: Line Lock PLL Registers (Sheet 1 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_CLEAR	0x0800		[7:6]		Reserved
		R/W	[5]	0x0	Master Reset
		R/W	[4]	0x0	Reset the PLL synthetic sync
		R/W	[3]	0x0	Reset PLL offset
		R/W	[2]	0x0	Reset PLL accumulator
		R/W	[1]	0x0	Reset the low pass filter
		R/W	[0]	0x0	Reset the PLL phase error

Table 7: Line Lock PLL Registers (Sheet 2 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_CTRL	0x0801	R/W	[7:6]		Reserved
		R/W	[5]	0x0	0: normal 1: diagnostic mode -- PLL uses only fine error
		R/W	[4]	0x0	0: normal 1: diagnostic -- coarse error is multiplied by 2
		R/W	[3]	0x0	input hsync edge selection 0: rising edge 1: falling edge
		R/W	[2]	0x0	sync on green input selection 0: composite sync (HSYNC pin) 1: sync on green (CSYNC pin)
		R/W	[1]	0x0	0: normal 1: divide PLL clock by 2
		R/W	[0]	0x0	0: normal 1: Free-running mode
LLK_PLL_MFACTOR_L	0x0802	R/W	[7:0]	0x0280	number of clocks in a line
LLK_PLL_MFACTOR_H	0x0803	R/W	[7:0]		
LLK_PLL_HPERIOD_L	0x0804	R/W	[7:0]	0x0040	pulse width of synthetic hsync
LLK_PLL_HPERIOD_H	0x0805	R/W	[7:0]		
LLK_PLL_PHASE_RATE_INIT_0	0x0806	R/W	[7:0]	0x0	Initial Phase Rate
LLK_PLL_PHASE_RATE_INIT_1	0x0807	R/W	[7:0]		$f_{OUT} = f_{XTAL} \times 2^{27+NDIV} / PHASE_RATE$
LLK_PLL_PHASE_RATE_INIT_2	0x0808	R/W	[7:0]		
LLK_PLL_PHASE_RATE_INIT_3	0x0809	R/W	[7:0]		
LLK_PLL_PHASE_RATE_INIT_WR	0x080A	R/W	[7:1]		Reserved
			[0]		When written to 1, the PLL phase rate is initialized with the initial phase rate register. Self clearing.
LLK_PLL_TC_AEF	0x080B		[7:4]		Reserved
		R/W	[3:0]	0xA	Fast Time Constant A Exponent
LLK_PLL_TC_BEF	0x080C		[7:4]		Reserved
		R/W	[3:0]	0xA	Fast Time Constant B Exponent
LLK_PLL_TC_ALF	0x080D		[7:6]		Reserved
		R/W	[5:0]	0x20	Fast Time Constant A Linear
LLK_PLL_TC_BLF	0x080E		[7:6]		Reserved
		R/W	[5:0]	0x20	Fast Time Constant B Linear
LLK_PLL_TC_AES	0x080F		[7:4]		Reserved
		R/W	[3:0]	0x6	Slow Time Constant A Exponent
LLK_PLL_TC_BES	0x0810		[7:4]		Reserved
		R/W	[3:0]	0x6	Slow Time Constant B Exponent
LLK_PLL_TC_ALS	0x0811		[7:6]		Reserved
		R/W	[5:0]	0x20	Slow Time Constant A Linear

Table 7: Line Lock PLL Registers (Sheet 3 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_TC_BLS	0x0812		[7:6]		Reserved
		R/W	[5:0]	0x20	Slow Time Constant B Linear
LLK_PLL_TC_AEK	0x0813		[7:4]		Reserved
		R/W	[3:0]	0x6	Lock Time Constant A Exponent
LLK_PLL_TC_BEK	0x0814		[7:4]		Reserved
		R/W	[3:0]	0x6	Lock Time Constant B Exponent
LLK_PLL_TC_ALK	0x0815		[7:6]		Reserved
		R/W	[5:0]	0x20	Lock Time Constant A Linear
LLK_PLL_TC_BLK	0x0816		[7:6]		Reserved
		R/W	[5:0]	0x20	Lock Time Constant B Linear
LLK_PLL_TC_SLOW_TOL	0x0817	R/W	[7:0]	0x80	More than SLOW_LINE_NB lines with a phase error less than the SLOW_TOL will set the slow status bit, and the PLL will work with the slow time constant. One or more lines with a phase error more than SLOW_TOL will reset the slow status bit, and the PLL will work with the fast time constant. LSB of SLOW_TOL is approx. 200ps.
LLK_PLL_TC_SLOW_LINE_NB	0x0818	R/W	[7:0]	0x10	
LLK_PLL_LOCK_TOL	0x0819	R/W	[7:0]	0x20	More than LOCK_LINE_NB lines with a phase error less than the LOCK_TOL will set the lock status bit, and the PLL will work with the lock time constant. One or more lines with a phase error more than LOCK_TOL will reset the lock status bit, and the PLL will work with the slow time constant. LSB of LOCK_TOL is approx. 200 ps.
LLK_PLL_LOCK_LINE_NB	0x081A	R/W	[7:0]	0x30	
LLK_PLL_PH_OFFSET	0x081B	R/W	[7:0]	0x0	Phase Adjustment. The maximum phase offset value is equal to PHASE_RATE[31:21] or 0x40, whichever is higher.
LLK_PLL_PH_OFFSET_EN	0x081C	R/W	[7]	0x0	Phase Enable
			[6:0]		Reserved
LLK_PLL_PULSE_HIGH_EXT	0x081D	R/W	[7]	0x0	0: no pulse extend 1: extend pulse (normal)
			[6:3]		Reserved
		R/W	[2:0]	0x0	Pulse Extend Amount 0x0: Minimum 0x7: Maximum (Normal)
LLK_PLL_STAT_LINES_L	0x081E	R/W	[7:0]	0x10	Number of lines to statistically analyze.
LLK_PLL_STAT_LINES_H	0x081F	R/W	[7:0]		
LLK_PLL_STAT_ERROR_INC_LOW	0x0820		[7:0]		Reserved

Table 7: Line Lock PLL Registers (Sheet 4 of 4)

Register Name	Addr	Mode	Bits	Default	Description
LLK_PLL_UPDATE	0x0840	R	[7]		In Free-running mode, toggles when status is updated. In one-shot mode, this bit is set when status is ready.
			[6:2]		Reserved
		R/W	[1]	0x0	0: Free-running mode 1: one-shot mode
		R/W	[0]	0x0	update enable
LLK_PLL_STATUS	0x0841		[7:4]		Reserved
		R	[3]		LLK overflow
		R	[2]		coarse error = 0
		R	[1]		in slow mode
		R	[0]		in lock mode
LLK_PLL_PH_ERROR_L	0x0842	R	[7:0]		phase error
LLK_PLL_PH_ERROR_H	0x0843	R	[7:0]		LSB = approx. 200ps
LLK_PLL_PHASE_RATE_0	0x0844	R	[7:0]		LLK phase rate
LLK_PLL_PHASE_RATE_1	0x0845	R	[7:0]		$f_{OUT} = f_{XTAL} \times 2^{27+NDIV} / PHASE_RATE$
LLK_PLL_PHASE_RATE_2	0x0846	R	[7:0]		
LLK_PLL_PHASE_RATE_3	0x0847	R	[7:0]		
LLK_PLL_PHASE_RATE_I_0	0x0848	R	[7:0]		integral phase rate
LLK_PLL_PHASE_RATE_I_1	0x0849	R	[7:0]		
LLK_PLL_PHASE_RATE_I_2	0x084A	R	[7:0]		
LLK_PLL_PHASE_RATE_I_3	0x084B	R	[7:0]		
LLK_PLL_STAT_ERROR_MEAN	0x084C	R	[7:0]		Average Phase Error over STAT_LINES phase error LSB is approx. 200ps
LLK_PLL_STAT_ERROR_PP_L	0x084D	R	[7:0]		Peak Phase Error over STAT_LINES
LLK_PLL_STAT_ERROR_PP_H	0x084E	R	[7:0]		phase error LSB is approx. 200ps
LLK_PLL_STAT_ERROR_ABS_L	0x084F	R	[7:0]		sum of absolute phase errors over STAT_LINES phase error LSB is approx. 200ps
LLK_PLL_STAT_ERROR_ABS_H	0x0850	R	[7:0]		
LLK_PLL_STAT_ERROR_GTX	0x0851		[7:0]		Reserved

2.5 Digital Video Input (DVI)

The DVI receiver has the following features:

- compatible with all DVI complaint transmitters up to 140 MHz pixel clock
- on chip termination adjustable by I2C and/or one (~10X) external reference resistor
- HDCP and standby / power down supported
- decoder digitally corrects for skew errors of at least ±1 pixel in reference to any other channel
- bitstream can be decoded and measured without the presence of horizontal and vertical sync pulses

Recommended values for best receiver quality are given in the following table:

Table 8: Recommended DVI Values

Clock Speed	DVI_PLL_0	DVI_PLL_1
0 to 30 MHz	0x02	0x00
31 to 60 MHz	0x03	0x00
61 to 100 MHz	0x04	0x00
101 to 140 MHz	0x05	0x00

Table 9: DVI Registers (Sheet 1 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DVI_ACCUM_CONST	0x0401		[7:4]	0x5	Reserved
		R/W	[3:0]	0x5	digital filter response speed 5: fastest 14: slowest
DVI_EXT_SHIFT_CNT	0x0402	R/W	[7:6]		Reserved
		R/W	[5:0]	0x08	alignment position of chan0, used for debugging only
DVI_EXT_SHIFT_CNT_ENAB	0x0403		[7:6]		Reserved
		R/W	[6]	0x0	0: normal 1: freeze alignment readout
		R/W	[5:0]	0x0	initial value for the alignment position for all channels
DVI_INVALID_L	0x0404				invalid code count for left position.
		R	[7:3]	0x0	exponent
		R	[2:0]	0x0	mantissa count = (mant+8) * $2^{(exp-4)}$, if exp>3, else count = mant
DVI_INVALID_C	0x0405				invalid code count for center position.
		R	[7:3]	0x0	exponent
		R	[2:0]	0x0	mantissa count = (mant+8) * $2^{(exp-4)}$, if exp>3, else count = mant
DVI_INVALID_R	0x0406				invalid code count for right position.
		R	[7:3]	0x0	exponent
		R	[2:0]	0x0	mantissa count = (mant+8) * $2^{(exp-4)}$, if exp>3, else count = mant

Table 9: DVI Registers (Sheet 2 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DVI_INVALID_SEL_EN	0x0407	R/W	[7:3]		Reserved
		R/W	[2:1]	0x0	channel to count invalid code events 0: blue channel 1: green channel 2: red channel
		R/W	[0]	0x0	invalid code accumulation period 0: 16k lines 1: 4 lines
DVI_ERROR_SKEW_EN	0x0408	R/W	[7:3]	0x0	Reserved
		R/W	[2]	0x0	0: tracking in data & blanking 1: tracking only in blanking
		R/W	[1]	0x0	enable channel skew protection
		R/W	[0]	0x0	enable error concealment
DVI_LCR0_1	0x0409	R/W	[7:4]	0x7	4 bit incr value (2's complement)
		R/W	[3:0]	0x4	4 bit incr value (2's complement)
DVI_LCR2_3	0x040A	R/W	[7:4]	0x0	4 bit incr value (2's complement)
		R/W	[3:0]	0x0	4 bit incr value (2's complement)
DVI_LCR4_5	0x040B	R/W	[7:0]	0x0	4 bit incr value (2's complement)
		R/W	[3:0]	0x9	4 bit incr value (2's complement)
DVI_LCR6_7	0x040C	R/W	[7:0]	0xF	4 bit incr value (2's complement)
		R/W	[3:0]	0x0	4 bit incr value (2's complement)
DVI_LCR_RV_EN	0x040D	R/W	[7]	0x1	Enable Restoring Force for LCR7.
		R/W	[6]	0x0	Enable Restoring Force for LCR6.
		R/W	[5]	0x0	Enable Restoring Force for LCR5.
		R/W	[4]	0x0	Enable Restoring Force for LCR4.
		R/W	[3]	0x0	Enable Restoring Force for LCR3.
		R/W	[2]	0x0	Enable Restoring Force for LCR2.
		R/W	[1]	0x0	Enable Restoring Force for LCR1.
		R/W	[0]	0x0	Enable Restoring Force for LCR0.
DVI_TEST_SEL	0x040E		[7:0]	0x0	Reserved
DVI_PLL_0	0x0480	R/W	[7]	0x0	Termination control 0: 50ohm Impedance (normal) 1: High impedance

Table 9: DVI Registers (Sheet 3 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DVI_PLL_0	0x0480	R/W	[7]		Reserved, must be set to 0
		R/W	[6:5]	0x0	Amplifier Current 0x0: 25uA (default) 0x1: 75uA 0x2: 125uA 0x3: 175uA (fastest)
		R/W	[4:3]	0x0	VTOL Range Overlap 0x0: 34.1uA (default) 0x1: 50.9uA 0x2: 26.0uA 0x3: 42.9uA
		R/W	[2:0]	0x0	Change Pump Current Select 0x0: 25uA (default) 0x1: 50uA 0x2: 75uA 0x3: 100uA 0x4: 125uA 0x5: 150uA 0x6: 175uA 0x7: 200uA (fastest)
DVI_PLL_1	0x0481	R/W	[7]	0x0	Bias Select 0: internal (default) 1: external
		R/W	[6:5]	0x0	Range Checking Interval 0x0: CLK/512 (default) 0x1: CLK/1024 0x2: CLK/2048 0x3: CLK/256
		R/W	[4:1]	0x0	Manual Range Select 0x0: Reserved 0x1: force Range 1 (lowest) 0x2 - 0x3: force Range 2 0x4 - 0x7: force Range 3 0x8 - 0xF: force Range 4 (highest)
			[0]	0x0	PLL Range Control 0: Auto (Default) 1: Manual
DVI_PLL_2	0x0482	R/W	[7:6]	0x0	Strobe 3 Adjust 0: Normal 1: Slower 2: Faster 3: Reserved
		R/W	[5:4]	0x0	Strobe 2 Adjust
		R/W	[3:2]	0x0	Strobe 1 Adjust
		R/W	[1:0]	0x0	Global Strobe Adjust 0: Normal 1: Slower 2: Faster 3: Reserved

Table 9: DVI Registers (Sheet 4 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DVI_PLL_3	0x0483	R/W	[7:6]	0x0	Strobe 7 Adjust
		R/W	[5:4]	0x0	Strobe 6 Adjust
		R/W	[3:2]	0x0	Strobe 5 Adjust
		R/W	[1:0]	0x0	Strobe 4 Adjust
DVI_PLL_4	0x0484	R/W	[7:6]	0x0	Strobe 11 Adjust
		R/W	[5:4]	0x0	Strobe 10 Adjust
		R/W	[3:2]	0x0	Strobe 9 Adjust
		R/W	[1:0]	0x0	Strobe 8 Adjust
DVI_PLL_5	0x0485	R/W	[7:6]	0x0	Strobe 15 Adjust
		R/W	[5:4]	0x0	Strobe 14 Adjust
		R/W	[3:2]	0x0	Strobe 13 Adjust
		R/W	[1:0]	0x0	Strobe 12 Adjust
DVI_PLL_6	0x0486	R/W	[7:6]	0x0	Strobe 19 Adjust
		R/W	[5:4]	0x0	Strobe 18 Adjust
		R/W	[3:2]	0x0	Strobe 17 Adjust
		R/W	[1:0]	0x0	Strobe 16 Adjust
DVI_PLL_7	0x0487	R/W	[7:6]	0x0	Strobe 23 Adjust
		R/W	[5:4]	0x0	Strobe 22 Adjust
		R/W	[3:2]	0x0	Strobe 21 Adjust
		R/W	[1:0]	0x0	Strobe 20 Adjust
DVI_PLL_8	0x0488	R/W	[7:6]	0x0	Strobe 27 Adjust
		R/W	[5:4]	0x0	Strobe 26 Adjust
		R/W	[3:2]	0x0	Strobe 25 Adjust
		R/W	[1:0]	0x0	Strobe 24 Adjust
DVI_PLL_2	0x0482	R/W	[7:6] [5:4] [3:2] [1:0]	0x0	Strobe [0:3] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved
DVI_PLL_3	0x0483	R/W	[7:6] [5:4] [3:2] [1:0]	0x0	Strobe [4:7] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved
DVI_PLL_4	0x0484	R/W	[7:6] [5:4] [3:2] [1:0]	0x0	Strobe [8:11] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved
DVI_PLL_5	0x0485	R/W	[7:6] [5:4] [3:2] [1:0]	0x0	Strobe [12:15] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved

Table 9: DVI Registers (Sheet 5 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DVI_PLL_6	0x0486	R/W	[7:6] [5:4] [3:2] [1:0]	0x0	Strobe [16:19] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved
DVI_PLL_7	0x0487	R/W	[7:6] [5:4] [3:2] [1:0]	0x0	Strobe [20:23] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved
DVI_PLL_8	0x0488	R/W	[7:6] [5:4] [3:2] [1:0]	0x0	Strobe [24:27] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved
DVI_PLL_9	0x0489		[7:6]		Reserved
		R/W	[5]	0x0	Test Enable (normal operation = 0)
		R/W	[4]	0x0	Strobe Delay Adjustment Step 0: 45pS (default) 1: 72pS
		R/W	[3:2]	0x0	Strobe 29 Adjust 0: Normal 1: Slower 2: Faster 3: Reserved
		R/W	[1:0]	0x0	Strobe 28 Adjust
		R/W	[3:2] [1:0]	0x0	Strobe [28:29] Delay Adjustment 0x0: Normal 0x1: Slow 0x2: Fast 0x3: Reserved
DVI_PLL_10	0x048A		[7]		Reserved
		R	[6:4]		Test Output DVIPLL[79:77]
		R	[3:0]		PLL Range Status
		R	[3:0]	0x0	PLL Range Status

2.6 HDCP Block

The HDCP block implements the datapath decryption block of the HDCP content protection scheme of DVI. Please refer to the HDCP Specification 1.0 for details. The state machines of the HDCP specification are split between the external microcontroller and this block. Only the high speed and data intensive cryptographic functions are implemented in this block to maintain maximum system level flexibility.

Table 10: HDCP Registers

Register Name	Addr	Mode	Bits	Default	Description
HDCP_STATUS	0x0500		[7:3]	0x0	Reserved
		R	[2:0]	0x0	Decrypt State Machine 0x0: Idle 0x1: Frame Key Recalc 0x2: Data 0x3: Unknown Blank 0x4: Horizontal Blank 0x5: Vertical Blank 0x6-0x7: Reserved
HDCP_CTRL	0x0501	R/W	[7:6]	0x0	Vsync Selection 0x0: IN_VSYNC 0x1: IN_VENAB Falling Edge 0x2: IN_VENAB Rising Edge 0x3: IN_VSYNC Falling Edge
		R/W	[5:4]	0x0	Hsync Selection 0x0: IN_HSYNC 0x1: IN_ENAB Falling Edge 0x2: IN_ENAB Rising Edge 0x3: IN_HSYNC Falling Edge
		R/W	[2]	0x0	Bypass HDCP block
		R/W	[1]	0x0	Authentication OK from MCU
		R/W	[0]	0x0	0: State Machine Standby 1: Trigger an Authentication Cycle
HDCP_AN0	0x0502	R/W	[7:0]	0x0	An
HDCP_AN1	0x0503	R/W	[7:0]		
HDCP_AN2	0x0504	R/W	[7:0]		
HDCP_AN3	0x0505	R/W	[7:0]		
HDCP_AN4	0x0506	R/W	[7:0]		
HDCP_AN5	0x0507	R/W	[7:0]		
HDCP_AN6	0x0508	R/W	[7:0]		
HDCP_AN7	0x0509	R/W	[7:0]		
HDCP_KM0	0x050A	R/W	[7:0]	0x0	Kn
HDCP_KM1	0x050B	R/W	[7:0]		
HDCP_KM2	0x050C	R/W	[7:0]		
HDCP_KM3	0x050D	R/W	[7:0]		
HDCP_KM4	0x050E	R/W	[7:0]		
HDCP_KM5	0x050F	R/W	[7:0]		
HDCP_KM6	0x0510	R/W	[7:0]		
HDCP_R_L	0x0511	R/W	[7:0]	0x0	R
HDCP_R_H	0x0512	R/W	[7:0]		

2.7 YUV Block

The TV video input module is used to interface external TV video decoder chip. It handles VESA Video Interface Port(VIP) 8-bit/16-bit YC_BC_R, VMI/ ITU-R Recommendation 656 (CCIR656) YC_BC_R and double clock edge input RGB data formats. It extracts embedded sync timing and converts data into RGB color space. All the functions in this module are controlled by the system microcontroller through I2C registers.

The following table describes the different pin configurations for YUV/RGB digital input.

Mode	YUV[7:0]	TCON[3:0]	TCON[7:4]
CCIR656	DATA[7:0]	X	X
VMI	DATA[7:0]	X	{HREF, VREF, VACTIVE, X}
VIP 8b	DATA[7:0]	X	X
VIP 16b	DATA[7:0]	DATA[11:8]	DATA[15:12]
RGB Posedge	BLUE[7:0]	GREEN[3:0]	{HSYNC,VSYNC,DE,X}
RGB Negedge	{RED[3:0],GREEN[7:4]}	RED[7:4]	{HSYNC,VSYNC,DE,X}

X = don’t care

Table 11: YUV Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
YUV_CTRL	0x0700		[7:6]		Reserved
		R/W	[5]	0x0	0: Rising edge of clock 1: Falling edge of clock
		R/W	[4]	0x0	Input Source of Color Space Converter 0: YUV pins 1: ADC
		R/W	[3]	0x0	Color Space Converter Enable
		R/W	[2]	0x0	Sync Decoder Enable
		R/W	[1]	0x0	Sample Input Data Rate 0:1x 1: 2x
		R/W	[0]	0x0	Status Reset
YUV_STATUS	0x0701		[7]		Reserved
		R/W	[6]	0x0	SAV detected
		R/W	[5]	0x0	EAV detected
		R/W	[4]	0x0	ANC detected
		R/W	[3]	0x0	TASK detected
		R/W	[2]	0x0	FIELDID detected
		R/W	[1]	0x0	HSYNC detected
		R/W	[0]	0x0	VSYNC detected Writing to this register will clear all bits.

Table 11: YUV Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
YUV_INT	0x0702		[7:6]		Reserved
		R/W	[5]	0x0	0: VIP 8b mode 1: VIP 16b mode (skip 1 clock after every 6 valid data)
		R/W	[4:2]	0x0	YUV data input format 0x2: YUV 16-bit 0x4: YUV 8-bit 0x6: RGB all others: Reserved
		R/W	[1]	0x0	0: C-Y 1: Y-C
		R/W	[0]	0x0	0: Cr-Cb 1: Cb-Cr

2.8 Sync Retiming Block

The Sync Retiming (SRT) block retimes incoming synchronization signals (H Sync, V Sync, etc) into the XCLK and INCLK domains.

For the XCLK domain, SRT has the following functionality:

- Retimes all sync signals going to SMEAS into the XCLK domain.
- Extracts vertical sync from composite sync signals (ahsync and acsync pins)
- Divides clocks by 1024 for activity detection purposes.
- Generates a delay-filtered version of vertical sync from a mux-selectable vertical sync source.
- Generates a coast signal in the XCLK domain for the LLPLL.

Table 12: Sync Retiming Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SRTXK_CSYNC_INV	0x01E0		[7:3]	0x0	Reserved
		R/W	[2]	0x0	invert filtered vert sync signal
		R/W	[1]	0x0	invert composite sync signal
		R/W	[0]	0x0	invert SOG signal
SRTXK_SOG_THR_L	0x01E1	R/W	[7:0]	0x080	SOG vert sync extractor threshold [7:0]
SRTXK_SOG_THR_H	0x01E2	R/W	[7:4]		Reserved
			[3:0]		SOG vert sync extractor threshold [11:8]
SRTXK_CSYNC_THR_L	0x01E3	R/W	[7:0]	0x080	composite sync vertical sync extractor threshold [7:0]
SRTXK_CSYNC_THR_H	0x01E4	R/W	[7:4]		Reserved
			[3:0]		composite sync vertical sync extractor threshold [11:8]

Table 12: Sync Retiming Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SRTXK_VSYNC_SEL	0x01E5	R/W	[7:3]		Reserved
			[2:0]	0x0	filtered vert sync source select 0x0: avsync pin 0x1: vsync from composite ahsync pin 0x2: vsync from composite acsync pin 0x3: Reserved 0x4: DVI vsync 0x5: YUV vsync 0x6 - 0x7: Reserved
SRTXK_VSYNC_THR_L	0x01E6	R/W	[7:0]	0x080	filtered vert sync delay [7:0]
SRTXK_VSYNC_THR_H	0x01E7	R/W	[7:4]		Reserved
		R/W	[3:0]		filtered vert sync delay [11:8]
SRTXK_COAST_VS_SEL	0x01E8		[7:4]	0x0	Reserved
		R/W	[3]	0x0	coast signal trigger edge 0: posedge of selected vertical 1: negedge of selected vertical
		R/W	[2:0]	0x0	source select for coast vert sync trigger 0x0: avsync pin 0x1: vsync from ahsync pin 0x2: vsync from acsync pin 0x3: Reserved 0x4: DVI vsync 0x5: YUV vsync 0x6: srt vsync (filtered vsync) 0x7: Reserved
SRTXK_COAST_RISE_L	0x01E9	R/W	[7:0]	0x0	rising edge of coast, in XCLKs from vsync trigger
SRTXK_COAST_RISE_M	0x01EA	R/W	[7:0]	0x0	
SRTXK_COAST_RISE_H	0x01EB	R/W	[7:0]	0x0	
SRTXK_COAST_FALL_L	0x01EC	R/W	[7:0]	0x0	falling edge of coast, in XCLKs from vsync trigger
SRTXK_COAST_FALL_M	0x01ED	R/W	[7:0]	0x0	
SRTXK_COAST_FALL_H	0x01EE	R/W	[7:0]	0x0	
SRTIK_HS_CTRL	0x01F0		[7:3]	0x0	Reserved
		R/W	[2]	0x0	Resample clock edge to transfer hsync into the INCLK domain; depends on LLK phase offset value. 0: posedge INCLK 1: negedge INCLK
		R/W	[1:0]	0x0	horz sync source select for resampling into the INCLK domain 0x0: LLPLL lock sync (normal) 0x1: ahsync pin 0x2: acsync pin 0x3: Reserved
SRTIK_VS_SEL	0x01F1		[7:2]	0x0	Reserved
		R/W	[1:0]	0x0	vert sync source select for resampling 0x0: avsync pin 0x1: vsync from ahsync pin 0x2: vsync from acsync pin 0x3: srt vsync (filtered vsync)

2.9 Sync Measurement Block

The Input Sync Measurement Block (SMEAS) continuously detects activity from all video sources. The module can measure the characteristics of the sync signals on any input port. The sync measurement module reports the results of the measurements to the system microcontroller.

This portion of the sync measurement is fully synchronous on the crystal clock (XCLK). Another block, the Sync Retiming Block (SRT), handles the asynchronous signal transfer of the incoming sync signals.

Input Sync Functions:

- Activity detection
- Sync management
- Measurement

Table 13: Sync Measurement Registers (Sheet 1 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_ACT_CTRL	0x0100		[7:4]	0x0	Reserved
		R/W	[3]	0x0	Enable activity detection in Free-running mode.
		R/W	[2]	0x0	Freeze results in Free-running mode. No meaning in One-shot mode. 0: Do not freeze the results. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results. The polling bit will still toggle and the block continues to free run; however, results will not be updated.
		R/W	[1]	0x0	activity detection start. In one-shot mode it triggers the start of a measurement and is reset to zero when the measurement is complete.
		R/W	[0]	0x0	activity detection mode control 0: free run 1: one shot
SMEAS_ACT_H_SMPTM_L	0x0101	R/W	[7:0]	0x0	Sample time value for clock or hsync activity. In units of XCLK_period*256
SMEAS_ACT_H_SMPTM_H	0x0102	R/W	[7:0]	0x0	
SMEAS_ACT_V_SMPTM_L	0x0103	R/W	[7:0]	0x0	Sample time value for vsync activity in units of XCLK_period*256. Note: this number MUST be larger than hsync sample time.
SMEAS_ACT_V_SMPTM_H	0x0104	R/W	[7:0]	0x0	
SMEAS_ACT_H_MINEDGE	0x0105	R/W	[7:0]	0x0	Minimum edge count value for clk or hsync activity.
SMEAS_ACT_V_MINEDGE	0x0106	R/W	[7:0]	0x0	Minimum edge count value for vsync activity.
SMEAS_H_TMOT_L	0x0107	R/W	[7:0]	0x4000	timeout counter value for clk or horizontal measurement in XCLKs
SMEAS_H_TMOT_H	0x0108	R/W	[7:0]		
SMEAS_V_TMOT_L	0x0109	R/W	[7:0]	0x1600	timeout counter value for vertical measurement in units of XCLK/256
SMEAS_V_TMOT_H	0x010A	R/W	[7:0]		

Table 13: Sync Measurement Registers (Sheet 2 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_CLEAR	0x0110		[7:3]		Reserved
		R/W	[2]	0x0	clear sticky status bits
		R/W	[1]	0x0	clear all out-of-range event counters
		R/W	[0]	0x0	clear all result registers
SMEAS_H_CTRL	0x0111		[7]	0x0	Reserved
		R/W	[6]	0x0	Enable Hsync Filter All hsync pulses less than SMEAS_FILTER_HS_WIDTH will be ignored.
		R/W	[5]	0x0	Measure hsync in the absence of vsync
		R/W	[4]	0x0	Enable Horizontal Measurement in Free-running mode
		R/W	[3]	0x0	Horizontal Event Edge Select 0: positive edge 1: negative edge
		R/W	[2]	0x0	Freeze horizontal measurements results during Free-running mode. No meaning in One-shot mode. 0: Do not freeze measurement results. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results. The polling bit will still toggle and the block continues to free run; however, results will not be updated.
		R/W	[1]	0x0	Horizontal Measurement Start In one-shot mode, this bit triggers the start of a measurement. The bit is reset to zero when the measurement is complete.
		R/W	[0]	0x0	Horizontal Measurement Mode 0: Free-running 1: One-shot

Table 13: Sync Measurement Registers (Sheet 3 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_V_CTRL	0x0112		[7]	0x0	Reserved
		R/W	[6]	0x0	Enable Interlace Measurement
		R/W	[5]	0x0	Measure odd frame from YUV only. Applies only if the odd signal from YUV is present. The results in SMEAS_XCLKS_PER_H and SMEAS_H_PER_V are updated for odd frames if this bit is set.
		R/W	[4]	0x0	Enable Vertical Measurement in Free-running mode.
		R/W	[3]	0x0	Vertical Event Edge select 0: positive edge 1: negative edge
		R/W	[2]	0x0	Freeze Vertical Measurement results in Free-running mode. No meaning in One-shot mode. 0: Do not freeze the results. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results in Free-running mode. The polling bit will still toggle and the block continues to free run; however, results will not be updated.
		R/W	[1]	0x0	Vertical measurement start. In One-shot mode, this bit triggers the start of a measurement. The bit is reset to zero when the measurement is complete.
		R/W	[0]	0x0	Vertical measurement mode 0: Free-running 1: One-shot
SMEAS_H_SEL	0x0113	R/W	[7:4]		Reserved
			[3:0]	0x0	Select a horizontal sync, enable or clock for measurement. 0x0: Analog hsync 0x1: Hsync generated from LLPLL 0x2: SOG from csync pin 0x3: DVI hsync 0x4: YUV hsync 0x5: DVI data enable 0x6: YUV data enable 0x7: DVIclk div1k 0x8: YUVclk div1k 0x9: TCON hsync 0xA: TCON data enable 0xB: INCLK div1k 0xC: DOTCLK div1k 0xD-0xF: Reserved

Table 13: Sync Measurement Registers (Sheet 4 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_V_SEL	0x0114	R/W	[7:4]	0x0	Selects a vertical signal for measurement of the high pulse width. 0x0: Analog vsync 0x1: Composite vsync 0x2: SOG vsync 0x3: DVI vsync 0x4: YUV vsync 0x5: YUV vert enab (locally generated) 0x6: DVI vert enab (locally generated) 0x7: TCON vsync 0x8 - 0xF: Reserved
		R/W	[3:0]	0x0	Selects a vertical signal for measurement of period and polarity. 0x0: Analog vsync 0x1: Composite vsync 0x2: SOG vsync 0x3: DVI vsync 0x4: YUV vsync 0x5: YUV vert enable (locally generated) 0x6: DVI vert enable (locally generated) 0x7: TCON vsync
SMEAS_STATUS_MASK	0x0119	R/W	[7]	0x0	Mask bit for hsync polarity check 0: ignore 1: check
		R/W	[6]	0x0	Mask bit for vsync polarity check 0: ignore 1: check
			[5:4]		Reserved
		R/W	[3]	0x0	Mask bit for vert pulse width check 0: ignore 1: check
		R/W	[2]	0x0	Mask bit for h per v check 0: ignore 1: check
		R/W	[1]	0x0	Mask bit for h period check 0: ignore 1: check
		R/W	[0]	0x0	Mask bit for v period check 0: ignore 1: check
SMEAS_H_NUM_LINES	0x011A	R/W	[7:0]	0x0	Number of lines to measure for Horizontal period. Valid range is 1 to 255.
SMEAS_H_SKIP_L	0x011B	R/W	[7:0]	0x0	Number of lines to skip before starting a horizontal measurement. The skip counter counts from the chosen vertical source and edge. [7:0]
SMEAS_H_SKIP_H	0x011C	R/W	[7:4]		Reserved
			[3:0]		Number of lines to skip before starting a horizontal measurement. The skip counter counts from the chosen vertical source and edge. [11:8]

Table 13: Sync Measurement Registers (Sheet 5 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_SKEW_CTRL	0x011D		[7:3]	0x0	Reserved
		R/W	[2]	0x0	1 = delay vsync a number of XCLKs specified in SMEAS_DELAY_VSYNC
			[1]	0x0	Reserved
		R/W	[0]	0x0	Write a rising edge to start the hv-skew measurement.
SMEAS_SKEW_THRES	0x011E	R	[7:0]	0x5	Test skew limit in XCLKs. If the skew is less than this test limit, the SMEASE_SKEW_STATUS register will report an error condition. SMEAS_DELAY_VSYNC should be reprogrammed until the skew is large enough to prevent vcount ambiguity.
SMEAS_DELAY_VSYNC	0x011F	R/W	[7:0]	0x3	Number of XCLKs to delay vsync.
SMEAS_REF_XK_PER_H_L	0x0120	R/W	[7:0]	0x0	Reference value for XCLKs per horizontal event actual value = programmed value + 1
SMEAS_REF_XK_PER_H_M	0x0121	R/W	[7:0]	0x0	
SMEAS_REF_XK_PER_H_H	0x0122	R/W	[7:0]	0x0	
SMEAS_REF_XK_PER_V_L	0x0123	R/W	[7:0]	0x0	Reference value for XCLKs per vertical event actual value = programmed value + 2
SMEAS_REF_XK_PER_V_M	0x0124	R/W	[7:0]	0x0	
SMEAS_REF_XK_PER_V_H	0x0125	R/W	[7:0]	0x0	
SMEAS_REF_H_PER_V_L	0x0126	R/W	[7:0]	0x0	Reference value for horizontal events per vertical event
SMEAS_REF_H_PER_V_H	0x0127	R/W	[7:0]	0x0	
SMEAS_REF_XK_V_PER_HI_L	0x0128	R/W	[7:0]	0x0	Reference value for vertical pulse width measurement result in XCLKs. actual value = programmed value + 1
SMEAS_REF_XK_V_PER_HI_M	0x0129	R/W	[7:0]	0x0	
SMEAS_REF_XK_V_PER_HI_H	0x012A	R/W	[7:0]	0x0	
SMEAS_REF_POLARITY	0x012B		[7:2]	0x0	Reserved
		R/W	[1]	0x0	Reference value for Hsync polarity. 0: active low 1: active high
		R/W	[0]	0x0	Reference value for Vsync polarity. 0: active low 1: active high
SMEAS_XK_HTOL_EXP	0x012C	R/W	[7:4]	0x0	Reserved
			[3:0]	0x0	Horizontal tolerance; +/- 2^n XCLKs
SMEAS_XK_VTOL_EXP	0x012D		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Vertical tolerance; +/- 2^n XCLKs
SMEAS_HSYNC_VTOL	0x012E		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	Horizontal per vertical tolerance, +/- 2^n
SMEAS_FILTR_HS_WIDTH	0x012F	R/W	[7:0]	0x1	Refer to register 0x0111
SMEAS_ACT_POLLING	0x013F		[7:1]	0x0	Reserved
		R	[0]	0x0	Toggle on activity status update in Free-running mode. No function in one-shot mode.

Table 13: Sync Measurement Registers (Sheet 6 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_ANA_ACT	0x0140		[7:5]	0x0	Reserved
		R	[4]	0x0	Composite sync is active
		R	[3]	0x0	Vsync from SOG separator is active
		R	[2]	0x0	Comp vsync from composite sync separator is active
		R	[1]	0x0	Analog hsync is active
		R	[0]	0x0	Analog vsync is active
SMEAS_DVI_ACT	0x0141		[7:2]	0x0	Reserved
		R	[1]	0x0	DVI enable is active
		R	[0]	0x0	DVI clk / 1K is active
SMEAS_YUV_ACT	0x0142		[7:5]	0x0	Reserved
		R	[4]	0x0	TCON vsync is active.
		R	[3]	0x0	TCON hsync is active.
		R	[2]	0x0	TCON enable is active.
		R	[1]	0x0	YUV enable is active.
		R	[0]	0x0	YUV clk / 1K is active.
SMEAS_ANA_STUCK	0x0143		[7:5]	0x0	Reserved
		R	[4]	0x0	Comp sync is stuck at 1(high)/0(low)
		R	[3]	0x0	Vsync from SOG separator is stuck at 1(high)/0(low)
		R	[2]	0x0	Comp vsync from separator is stuck at 1(high)/0(low)
		R	[1]	0x0	Analog hsync is stuck at 1(high)/0(low)
		R	[0]	0x0	Analog vsync is stuck at 1(high)/0(low)
SMEAS_DVI_STUCK	0x0144		[7:2]	0x0	Reserved
		R	[1]	0x0	DVI data enable is stuck at 1(high)/0(low)
		R	[0]	0x0	DVI clk / 1K is stuck at 1(high)/0(low)
SMEAS_YUV_STUCK	0x0145	R	[7:5]	0x0	Reserved
		R	[4]	0x0	TCON vsync is stuck at 1(high)/0(low)
		R	[3]	0x0	TCON hsync is stuck at 1(high)/0(low)
		R	[2]	0x0	TCON data enable is stuck at 1(high)/0(low)
		R	[1]	0x0	YUV data enable is stuck at 1(high)/0(low)
		R	[0]	0x0	YUV clk / 1K is stuck at 1(high)/0(low)
SMEAS_XK_PER_H_L	0x0146	R	[7:0]	0x0	XCLKs per horizontal event - 1
SMEAS_XK_PER_H_M	0x0147	R	[7:0]	0x0	
SMEAS_XK_PER_H_H	0x0148	R	[7:0]	0x0	
SMEAS_XK_PER_V_L	0x0149	R	[7:0]	0x0	XCLKs per vertical event - 1
SMEAS_XK_PER_V_M	0x014A	R	[7:0]	0x0	
SMEAS_XK_PER_V_H	0x014B	R	[7:0]	0x0	

Table 13: Sync Measurement Registers (Sheet 7 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_H_PER_V_L	0x014C	R	[7:0]	0x0	Horizontal events per vertical event
SMEAS_H_PER_V_H	0x014D	R	[7:0]	0x0	
SMEAS_SK_V_HI_L	0x014E	R	[7:0]	0x0	Vertical high time in XCLKs - 1
SMEAS_SK_V_HI_M	0x014F	R	[7:0]	0x0	
SMEAS_SK_V_HI_H	0x0150	R	[7:0]	0x0	
SMEAS_TIMEOUT_STATUS	0x0151		[7:2]	0x0	Reserved
		R	[1]	0x0	Indicates that the horizontal measurement timed out.
		R	[0]	0x0	Indicates that the vertical measurement timed out.
SMEAS_STATUS_RANGE	0x0152	R	[7]	0x0	In Free-running mode any of the status bits can change at the end of each measurement. In One-shot mode any of the status bits can change at the completion of the measurement. The meas_sticky_status bit is a bitwise OR of bits[3:0] (before the bitwise OR, the mask in SMEAS_STATUS_MASK is AND in) and is sticky. The only way to reset it is for software to write a zero into this bit. This bit goes to the scaler to blank the scaler output. A write to this reg will reset it to 0.
		R	[6]	0x0	Indicates that one of the measured polarities does not match the reference value.
		R	[5]	0x0	Hsync (selected by SMEAS_H_SEL) polarity. 0: active low 1: active high
		R	[4]	0x0	Vsync (selected by SMEAS_V_SEL) polarity. 0: active low 1: active high
		R	[3]	0x0	Indicates that the vertical pulse width measurement exceeded the reference +/- tolerance range.
		R	[2]	0x0	Indicates that the horizontal per vertical measurement exceeded the reference +/- tolerance range.
		R	[1]	0x0	Indicates that the XCLKs per horizontal measurement exceeded the reference +/- tolerance range.
		R	[0]	0x0	Indicates that the XCLKs per vertical measurement exceeded the reference +/- tolerance range.
SMEAS_MEAS_POLLING	0x0153		[7:2]	0x0	Reserved
		R	[1]	0x0	Toggle on h meas Free-running mode, at end of each meas. No function on one-shot mode.
		R	[0]	0x0	Toggle on v meas Free-running mode, at end of each meas. No function on one-shot mode.

Table 13: Sync Measurement Registers (Sheet 8 of 8)

Register Name	Addr	Mode	Bits	Default	Description
SMEAS_SKEW_STATUS	0x0154		[7:2]	0x0	Reserved
		R	[1]	0x0	0: hsync to vsync skew above threshold 1: hsync to vsync skew below theshold
		R	[0]	0x0	0: skew measurement running 1: skew measurement finished
SMEAS_V_OUTOF_RNG	0x0155	R	[7:0]	0x0	The number of times the XCLKs per vertical reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_H_OUTOF_RNG	0x0156	R	[7:0]	0x0	The number of times the XCLKs per horizontal reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_HV_OUTOF_RNG	0x0157	R	[7:0]	0x0	The number of times the horizontal per vertical reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_VHI_OUTOF_RNG	0x0158	R	[7:0]	0x0	The number of times the vertical pulse width in XCLKs reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_HPOL_OUTOF_RNG	0x0159	R	[7:0]	0x0	The number of times the horizontal polarity reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].
SMEAS_VPOL_OUTOF_RNG	0x015A	R	[7:0]	0x0	The number of times the vertical polarity reference/meas comparison has been out of range. Maximum is 240. Clear by setting SMEAS_CLEAR[1].

2.10 Sync Mux Block

The Sync Mux (SMUX) block provides the following functions:

- selects between all possible sync signals
- generates missing sync signals
- selects between original and generated signals for output
- generates the clamp signal for the ADC

Table 14: Sync Mux Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SMUX_CTRL0	0x0200	R/W	[7]	0x0	Select TCON[7] as internal_hsync source. Overrides SMUX_CTRL0[1:0] selection.
		R/W	[6]	0x0	Select TCON[6] as internal_vsync source. Overrides SMUX_CTRL0[3:2] selection.
		R/W	[5]	0x0	Select TCON[5] as internal_enable source. Overrides SMUX_CTRL0[4] selection.
		R/W	[4]	0x0	Internal_enab select 0: DVI 1: YUV
		R/W	[3:2]	0x0	Vsync_internal select 0x0: DVI 0x1: SRT vsync (normally analog) 0x2: YUVi 0x3: composite sync decoder
		R/W	[1:0]	0x0	Hsync_internal select 0x0: DVI 0x1: LLK hsync (normally analog) 0x2: YUVi 0x3: raw vga hsync (may have jitter)
SMUX_CTRL1	0x0201		[7:6]	0x0	Reserved
		R/W	[5]	0x0	Vsync_out invert
		R/W	[4]	0x0	Hsync_out invert
		R/W	[3]	0x0	V_reference edge select 0: falling 1: rising
		R/W	[2]	0x0	V_reference select 0: venab_generated 1: vsync_internal
		R/W	[1]	0x0	H_reference edge select 0: falling 1: rising
		R/W	[0]	0x0	H_reference select 0: enab_internal 1: hsync_internal

Table 14: Sync Mux Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SMUX_CTRL2	0x0202	R	[7]	0x0	V_reference toggle output
		R/W	[6]	0x0	Software odd set (for testing odd params on the bench)
		R/W	[5:4]	0x0	Odd_out select 0x0: YUV 0x1: v_reference toggle 0x2: SMUX_CTRL2[6] 0x3: Reserved
		R/W	[3]	0x0	Valid_out select 0: YUV 1: valid_generated
		R/W	[2]	0x0	Enab_out select 0: enab_internal 1: enab_generated
		R/W	[1]	0x0	Vsync_out select 0: vsync_internal 1: hsync_generated
		R/W	[0]	0x0	Hsync_out select 0: hsync_internal 1: hsync_generated
SMUX_CLAMP_SET_L	0x0203	R/W	[7:0]	0x0	ADC clamp signal rising edge [11:0], relative to selected horizontal reference signal, in INCLKs (pixels)
SMUX_CLAMP_SET_H	0x0204	R/W	[3:0]	0x0	
SMUX_CLAMP_RST_L	0x0205	R/W	[7:0]	0x0	ADC clamp falling edge [11:0]
SMUX_CLAMP_RST_H	0x0206	R/W	[3:0]	0x0	
SMUX_HENAB_SET_L	0x0207	R/W	[7:0]	0x0	Horizontal enable start [11:0] (left edge of image) relative to the selected horizontal reference edge in INCLKs (pixels))
SMUX_HENAB_SET_H	0x0208	R/W	[3:0]	0x0	
SMUX_HENAB_RST_L	0x0209	R/W	[7:0]	0x0	Horizontal enable end [11:0]
SMUX_HENAB_RST_H	0x020A	R/W	[3:0]	0x0	
SMUX_VENAB_SET_L	0x020B	R/W	[7:0]	0x0	Vertical enable start [11:0] (top edge of image) relative to the selected vertical reference edge (in lines)
SMUX_VENAB_SET_H	0x020C	R/W	[3:0]	0x0	
SMUX_VENAB_RST_L	0x020D	R/W	[7:0]	0x0	Vertical enable end
SMUX_VENAB_RST_H	0x020E	R/W	[3:0]	0x0	
SMUX_HSYNC_PHASE	0x020F	R/W	[7:0]	0x0	Number of horizontal pixels/INCLKs that the generated hsync edge is from the horizontal reference edge. 2’s complement [-128,127]
SMUX_VSYNC_PHASE	0x0210	R/W	[7:0]	0x0	Number of vertical lines that the generated vsync edge is from the vertical reference edge. 2’s complement [-128,127]

2.11 Data Mux Block

Data mux provides the following functions:

- selection of one among three data sources
- debug modes (e.g. bit order swap, color swap)

Table 15: Data Mux Registers

Register	Addr.	Mode	Bits	Default	Description
DMUX_CHANSEL	0x0280		[7]	0x0	Reserved
		R/W	[6]	0x0	0: normal 1: msb/lsb byte flip
		R/W	[5:3]	0x0	If enabled by [2] 0x0: Reserved 0x1: R & G bytes are swapped 0x2: B & G bytes are swapped 0x3: R => G, G => B, B => R 0x4: R & B bytes are swapped 0x5: R => B, G => R, B => G 0x0, 0x6-0x7: Reserved
		R/W	[2]	0x0	0: normal 1: enable color swap
		R/W	[1:0]	0x0	Video Source Select 0x0: ADC data 0x1: YUV data 0x2: DVI data 0x3: DVI xor YUV xor ADC (for test only)

2.12 Data Measurement Block

The Data Measurement module measures several characteristics of the data and sync signals. Data measurements are taken over a programmable window as defined by an upper left (mix_x, min_y) and a lower right (max_x, max_y), which may be the whole frame. Measurements are programmable either per color channel or over all color channels.

This module computes all measurements of sync and data format that are done in the INCLK domain. The Sync Measurement module does measurements in the XCLK domain. The INCLKs per DE measurement does not use the window feature. It measures the number of INCLK per DE and returns the result for every line.

All unused or reserved bits return as zero.

Windows are relative to Sync pulses. A window defined from (0,0) - (0xFFF, 0xFFF) goes from sync to sync. The reference edge to use, rising or falling, is also programmable per X and Y coordinates. Configure SMUX to provide a positive polarity sync to the DMEAS block. All window enables reset at 0 and always reset on the rising or falling edge of sync.

See the description of the specific PHM and DMM measurements performed within DMEAS here below. Most algorithms are run over separate or all color channels. Most algorithms also contain a threshold value to zero out noise and / or amplify edges. Algorithm, Color, Threshold, or Window Control changes are accepted at the end of a valid measurement, the current measurement in progress is not affected.

Software requests measurements in one of two ways:

- One shot - synchronous with respect to the microcontroller.
- Free Run - asynchronous with respect to the microcontroller.

In One-shot mode, the block indicates that measurement is valid through an auto-clear of start condition.

In Free-running mode, the block indicates that measurement is valid through a polling bit. In Free-running mode, a freeze bit is provided to freeze the results. Measurements continue with the polling bit active, but they are not updated if the Freeze bit is set.

2.12.1 Edge Intensity

The Edge Intensity measurement is the sum of the absolute value of the delta between adjacent pixels. A programmable threshold is applied to zero out noise and amplify edges.
Equation:

Delta_val = abs(pixelA - pixelB) - threshold;

Delta_val = Delta_val < 0 ? 0: Delta_val;

Sum += Delta_val;

For all 3 color channels:
Sum += Delta_val on Red channel + Delta_val on Green channel + Delta_val on Blue channel

2.12.2 Pixel Sum

The Pixel Sum is the sum of all selected pixels for either a specific color channel or all color channels within the window specified.

2.12.3 Min / Max

The Min / Max reports the minimum and maximum pixel found withing the window specified.

2.12.4 PCD

Pixel cumulative distribution function reports the total number of pixels greater than (or less than) a programmable threshold.

To switch between pixels greater than or pixel less than the threshold, a control bit is provided in the DMM_Mode register when requesting a measurement.

2.12.5 H Position Min / Max

Horizontal position measures the start and end of video data in INCLKs relative to the posedge of hsync.

Data horizontal start is defined as the number of INCLKs between posedge of hsync and the "first data pixel".

First data pixel is either:

- first pixel greater than the programmable threshold value, or
- first pixel with the absolute value (current pixel - previous pixel) is greater than the programmable threshold value

Data horizontal end is defined as the number of INCLKs between posedge of hsync and the "last data pixel plus one". The search for the last pixels ends at the end of a window.

Last data pixel plus one is either:

- pixel after the last pixel that is greater than the programmable threshold value,or
- last pixel with the absolute value(current pixel - previous pixel) is greater than the programmable threshold value.

When measurement is required, a control bit in the DMM_Mode register is used to switch between the two threshold methods for first and last pixels.

The first and last pixels are measured for each line, and the earliest first and latest last for the selected pixel area are reported out at the end of the measurement. The intention is that "last data pixel plus one" minus "first data pixel" is equal to the horizontal width of the video format.

2.12.6 V Position Min / Max

Vertical position measures the start and end of video data in hsyncs relative to the posedge of vsync.

Data vertical start is defined as the number of hsyncs between posedge of vsync and the "first data pixel line".

First data pixel line definition is the first line with at least one pixel greater then the programmable threshold.

Data vertical end is defined as the number of hsyncs between posedge of vsync and the "first blanking line after data plus one". The first blanking line is detected and confirms that each subsequent line contains no data pixels. The confirmation of the first blanking line measurement ends at the posedge of vsync.

First blanking line after data definition is the row after the last row with at least one pixel greater than the programmable threshold.

The first and last data pixel lines are measured within a frame. The earliest first and latest last data pixels corresponding to the selected pixel area are reported out at the end of the measurement. The intention is that "data vertical end plus one" minus "data vertical start" is equal to the vertical height of the video format.

2.12.7 DE Size

DE Size measures the number of INCLKs per data enable. DVI input measures precisely the input image horizontal size.

At the end of the measurement (DE falling edge), the measured value is compared to a programmed expected value +/- a programmed threshold. If the expected value is within the threshold, the DE_size_mismatch flag is not set. If the measued size is outside the threshold, the DE_size_mismatch flag is set.

In Free-running mode, results are updated at every line. The DE_size_mismatch flag is set at DE falling edge and reset at DE rising edge.

In One-shot mode, results are updated once and kept until they are cleared by software. The DE_size_mismatch flag can only be cleared when the reset flag bit is set by software.

Table 16: Data Measurement Registers (Sheet 1 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_ALG_CTRL	0x0900		[7:5]		Reserved
		R/W	[4]	0x0	Interlace Mode Enable
		R/W	[3]	0x0	0: use data valid (TV mode only) 1: use data enable for data valid
		R/W	[2:0]	0x0	Algorithm 0x0: PHM Edge Intensity & Pixel Sum 0x1: DMM Min / Max 0x2: DMM PCD 0x3: DMM H position and V position 0x4: DMM DE size 0x5 - 0x7: Reserved

Table 16: Data Measurement Registers (Sheet 2 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_COLOR_CTRL	0x0901		[7:4]		Reserved
		R/W	[3:2]	0x0	color channel for DMM Min / Max, PCD; does not apply to H position, V position 0x0: All 0x1: Red 0x2: Green 0x3: Blue
		R/W	[1:0]	0x0	color channel for PHM Edge Intensity and Pixel Sum algorithms 0x0: All 0x1: Red 0x2: Green 0x3: Blue
DMEAS_THR_PHM_EDGE	0x0902	R/W	[7:0]	0x0	threshold value for PHM Edge Intensity algorithm
DMEAS_THR_DMM	0x0903	R/W	[7:0]	0x0	threshold value for DMM Min / Max, PCD, H position, V position
DMEAS_WIN_PHM_MINX_L	0x0904	R/W	[7:0]	0x0	minimum X PHM window [7:0]
DMEAS_WIN_PHM_MINX_H	0x0905		[7:4]		Reserved
		R/W	[3:0]		minimum X PHM window [11:8] relative to hsync
DMEAS_WIN_PHM_MAXX_L	0x0906	R/W	[7:0]	0xFFF	maximum X PHM window [7:0]
DMEAS_WIN_PHM_MAXX_H	0x0907		[7:4]		Reserved
		R/W	[3:0]		maximum X PHM window [11:8] Relative to hsync, must be less than input horizontal total (LLK_LINELEN for analog input).
DMEAS_WIN_PHM_MINY_L	0x0908	R/W	[7:0]	0x0	minimum Y PHM window [7:0]
DMEAS_WIN_PHM_MINY_H	0x0909		[7:4]		Reserved
		R/W	[3:0]		minimum Y PHM window [11:8] relative to vsync
DMEAS_WIN_PHM_MAXY_L	0x090A	R/W	[7:0]	0xFFF	maximum Y PHM window [7:0]
DMEAS_WIN_PHM_MAXY_H	0x090B		[7:4]		Reserved
		R/W	[3:0]		maximum Y PHM window [11:8] relative to vsync
DMEAS_WIN_DMM_MINX_L	0x090C	R/W	[7:0]	0x0	minimum X DMM window [7:0]
DMEAS_WIN_DMM_MINX_H	0x090D		[7:4]	0x0	Reserved
		R/W	[3:0]		minimum X DMM window [11:8] relative to hsync, does not apply for V position
DMEAS_WIN_DMM_MAXX_L	0x090E	R/W	[7:0]	0xFFF	maximum X DMM window [7:0]
DMEAS_WIN_DMM_MAXX_H	0x090F		[7:4]	0xFFF	Reserved
		R/W	[3:0]		maximum X DMM window [11:8] relative to hsync, does not apply for V position
DMEAS_WIN_DMM_MINY_L	0x0910	R/W	[7:0]	0x0	minimum Y DMM window [7:0]

Table 16: Data Measurement Registers (Sheet 3 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_WIN_DMM_MINY_H	0x0911		[7:4]		Reserved
		R/W	[3:0]		minimum Y DMM window [11:8] relative to vsync
DMEAS_WIN_DMM_MAXY_L	0x0912	R/W	[7:0]	0xFFF	maximum Y DMM window [7:0]
DMEAS_WIN_DMM_MAXY_H	0x0913		[7:4]		Reserved
		R/W	[3:0]		maximum Y DMM window [11:8] relative to vsync
DMEAS_PHM_EDGESEL	0x0914		[7:2]	0xFFF	Reserved
		R/W	[1]	0x0	vsync edge select for PHM measurements 0: rising edge 1: falling edge
		R/W	[0]	0x0	hsync edge select for PHM measurements 0: rising edge 1: falling edge
DMEAS_DMM_EDGESEL	0x0915		[7:2]		Reserved
		R/W	[1]	0x0	vsync edge select for DMM measurements 0: rising edge 1: falling edge
		R/W	[0]	0x0	hsync edge select for DMM measurements 0: rising edge 1: falling edge
DMEAS_PHM_MODE_CTRL	0x0916		[7:5]		Reserved
		R/W	[4]	0x0	clear PHM result registers
		R/W	[3]	0x0	0: Do not freeze the results in Free-running mode. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results in Free-running mode. The polling bit will still toggle and the block continues to free run; however, results will not update. No meaning in one-shot mode.
		R/W	[2]	0x0	PHM measurement polling bit. Toggles at the end of each measurement in free-run mode. Undefined in one-shot mode.
		R/W	[1]	0x0	PHM algorithm measurement start. In free-run mode it enables measurements. In one-shot mode it triggers the start of a measurement and is reset to zero when the measurement is complete.
		R/W	[0]	0x0	0: PHM free-run mode. 1: PHM one-shot mode.

Table 16: Data Measurement Registers (Sheet 4 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_DMM_MODE_CTRL	0x0917	R/W	[7]	0x0	Listen to odd frame only. Applies only if the odd signal is present from YUV. The results in the Vertical Position algorithm are updated with only the odd frame if this bit is set.
		R/W	[6]	0x0	PCD algorithm 0: pixel < threshold 1: pixel >= threshold
		R/W	[5]	0x0	horizontal position algorithm 0: pixel > threshold 1: abs (pixel - previous pixel) > threshold
		R/W	[4]	0x0	clear DMM result registers
		R/W	[3]	0x0	0: Do not freeze the results in Free-running mode. New result will be available on the next and subsequent toggle of the polling bit. 1: Freeze the current results in Free-running mode. The polling bit will still toggle and the block continues to free run; however, results will not update. No meaning in one-shot mode.
		R/W	[2]	0x0	DMM measurement polling bit. Toggles at the end of each measurement in free-run mode. Undefined in one-shot mode.
		R/W	[1]	0x0	DMM algorithm measurement start. In free-run mode it enables measurements. In one-shot mode it triggers the start of a measurement and is reset to zero when the measurement is complete.
		R/W	[0]	0x0	0: DMM Free-running mode. 1: DMM One-shot mode.
DMEAS_DMM_DE_REF_L	0x0918	R/W	[7:0]	0x0	DE Size expected result
DMEAS_DMM_DE_REF_H	0x0919	R/W	[7:0]		
DMEAS_DMM_DE_TOL	0x091A	R/W	[7:0]	0x0	DE Size tolerance threshold value
DMEAS_DMM_DE_RST	0x091B		[7:1]		Reserved
		R/W	[0]	0x0	Reset the DMM flag in One-shot mode
DMEAS_DATA_PHM_EDGE0	0x091C	R	[7:0]		Result of PHM edge intensity algorithm
DMEAS_DATA_PHM_EDGE1	0x091D	R	[7:0]		
DMEAS_DATA_PHM_EDGE2	0x091E	R	[7:0]		
DMEAS_DATA_PHM_EDGE3	0x091F	R	[7:0]		
DMEAS_DATA_PHM_PSUM0	0x0920	R	[7:0]		Result for PHM pixel sum algorithm
DMEAS_DATA_PHM_PSUM1	0x0921	R	[7:0]		
DMEAS_DATA_PHM_PSUM2	0x0922	R	[7:0]		
DMEAS_DATA_PHM_PSUM3	0x0923	R	[7:0]		
DMEAS_DATA_DMM_MIN	0x0924	R	[7:0]		Result for DMM Minimum pixel value found.
DMEAS_DATA_DMM_MAX	0x0925	R	[7:0]		Result for DMM Maxmum pixel value found.

Table 16: Data Measurement Registers (Sheet 5 of 5)

Register Name	Addr	Mode	Bits	Default	Description
DMEAS_DATA_DMM_PCD_L	0x0926	R	[7:0]		Result for DMM pixel cumulative distribution
DMEAS_DATA_DMM_PCD_M	0x0927	R	[7:0]		
DMEAS_DATA_DMM_PCD_H	0x0928	R	[7:0]		
DMEAS_DATA_DMM_HPOSMIN_L	0x0929	R	[7:0]		DMM Hposition of first pixel [7:0]
DMEAS_DATA_DMM_HPOSMIN_H	0x092A		[7:4]		Reserved
		R	[3:0]		DMM Hposition of first pixel [11:8]
DMEAS_DATA_DMM_HPOSMAX_L	0x092B	R	[7:0]		DMM Hposition of last pixel [7:0]
DMEAS_DATA_DMM_HPOSMAX_H	0x092C		[7:4]		Reserved
		R	[3:0]		DMM Hposition of last pixel [11:8]
DMEAS_DATA_DMM_VPOSMIN_L	0x092D	R	[7:0]		DMM Vposition of first line [7:0]
DMEAS_DATA_DMM_VPOSMIN_H	0x092E		[7:4]		Reserved
		R	[3:0]		DMM Vposition of first line [11:8]
DMEAS_DATA_DMM_VPOSMAX_L	0x092F	R	[7:0]		DMM Vposition of last line [7:0]
DMEAS_DATA_DMM_VPOSMAX_H	0x0930		[7:4]		Reserved
		R	[3:0]		DMM Vposition of last line [11:8]
DMEAS_DATA_DMM_SIZE_L	0x0931	R	[7:0]		number of INCLKs per DE = input horizontal pixel size for DVI mode selection.
DMEAS_DATA_DMM_SIZE_H	0x0932	R	[7:0]		
DMEAS_DATA_DMM_DE_STATUS	0x0933		[7:1]		Reserved
		R	[0]		DE measured value does not match expected value within the DE tolerance
DMEAS_SCR_PAD_0	0x0934	R	[7:0]	0x0	Scratch Pad Registers
DMEAS_SCR_PAD_1	0x0935	R/W	[7:0]		
DMEAS_SCR_PAD_2	0x0936	R/W	[7:0]		
DMEAS_SCR_PAD_3	0x0937	R/W	[7:0]		
DMEAS_SCR_PAD_4	0x0938	R/W	[7:0]		
DMEAS_SCR_PAD_5	0x0939	R/W	[7:0]		
DMEAS_SCR_PAD_6	0x093A	R/W	[7:0]		
DMEAS_SCR_PAD_7	0x093B	R/W	[7:0]		
DMEAS_SCR_PAD_8	0x093C	R/W	[7:0]		
DMEAS_SCR_PAD_9	0x093D	R/W	[7:0]		
DMEAS_SCR_PAD_10	0x093E	R/W	[7:0]		
DMEAS_SCR_PAD_11	0x093F	R/W	[7:0]		
DMEAS_SCR_PAD_12	0x0940	R/W	[7:0]		
DMEAS_SCR_PAD_13	0x0941	R/W	[7:0]		
DMEAS_SCR_PAD_14	0x0942	R/W	[7:0]		
DMEAS_SCR_PAD_15	0x0943	R/W	[7:0]		

2.13 Programmable Nonlinearity Block

The programmable nonlinearity (PNL) block performs a gamma type enhancement to all color channels prior to the scaler to suppress halo and roping effects. For best performance, tune the

PNL block to the LCD gamma value, then the post-scaler gamma RAM implements the corresponding inverse gamma function.

Table 17: PNL Registers

Register Name	Addr	Mode	Bits	Default	Description
PNL_CTRL	0x0080	R/W	[7:6]	0x0	Reserved
			[5:0]	0x0	0x00: bypass 0x01 - 0x1F: gamma <1.0 0x20 - 0x3F: gamma >1.0 0x30: gamma = 2.2

2.14 Scaler Block

The scale module resizes images from one resolution to another. For this, a 3x3 non-separable scaling filter performs a dot product of the input pixel values with a weighting vector computed from the chosen filtering function. To sharpen text without introducing excessive artifacts, the output pixel contrast level is adjusted with the context value measured over a 3x3 grid in the relevant area of the source image.

For proper scaler operation, set the SCLK frequency to be greater than the max of dclk and in_hpixel x dclk_freq / (dest_hpixel x pixel_avg).

Table 18: Scaler Block Registers (Sheet 1 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SCL_SRC_HPIX_L	0x0A00	R/W	[7:0]	0x0	input horizontal resolution in top 12 bits Bits [3:0] must be set to zero. If pixel averaging is necessary then this register contains the averaged, round-down resolution, e.g, if the original resolution is 65 and if the mode is averaging-by-2 then 32 should be programmed in this register.
SCL_SRC_HPIX_H	0x0A01	R/W	[7:0]		
SCL_SRC_VPIX_L	0x0A02	R/W	[7:0]	0x0	Input Vertical Resolution [3:0] must be set to 0.
SCL_SRC_VPIX_H	0x0A03	R/W	[7:0]		
SCL_DES_HPIX_L	0x0A04	R/W	[7:0]	0x0	scaled active area width in pixels [15:4] = integer; [3:0] = fraction
SCL_DES_HPIX_H	0x0A05	R/W	[7:0]		
SCL_DES_VPIX_L	0x0A08	R/W	[7:0]	0x0	scaled active area height in lines [15:4] = integer; [3:0] = fraction
SCL_DES_VPIX_H	0x0A09	R/W	[7:0]		
SCL_HPOS_L	0x0A0A	R/W	[7:0]	0x0	horizontal position of upper left pixel of active output data [15:4] = integer; [3:0] = fraction
SCL_HPOS_H	0x0A0B	R/W	[7:0]		
SCL_VPOS_E_L	0x0A0E	R/W	[7:0]	0x0	vertical position of upper left pixel of output data for even/non-interlace frames [15:4] = integer; [3:0] = fraction
SCL_VPOS_E_H	0x0A0F	R/W	[7:0]		
SCL_VPOS_O_L	0x0A10	R/W	[7:0]	0x0	vertical position of the upper left pixel of output data of odd fields bits [15:4] = integer; bits [3:0] = fraction
SCL_VPOS_O_H	0x0A11	R/W	[7:0]		
SCL_THRES_SLOPE	0x0A12	R/W	[7:6]	0x0	Reserved
			[5:0]	0x28	slope of the contrast amplification function

Table 18: Scaler Block Registers (Sheet 2 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SCL_THRES_OFFSET_L	0x0A13	R/W	[7:0]	0x40	offset of the contrast amplification function [7:0]
SCL_THRES_OFFSET_H	0x0A14	R/W	[7:2]	0x0	Reserved
		R/W	[1:0]	0x2	offset of the contrast amplification function [9:8]
SCL_CBBYPASS	0x0A15	R/W	[7:2]	0x0	Reserved
		R/W	[1]	0x0	0: normal 1: TCON control of contrast amplification
		R/W	[0]	0x0	0: contrast amplification enabled 1: bypass contrast amplification
SCL_CON_CAL_SEL	0x0A16		[7:1]		Reserved
		R/W	[0]	0x0	0: context = max of RGB pk-pk 1: context = sum of RGB pk-pk
SCL_TESTCON	0x0A17		[7:2]		6b contrast amplification test data
		R/W	[1:0]	0x0	0x0, 0x3: normal 0x1: force input data into the contrast amplifiation function to bits [7:2] 0x2: force the output context data to be bits [5:2]
SCL_LUT1	0x0A18	R/W	[7:0]	0xFA	sigmoidal function LUT entry 1, 8b 2's complement
SCL_LUT2	0x0A19	R/W	[7:0]	0xF7	sigmoidal function LUT entry 2, 8b 2's complement
SCL_LUT3	0x0A1A	R/W	[7:0]	0xF7	sigmoidal function LUT entry 3, 8b 2's complement
SCL_LUT4	0x0A1B	R/W	[7:0]	0xFC	sigmoidal function LUT entry 4, 8b 2's complement
SCL_LUT5	0x0A1C	R/W	[7:0]	0x2	sigmoidal function LUT entry 5, 8b 2's complement
SCL_LUT6	0x0A1D	R/W	[7:0]	0x0D	sigmoidal function LUT entry 6, 8b 2's complement
SCL_LUT7	0x0A1E	R/W	[7:0]	0x17	sigmoidal function LUT entry 7, 8b 2's complement
SCL_LUT8	0x0A1F	R/W	[7:0]	0x21	sigmoidal function LUT entry 8, 8b 2's complement
SCL_LUT9	0x0A20	R/W	[7:0]	0x28	sigmoidal function LUT entry 9, 8b 2's complement
SCL_LUT10	0x0A21	R/W	[7:0]	0x2C	sigmoidal function LUT entry 10, 8b 2's complement
SCL_LUT11	0x0A22	R/W	[7:0]	0x2C	sigmoidal function LUT entry 11, 8b 2's complement
SCL_LUT12	0x0A23	R/W	[7:0]	0x28	sigmoidal function LUT entry 12, 8b 2's complement
SCL_LUT13	0x0A24	R/W	[7:0]	0x21	sigmoidal function LUT entry 13, 8b 2's complement
SCL_LUT14	0x0A25	R/W	[7:0]	0x17	sigmoidal function LUT entry 14, 8b 2's complement

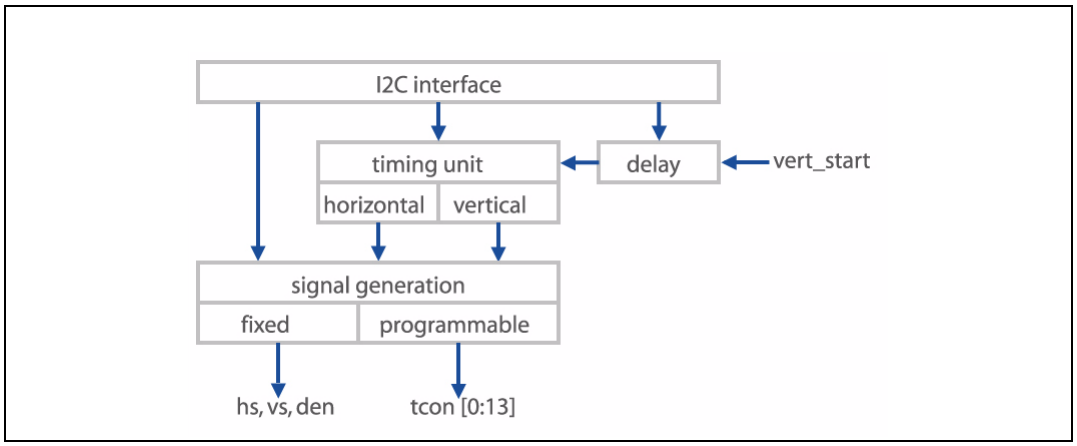
Table 18: Scaler Block Registers (Sheet 3 of 3)

Register Name	Addr	Mode	Bits	Default	Description
SCL_LUT15	0x0A26	R/W	[7:0]	0x0C	sigmoidal function LUT entry 15, 8b 2's complement
SCL_BGCOLOR_R	0x0A27	R/W	[7:0]	0x0	red component of background color
SCL_BGCOLOR_G	0x0A28	R/W	[7:0]	0x0	green component of background color
SCL_BGCOLOR_B	0x0A29	R/W	[7:0]	0x0	blue component of background color
SCL_BCOLOR_CTRL	0x0A2A	R/W	[7]	0x0	0: normal 1: force image to background color
		R/W	[6]	0x0	top & botton border control 0: pixel replicating 1: background color blending
		R/W	[5]	0x0	left & right border control: 0: pixel replicating 1: background color blending
		R/W	[4]	0x0	force output data as described in bit [1] when the maximum output vertical is reached.
		R/W	[3]	0x0	force output data as described in bit [1] when an abnormal codition is detected by the sync measurement module.
		R/W	[2]	0x0	When the scaler is not running, force the ouput data to black if this bit is 0 or to the background color if the bit is 1.
		R/W	[1]	0x0	If an abnormality is detected in the sync measurement module or if the maximum output vertical total has been reached, force the ouput data to black if this bit is 0 or to white if this bit is 1.
		R/W	[0]	0x0	During blanking, force output data to black if this bit is 0 or to the background color if this bit is 1.
SCL_AVERAGE_IK	0x0AF0		[7:3]		Reserved
		R/W	[2:1]	0x0	0x0: bypass 0x1: horizontal average by 2 0x2: horizontal average by 4 0x3: horizontal average by 8
		R/W	[0]	0x0	0: no pixel average 1: enable pixel averager This function is only necessary if the input horizontal resolution is greater than 1280 pixels.
SCL_FLIP_H_IK	0x0AF1		[7:1]		Reserved
		R/W	[0]	0x0	horizontal flip enable

2.15 Output Sequencer Block

The output sequencer module provides timing for the output video interface. It allows sufficient flexibility to support a broad range of Smart Panel applications as well. The timing unit is based on horizontal and vertical counters, which are locked with the input video stream.

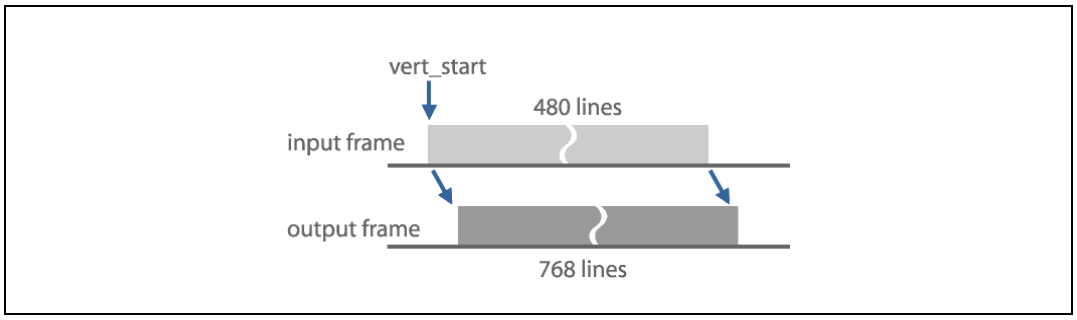
Figure 4: Output Sequencer Block Diagram



Frame Synchronization

Due to the limited pixel memory of the chip, the output active video needs to be perfectly synchronized with the input active video. This mode of operation is called *Frame Lock*.

Figure 5: Frame Lock Operation



Timing Unit

The timing unit consists of a 12-bit horizontal and a 12-bit vertical counter, synchronized with the input video stream.

Signal Generation

The signal generation unit generates all fixed control signals like hsync, vsync and data enable as well as those required to run the internal data path. Also included, a generalized timing section supports flat panel TCON signals like polarity and other control signals.

Table 19: Output Sequencer Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
OSQ_CONTROL	0x0BC1	R	[7]		out_vmax detected, sticky bit
		R/W	[6]	0x0	out_vmax detect reset
		R/W	[5]	0x0	interlace enable
		R/W	[4]	0x0	fractional line extend 0: +1 1: +2
		R/W	[3]	0x0	frame lock reference 0: last input pixel 1: first input pixel
		R/W	[2]	0x0	frame lock selection 0: last line variable 1: fixed line length
		R	[1]		shutdown ready - current frame has completed, panel can now be shut down
		R/W	[0]	0x0	run sequencer when 1, otherwise stop at the end of the frame and set shutdown ready flag (bit [1])
OSQ_CLOCK_FRAC	0x0BC2	R/W	[7:0]	0x0	the fraction of lines (/256) that are extended
OSQ_OUT_HTOTAL_L	0x0BC3	R/W	[7:0]	0x0	nominal output horizontal total [7:0]
OSQ_OUT_HTOTAL_H	0x0BC4		[7:4]		Reserved
		R/W	[3:0]	0x0	nominal output horizontal total [11:8]
OSQ_OUT_VTOTAL_MIN_L	0x0BC5	R/W	[7:0]	0x0	minimum output vertical total, used to rearm for vert_enab trigger [7:0]
OSQ_OUT_VTOTAL_MIN_H	0x0BC6		[7:4]		Reserved
		R/W	[3:0]	0x0	minimum output vertical total, used to rearm for vert_enab triggers [11:8]
OSQ_VTOTAL_MAX_L	0x0BC7	R/W	[7:0]	0x0	maximum output vertical total, prevents panel burn with loss of vert_enab trigger [7:0]
OSQ_VTOTAL_MAX_H	0x0BC8		[7:4]		Reserved
		R/W	[3:0]	0x0	maximum output vertical total, prevents panel burn with loss of vert_enab triggers [11:8]
OSQ_VERTEN_DLY_E_L	0x0BC9	R/W	[7:0]	0x0	delay of the vert_enab signal to the reset of the horizontal and vertical counters, even and non-interlaced modes [15:0]
OSQ_VERTEN_DLY_E_M	0x0BCA	R/W	[7:0]	0x0	
OSQ_VERTEN_DLY_E_H	0x0BCB		[7:4]		Reserved
		R/W	[3:0]	0x0	delay of the vert_enab signal to the reset of the horizontal and vertical counters, even and non-interlaced [19:16]
OSQ_VERTEN_DLY_O_L	0x0BCC	R/W	[7:0]	0x0	delay of the vert_enab signal to the reset of the horizontal and vertical counters, odd frame in interlace mode only [15:0]
OSQ_VERTEN_DLY_O_M	0x0BCD	R/W	[7:0]	0x0	

Table 19: Output Sequencer Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
OSQ_VERTEN_DLY_O_H	0x0BCE		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	delay of the vert_enab signal to the reset of the horizontal and vertical counters, odd frame in interlace mode only [19:16]
OSQ_VSYNC_SET_L	0x0BCF	R/W	[7:0]	0x0	vertical count at which vsync goes high [7:0]
OSQ_VSYNC_SET_H	0x0BD0		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	vertical count at which vsync goes high [11:8]
OSQ_VSYNC_RST_L	0x0BD1	R/W	[7:0]	0x0	vertical count at which vsync goes low [7:0]
OSQ_VSYNC_RST_H	0x0BD2		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	vertical count at which vsync goes low [11:8]
OSQ_HSYNC_SET_L	0x0BD3	R/W	[7:0]	0x0	horizontal count at which hsync goes high [7:0]
OSQ_HSYNC_SET_H	0x0BD4		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	horizontal count at which hsync goes high [11:8]
OSQ_HSYNC_RST_L	0x0BD5	R/W	[7:0]	0x0	horizontal count at which hsync goes low [7:0]
OSQ_HSYNC_RST_H	0x0BD6		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	horizontal count at which hsync goes low [11:8]
OSQ_HENAB_SET_L	0x0BD7	R/W	[7:0]	0x0	horizontal count at which enab goes high [7:0]
OSQ_HENAB_SET_H	0x0BD8		[7:4]		Reserved
		R/W	[3:0]		horizontal count at which enab goes high [11:8] value must be greater than 0x01C
OSQ_HENAB_RST_L	0x0BD9	R/W	[7:0]	0x0	horizontal count at which enab goes low [7:0]
OSQ_HENAB_RST_H	0x0BDA		[7:4]		Reserved
		R/W	[3:0]		horizontal count at which enab goes low [11:8]
OSQ_VENAB_SET_L	0x0BDB	R/W	[7:0]	0x0	vertical count at which enab goes high [7:0]
OSQ_VENAB_SET_H	0x0BDC		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	vertical count at which enab goes high [11:8]
OSQ_VENAB_RST_L	0x0BDD	R/W	[7:0]	0x0	vertical count at which enab goes low [7:0]
OSQ_VENAB_RST_H	0x0BDE		[7:4]	0x0	Reserved
		R/W	[3:0]	0x0	vertical count at which enab goes low [11:8]
OSQ_OUT_VCOUNT	0x0BDF	R	[7:0]	0x0	vertical counter /16 indicating the current frame position

2.16 Timing Controller (TCON) Block

The Output Timing Controller module provides timing for Smart Panel applications. The timing unit is based on horizontal and vertical counters locked with the output video stream. A set of programmable comparators provides all necessary time events to generate signals for the driver interface.

Please refer to the programming tools for more details.

Figure 6: TCON Block Diagram

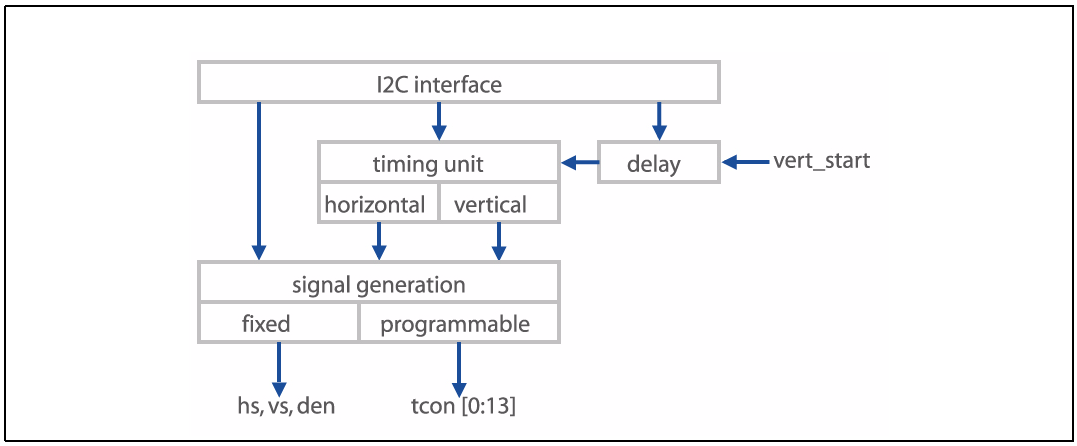


Table 20: TCON Registers (Sheet 1 of 6)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_CONTROL	0x0BC0		[7:3]		Reserved
		R/W	[2]	0	0: no TCON pipe delay matching 1: TCON pipe delay enabled (normal)
		R/W	[1]	0	initialize SRTDs
		R/W	[0]	0	enableTCON
TCON_COMP_0_L	0x0B10	R/W	[7:0]	0	count comparison value [7:0]
TCON_COMP_0_H	0x0B11	R/W	[7:5]		Reserved
		R/W	[4]		0: horizontal count compare 1: vertical count compare
		R/W	[3:0]		count comparison value [11:8]
TCON_COMP_1_L	0x0B12	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_1_H	0x0B13	R/W	[7:0]		
TCON_COMP_2_L	0x0B14	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_2_H	0x0B15	R/W	[7:0]		
TCON_COMP_3_L	0x0B16	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_3_H	0x0B17	R/W	[7:0]		
TCON_COMP_4_L	0x0B18	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_4_H	0x0B19	R/W	[7:0]		
TCON_COMP_5_L	0x0B1A	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_5_H	0x0B1B	R/W	[7:0]		
TCON_COMP_6_L	0x0B1C	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_6_H	0x0B1D	R/W	[7:0]		

Table 20: TCON Registers (Sheet 2 of 6)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_COMP_7_L	0x0B1E	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_7_H	0x0B1F	R/W	[7:0]		
TCON_COMP_8_L	0x0B20	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_8_H	0x0B21	R/W	[7:0]		
TCON_COMP_9_L	0x0B22	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_9_H	0x0B23	R/W	[7:0]		
TCON_COMP_10_L	0x0B24	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_10_H	0x0B25	R/W	[7:0]		
TCON_COMP_11_L	0x0B26	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_11_H	0x0B27	R/W	[7:0]		
TCON_COMP_12_L	0x0B28	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_12_H	0x0B29	R/W	[7:0]		
TCON_COMP_13_L	0x0B2A	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_13_H	0x0B2B	R/W	[7:0]		
TCON_COMP_14_L	0x0B2C	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_14_H	0x0B2D	R/W	[7:0]		
TCON_COMP_15_L	v0B2E	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_15_H	v0B2F	R/W	[7:0]		
TCON_COMP_16_L	0x0B30	R/W	[7:0]	0	refer to TCON_COMP_0 for definition
TCON_COMP_16_H	0x0B31	R/W	[7:0]		
TCON_COMP_17_L	0x0B32	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_17_H	0x0B33	R/W	[7:0]		
TCON_COMP_18_L	0x0B34	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_18_H	0x0B35	R/W	[7:0]		
TCON_COMP_19_L	0x0B36	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_19_H	0x0B37	R/W	[7:0]		
TCON_COMP_20_L	0x0B38	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_20_H	0x0B39	R/W	[7:0]		
TCON_COMP_21_L	0x0B3A	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_21_H	0x0B3B	R/W	[7:0]		
TCON_COMP_22_L	0x0B3C	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_22_H	0x0B3D	R/W	[7:0]		
TCON_COMP_23_L	0x0B3E	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_23_H	0x0B3F	R/W	[7:0]		
TCON_COMP_24_L	0x0B40	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_24_H	0x0B41	R/W	[7:0]		
TCON_COMP_25_L	0x0B42	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_25_H	0x0B43	R/W	[7:0]		

Table 20: TCON Registers (Sheet 3 of 6)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_COMP_26_L	0x0B44	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_26_H	0x0B45	R/W	[7:0]		
TCON_COMP_27_L	0x0B46	R/W	[7:0]	0x0	refer to TCON_COMP_0 for definition
TCON_COMP_27_H	0x0B47	R/W	[7:0]		
TCON_SRTD_0	0x0B50		[7:4]		Reserved
		R/W	[3]	0x0	SRTD initialization state
		R/W	[2:0]	0x0	0x0: f (A&B,&C&D,0,0) 0x1: f (A&B,&C&D,0,0) 0x2: f (A&B,&C&D,0,0) 0x3: f (0,0,A&B,0) 0x4: f (0,0,0,A&B) 0x5: f (0,0,0,A|B) 0x6: f (0,0,0,A^B) 0x7: f (0,0,0,!(A&B)) where f(Set, Reset, Toggle, Dflop) is a configurable logic/flop element
TCON_SRTD_1	0x0B51	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_2	0x0B52	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_3	0x0B53	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_4	0x0B54	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_5	0x0B55	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_6	0x0B56	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_7	0x0B57	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_8	0x0B58	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_9	0x0B59	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_10	0x0B5A	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_11	0x0B5B	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_12	0x0B5C	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_13	0x0B5D	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_14	0x0B5E	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_15	0x0B5F	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_16	0x0B60	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_17	0x0B61	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_18	0x0B62	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_19	0x0B63	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_20	0x0B64	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_21	0x0B65	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_22	0x0B66	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_23	0x0B67	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_24	0x0B68	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_25	0x0B69	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_26	0x0B6A	R/W	[7:0]		refer to TCON_srtd_0 for definition

Table 20: TCON Registers (Sheet 4 of 6)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_SRTD_27	0x0B6B	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_28	0x0B6C	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_29	0x0B6D	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_30	0x0B6E	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_SRTD_31	0x0B6F	R/W	[7:0]		refer to TCON_srtd_0 for definition
TCON_X_0	0x0B80		[7:6]		Reserved
		R/W	[5:0]	0x0	Input Selection for SRTD_0.A 0x00: 0 0x01: 1 0x02: external TCON input pin 0x03: I2C SRTD init bit 0x04 - 0x1F: comp0 - comp27 0x20 - 0x37: SRTD8 - SRTD31 0x38: 2 frame + 1 line + 2 pixel toggle 0x39: 2 frame + 2 line + 1 pixel toggle 0x3A: HCOUNT[0] 0x3B: HCOUNT[1] 0x3C: HCOUNT[0] 0x3D: HCOUNT[1] 0x3E: FCOUNT[0] 0x3F: FCOUNT[1]
TCON_X_1	0x0B81	R/W	[7:0]		Input Selection for SRTD_0.B[1]
TCON_X_2	0x0B82	R/W	[7:0]		Input Selection for SRTD_1.A[1]
TCON_X_3	0x0B83	R/W	[7:0]		Input Selection for SRTD_1.B[1]
TCON_X_4	0x0B84	R/W	[7:0]		Input Selection for SRTD_2.A[1]
TCON_X_5	0x0B85	R/W	[7:0]		Input Selection for SRTD_2.B[1]
TCON_X_6	0x0B86	R/W	[7:0]		Input Selection for SRTD_3.A[1]
TCON_X_7	0x0B87	R/W	[7:0]		Input Selection for SRTD_3.B[1]
TCON_X_8	0x0B88	R/W	[7:0]		Input Selection for SRTD_4.A[1]
TCON_X_9	0x0B89	R/W	[7:0]		Input Selection for SRTD_4.B[1]
TCON_X_10	0x0B8A	R/W	[7:0]		Input Selection for SRTD_5.A[1]
TCON_X_11	0x0B8B	R/W	[7:0]		Input Selection for SRTD_5.B[1]
TCON_X_12	0x0B8C	R/W	[7:0]		Input Selection for SRTD_6.A[1]
TCON_X_13	0x0B8D	R/W	[7:0]		Input Selection for SRTD_6.B[1]
TCON_X_14	0x0B8E	R/W	[7:0]		Input Selection for SRTD_7.[1]
TCON_X_15	0x0B8F	R/W	[7:0]		Input Selection for SRTD_7.B[1]
TCON_X_16	0x0B90	R/W	[7:0]		Input Selection for SRTD_8.[1]
TCON_X_17	0x0B91	R/W	[7:0]		Input Selection for SRTD_8.B[1]
TCON_X_18	0x0B92	R/W	[7:0]		Input Selection for SRTD_9.A[1]
TCON_X_19	0x0B93	R/W	[7:0]		Input Selection for SRTD_9.B[1]
TCON_X_20	0x0B94	R/W	[7:0]		Input Selection for SRTD_10.A[1]

Table 20: TCON Registers (Sheet 5 of 6)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_X_21	0x0B95	R/W	[7:0]		Input Selection for SRTD_10.B[1]
TCON_X_22	0x0B96	R/W	[7:0]		Input Selection for SRTD_11.A[1]
TCON_X_23	0x0B97	R/W	[7:0]		Input Selection for SRTD_11.B[1]
TCON_X_24	0x0B98	R/W	[7:0]		Input Selection for SRTD_12.A[1]
TCON_X_25	0x0B99	R/W	[7:0]		Input Selection for SRTD_12.B[1]
TCON_X_26	0x0B9A	R/W	[7:0]		Input Selection for SRTD_13.A[1]
TCON_X_27	0x0B9B	R/W	[7:0]		Input Selection for SRTD_13.B[1]
TCON_X_28	0x0B9C	R/W	[7:0]		Input Selection for SRTD_14.A[1]
TCON_X_29	0x0B9D	R/W	[7:0]		Input Selection for SRTD_14.B[1]
TCON_X_30	0x0B9E	R/W	[7:0]		Input Selection for SRTD_15.A[1]
TCON_X_31	0x0B9F	R/W	[7:0]		Input Selection for SRTD_15.B[1]
TCON_X_32	0x0BA0	R/W	[7:0]		Input Selection for SRTD_16.A[1]
TCON_X_33	0x0BA1	R/W	[7:0]		Input Selection for SRTD_16.B[1]
TCON_X_34	0x0BA2	R/W	[7:0]		Input Selection for SRTD_17.A[1]
TCON_X_35	0x0BA3	R/W	[7:0]		Input Selection for SRTD_17.B[1]
TCON_X_36	0x0BA4	R/W	[7:0]		Input Selection for SRTD_18.A[1]
TCON_X_37	0x0BA5	R/W	[7:0]		Input Selection for SRTD_18.B[1]
TCON_X_38	0x0BA6	R/W	[7:0]		Input Selection for SRTD_19.A[1]
TCON_X_39	0x0BA7	R/W	[7:0]		Input Selection for SRTD_19.B[1]
TCON_X_40	0x0BA8	R/W	[7:0]		Input Selection for SRTD_20.A[1]
TCON_X_41	0x0BA9	R/W	[7:0]		Input Selection for SRTD_20.B[1]
TCON_X_42	0x0BAA	R/W	[7:0]		Input Selection for SRTD_21.A[1]
TCON_X_43	0x0BAB	R/W	[7:0]		Input Selection for SRTD_21.B[1]
TCON_X_44	0x0BAC	R/W	[7:0]		Input Selection for SRTD_22.A[1]
TCON_X_45	0x0BAD	R/W	[7:0]		Input Selection for SRTD_22.B[1]
TCON_X_46	0x0BAE	R/W	[7:0]		Input Selection for SRTD_23.A[1]
TCON_X_47	0x0BAF	R/W	[7:0]		Input Selection for SRTD_23.B[1]
TCON_X_48	0x0BB0	R/W	[7:0]		Input Selection for SRTD_24.A[1]
TCON_X_49	0x0BB1	R/W	[7:0]		Input Selection for SRTD_24.B[1]
TCON_X_50	0x0BB2	R/W	[7:0]		Input Selection for SRTD_25.A[1]
TCON_X_51	0x0BB3	R/W	[7:0]		Input Selection for SRTD_25.B[1]
TCON_X_52	0x0BB4	R/W	[7:0]		Input Selection for SRTD_26.A[1]
TCON_X_53	0x0BB5	R/W	[7:0]		Input Selection for SRTD_26.B[1]
TCON_X_54	0x0BB6	R/W	[7:0]		Input Selection for SRTD_27.A[1]

Table 20: TCON Registers (Sheet 6 of 6)

Register Name	Addr.	Mode	Bits	Default	Description
TCON_X_55	0x0BB7	R/W	[7:0]		Input Selection for SRTD_27.B[1]
TCON_X_56	0x0BB8	R/W	[7:0]		Input Selection for SRTD_28.A[1]
TCON_X_57	0x0BB9	R/W	[7:0]		Input Selection for SRTD_28.B[1]
TCON_X_58	0x0BBA	R/W	[7:0]		Input Selection for SRTD_29.A[1]
TCON_X_59	0x0BBB	R/W	[7:0]		Input Selection for SRTD_29.B[1]
TCON_X_60	0x0BBC	R/W	[7:0]		Input Selection for SRTD_30.A[1]
TCON_X_61	0x0BBD	R/W	[7:0]		Input Selection for SRTD_30.B[1]
TCON_X_62	0x0BBE	R/W	[7:0]		Input Selection for SRTD_31.A[1]
TCON_X_63	0x0BBF	R/W	[7:0]		Input Selection for SRTD_31.B[1]

1. Refer to register TCON_X_O for definition.

2.17 Pattern Generator Block

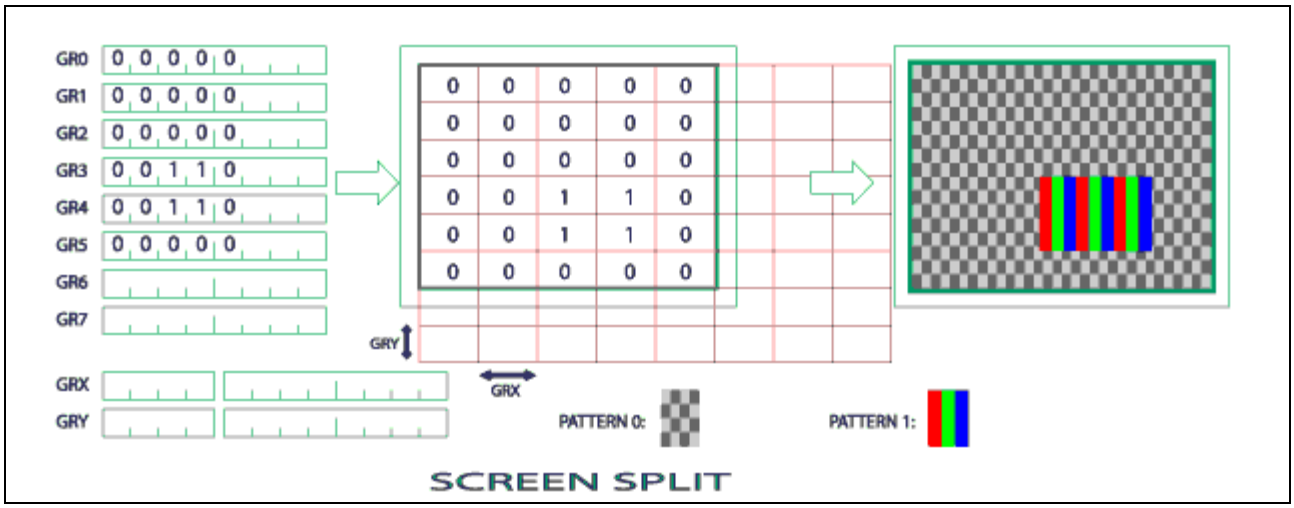
The integrated Pattern Generator displays a set of graphic patterns to help debugging systems and test LCD panels. It is located ahead of the color management block, all generated colors are subject to further transforms.

The screen can be split into a programmable grid of up to 8x8 areas. One of two independent programmable patterns are displayed in each area.

Screen Split

A set of eight Grid registers *grid0 - grid7,* each with 8 bits, represents a block map of the grid (8x8 blocks). Each bit from the Grid registers represents one rectangular (gridX)x(gridY) block of pixels which covers the LCD screen display area. Within these registers, a 0 selects Pattern 0 (defined below) and a 1 selects Pattern 1.

Figure 7: Pattern Generator: Screen Split



All cells are the same size, defined by one horizontal and one vertical grid block size registers *gridX and gridY.*

When the programmed block size corresponds to a larger 8x8 grid than the total screen area, only the blocks or part of blocks included in the output screen space are rendered. The 8x8 block set is upper left justified. All blocks from the right and bottom sides which are outside the total display area are not rendered.

When the programmed block size corresponds to a smaller 8x8 grid than the total screen area, the part of the screen area which is outside the 8x8 grid is forced to black.

Pattern Engine

The pattern generator has two pattern display engines to display two patterns simultaneously on the LCD screen. Each engine displays horizontal or vertical bicolor stripes, bicolor checkers, color bars, gray scales or color scales. It is also possible to select the video stream from the scaler as a pattern.

The pattern engine displays a bi-directional x-y symmetric pattern. Two 24b colors, C0 and C1, are alternately displayed with a horizontal period of Width and vertical period of Height. Programming a large Width and a small Height generates horizontal bars whereas the opposite generates vertical bars. Programming small numbers for Width and Height generates checker patterns.

Both patterns are also given X and Y offset attributes, they can be centered inside the grid blocks.

A gradient effect can be applied independently on each pattern, to either or both horizontal and vertical directions. The gradient effect takes two parameters: STEP and DELTA that define a ramp.

Borders

The border generator adds a single pixel width border to the whole display area. Each side color of the display is selectable among 8 independent colors.

Table 21: PGEN Registers (Sheet 1 of 4)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_PGEN_ENAB	0x0600		[7:1]		Reserved
		R/W	[0]	0x0	0 = disable PGEN block 1 = enable PGEN block
PGEN_GRID0	0x0601	R/W	[7:0]	0x0	Grid Row 0
PGEN_GRID1	0x0602	R/W	[7:0]	0x0	Grid Row 1
PGEN_GRID2	0x0603	R/W	[7:0]	0x0	Grid Row 2
PGEN_GRID3	0x0604	R/W	[7:0]	0x0	Grid Row 3
PGEN_GRID4	0x0605	R/W	[7:0]	0x0	Grid Row 4
PGEN_GRID5	0x0606	R/W	[7:0]	0x0	Grid Row 5
PGEN_GRID6	0x0607	R/W	[7:0]	0x0	Grid Row 6
PGEN_GRID7	0x0608	R/W	[7:0]	0x0	Grid Row 7
PGEN_GRID_X_L	0x0609	R/W	[7:0]	0x0	width of a grid block in pixels [7:0]
PGEN_GRID_X_H	0x060A		[7:4]		Reserved
		R/W	[3:0]	0x0	width of a grid block in pixels [11:8]
PGEN_GRID_Y_L	0x060B	R/W	[7:0]	0x0	height of a grid block in pixels [7:0]
PGEN_GRID_Y_H	0x060C		[7:4]		Reserved
		R/W	[3:0]	0x0	height of a grid block in pixels [11:8]
PGEN_GRID_X_OFFSET_X_L	0x060D	R/W	[7:0]	0x0	grid block horizontal offset in pixels [7:0]
PGEN_GRID_X_OFFSET_X_H	0x060E		[7:4]		Reserved
		R/W	[3:0]	0x0	grid block horizontal offset in pixels [11:8]
PGEN_GRID_Y_OFFSET_Y_L	0x060F	R/W	[7:4]	0x0	grid block vertical offset in pixels
PGEN_GRID_Y_OFFSET_Y_H	0x0610	R/W	[3:0]		

Table 21: PGEN Registers (Sheet 2 of 4)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_P0_MODE	0x0611	R/W			pattern 0 control
		R/W	[7:5]	0x0	number of bars in C0
		R/W	[4:2]	0x0	number of bars in C1
		R/W	[1]	0x0	0: pattern continues to progress across block boundaries 1: block boundaries cause the pattern to restart
		R/W	[0]	0x0	0: normal mode 1: C0 = video bypass
PGEN_P1_MODE	0x0612				pattern 1 control
		R/W	[7:5]	0x0	number of bars in C0
		R/W	[4:2]	0x0	number of bars in C1
		R/W	[1]	0x0	0: pattern continues to progress across block boundaries 1: block boundaries cause the pattern to restart
		R/W	[0]	0x0	0: normal mode 1: C0 = video bypass
PGEN_P0_WIDTH_X_L	0x0613	R/W	[7:0]	0x0	Pattern 0 Bar Width [7:0]
PGEN_P0_WIDTH_X_H	0x0614		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 0 Bar Width [11:8]
PGEN_P0_WIDTH_X_OFFSET_L	0x0615	R/W	[7:0]	0x0	Pattern 0 Horizontal Offset [7:0]
PGEN_P0_WIDTH_X_OFFSET_H	0x0616		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 0 Horizontal Offset [11:8]
PGEN_P0_HEIGHT_Y_L	0x0617	R/W	[7:0]	0x0	Pattern 0 Bar Height [7:0]
PGEN_P0_HEIGHT_Y_H	0x0618	R/W	[7:4]	0x0	Pattern 0 Vertical Sequence Increment
		R/W	[3:0]	0x0	Pattern 0 Bar Height [11:8]
PGEN_P0_HEIGHT_Y_OFFSET_L	0x0619	R/W	[7:0]	0x0	Pattern 0 Vertical Offset [7:0]
PGEN_P0_HEIGHT_Y_OFFSET_H	0x061A		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 0 Vertical Offset [11:8]
PGEN_P1_WIDTH_X_L	0x061B	R/W	[7:0]	0x0	Pattern 1 Bar Width [7:0]
PGEN_P1_WIDTH_X_H	0x061C		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 1 Bar Width [11:8]
PGEN_P1_WIDTH_X_OFFSET_L	0x061D	R/W	[7:0]	0x0	Pattern 1 Horizontal Offset [7:0]
PGEN_P1_WIDTH_X_OFFSET_H	0x061E		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 1 Horizontal Offset [11:8]
PGEN_P1_HEIGHT_Y_L	0x061F	R/W	[7:0]	0x0	Pattern 1 Bar Height [7:0]
PGEN_P1_HEIGHT_Y_H	0x0620	R/W	[7:4]	0x0	Pattern 1 Vertical Sequence Increment
		R/W	[3:0]	0x0	Pattern 1 Bar Height [11:8]
PGEN_P1_HEIGHT_Y_OFFSET_L	0x0621	R/W	[7:0]	0x0	Pattern 1 Vertical Offset [7:0]
PGEN_P1_HEIGHT_Y_OFFSET_H	0x0622		[7:4]		Reserved
		R/W	[3:0]	0x0	Pattern 1 Vertical Offset [11:8]
PGEN_P0_COLOR_R_C0	0x0623	R/W	[7:0]	0x0	Pattern 0 Color C0 - Red
PGEN_P0_COLOR_G_C0	0x0624	R/W	[7:0]	0x0	Pattern 0 Color C0 - Green
PGEN_P0_COLOR_B_C0	0x0625	R/W	[7:0]	0x0	Pattern 0 Color C0 - Blue
PGEN_P0_COLOR_R_C1	0x0626	R/W	[7:0]	0x0	Pattern 0 Color C1 - Red
PGEN_P0_COLOR_G_C1	0x0627	R/W	[7:0]	0x0	Pattern 0 Color C1 - Green

Table 21: PGEN Registers (Sheet 3 of 4)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_P0_COLOR_B_C1	0x0628	R/W	[7:0]	0x0	Pattern 0 Color C1 - Blue
PGEN_P1_COLOR_R_C0	0x0629	R/W	[7:0]	0x0	Pattern 1 Color C0 - Red
PGEN_P1_COLOR_G_C0	0x062A	R/W	[7:0]	0x0	Pattern 1 Color C0 - Green
PGEN_P1_COLOR_B_C0	0x062B	R/W	[7:0]	0x0	Pattern 1 Color C0 - Blue
PGEN_P1_COLOR_R_C1	0x062C	R/W	[7:0]	0x0	Pattern 1 Color C1 - Red
PGEN_P1_COLOR_G_C1	0x062D	R/W	[7:0]	0x0	Pattern 1 Color C1 - Green
PGEN_P1_COLOR_B_C1	0x062E	R/W	[7:0]	0x0	Pattern 1 Color C1 - Blue
PGEN_P0_GRADDELTA_R	0x062F	R/W	[7:0]	0x0	Pattern 0 Gradient Delta on Red
PGEN_P0_GRADDELTA_G	0x0630	R/W	[7:0]	0x0	Pattern 0 Gradient Delta on Green
PGEN_P0_GRADDELTA_B	0x0631	R/W	[7:0]	0x0	Pattern 0 Gradient Delta on Blue
PGEN_P0_GRADSTEP_X	0x0632	R/W	[7:0]	0x0	Pattern 0 Gradient Horizontal Step
PGEN_P0_GRADSTEP_Y	0x0633	R/W	[7:0]	0x0	Pattern 0 Gradient Vertical Step
PGEN_P1_GRADDELTA_R	0x0634	R/W	[7:0]	0x0	Pattern 1 Gradient Delta on Red
PGEN_P1_GRADDELTA_G	0x0635	R/W	[7:0]	0x0	Pattern 1 Gradient Delta on Green
PGEN_P1_GRADDELTA_B	0x0636	R/W	[7:0]	0x0	Pattern 1 Gradient Delta on Blue
PGEN_P1_GRADSTEP_X	0x0637	R/W	[7:0]	0x0	Pattern 1 Gradient Horizontal Step
PGEN_P1_GRADSTEP_Y	0x0638	R/W	[7:0]	0x0	Pattern 1 Gradient Vertical Step
PGEN_P0_SEQ_COL0_COL1	0x0639		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 1 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Ba R0 Color
PGEN_P0_SEQ_COL2_COL3	0x063A		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 3 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Bar 2 Color
PGEN_P0_SEQ_COL4_COL5	0x063B		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 5 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Bar 4 Color
PGEN_P0_SEQ_COL6_COL7	0x063C		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 0 Bar 7 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 0 Bar 6 Color
PGEN_P1_SEQ_COL0_COL1	0x063D		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 1 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 0 Color
PGEN_P1_SEQ_COL2_COL3	0x063E		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 3 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 2 Color
PGEN_P1_SEQ_COL4_COL5	0x063F		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 5 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 4 Color

Table 21: PGEN Registers (Sheet 4 of 4)

Register Name	Addr	Mode	Bits	Default	Description
PGEN_P1_SEQ_COL6_COL7	0x0640		[7]		Reserved
		R/W	[6:4]	0x0	Pattern 1 Bar 7 Color
			[3]		Reserved
		R/W	[2:0]	0x0	Pattern 1 Bar 6 Color
PGEN_B_TOP_BOTTOM	0x0641	R/W	[7]	0x0	Top Border Enable
		R/W	[6]	0x0	Top Border Red; 0 = Off, 1= On
		R/W	[5]	0x0	Top Border Green; 0 = Off, 1= On
		R/W	[4]	0x0	Top Border Blue; 0 = Off, 1= On
		R/W	[3]	0x0	Bottom Border Enable
		R/W	[2]	0x0	Bottom Border Red; 0 = Off, 1= On
		R/W	[1]	0x0	Bottom Border Green; 0 = Off, 1= On
		R/W	[0]	0x0	Bottom Border Blue; 0 = Off, 1= On
PGEN_B_LEFT_RIGHT	0x0642	R/W	[7]	0x0	Left Border Enable
		R/W	[6]	0x0	Left Border Red; 0 = Off, 1= On
		R/W	[5]	0x0	Left Border Green; 0 = Off, 1= On
		R/W	[4]	0x0	Left Border Blue; 0 = Off, 1= On
		R/W	[3]	0x0	Right Border Enable
		R/W	[2]	0x0	Right Border Red; 0 = Off, 1= On
		R/W	[1]	0x0	Right Border Green; 0 = Off, 1= On
		R/W	[0]	0x0	Right Border Blue; 0 = Off, 1= On
PGEN_X_TOTAL_L	0x0643	R/W	[7:0]	0x0	Total Horizontal Size [7:0]
PGEN_X_TOTAL_H	0x0644		[7:4]		Reserved
		R/W	[3:0]	0x0	Total Horizontal Size [11:8]
PGEN_Y_TOTAL_L	0x0645	R/W	[7:0]	0x0	Total Vertical Size [7:0]
PGEN_Y_TOTAL_H	0x0646		[7:4]		Reserved
		R/W	[3:0]	0x0	Total Vertical Size [11:8]

2.18 SRGB Block

The sRGB block performs two primary functions:

1. Parametric gamma correction on multiple windows or full screen for video enhancement in a window and digital contrast/brightness control. The window coordinates are set by TCON registers.
2. 3D color cube warping RGB color space.

2.18.1 Parametric Gamma Correction and Digital Contrast/Brightness Control

The function is applied to the entire window by programming the window control to full screen. Each color channel acts independently. Simple digital contrast and brightness are programmable with this hardware function. The desired window coordinates are programmed into the TCON.

2.18.2 Color Space Warp

The 8 corners of the color cube are independently controlled in 3D space with smooth interpolation of intermediate colors. Registers are 2's complement color delta's. For example, to make WHITE more like RED, program SRGB_WHITE_R to a small positive value.

Figure 8: Color Space Warp

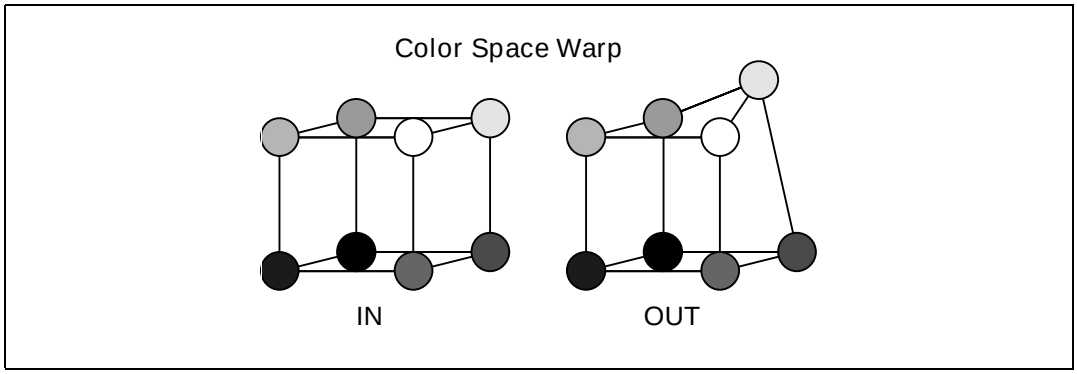


Table 22: SRGB Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SRGB_CTRL	0x0D00	R/W	[7:6]	0x0	Reserved
		R/W	[5:4]	0x0	GAMMA_B Control 0x0: Disable 0x1: Full Screen 0x2: Windowed 0x3: Reserved
		R/W	[3:2]	0x0	GAMMA_A Control 0x0: Disable 0x1: Full Screen 0x2: Windowed 0x3: Reserved
		R/W	[1:0]	0x0	SRGB Control 0x0: Disabled 0x1: Full Screen 0x2: Windowed 0x3: Reserved
SRGB_BLACK_R	0x0D01	R/W	[7:0]	0x0	Black Point Red Delta
SRGB_BLACK_G	0x0D02	R/W	[7:0]	0x0	Black Point Green Delta
SRGB_BLACK_B	0x0D03	R/W	[7:0]	0x0	Black Point Blue Delta
SRGB_RED_R	0x0D04	R/W	[7:0]	0x0	Red Point Red Delta
SRGB_RED_G	0x0D05	R/W	[7:0]	0x0	Red Point Green Delta
SRGB_RED_B	0x0D06	R/W	[7:0]	0x0	Red Point Blue Delta
SRGB_GREEN_R	0x0D07	R/W	[7:0]	0x0	Green Point Red Delta
SRGB_GREEN_G	0x0D08	R/W	[7:0]	0x0	Green Point Green Delta
SRGB_GREEN_B	0x0D09	R/W	[7:0]	0x0	Green Point Blue Delta
SRGB_BLUE_R	0x0D0A	R/W	[7:0]	0x0	Blue Point Red Delta
SRGB_BLUE_G	0x0D0B	R/W	[7:0]	0x0	Blue Point Green Delta
SRGB_BLUE_B	0x0D0C	R/W	[7:0]	0x0	Blue Point Blue Delta
SRGB_YELLOW_R	0x0D0D	R/W	[7:0]	0x0	Yellow Point Red Delta
SRGB_YELLOW_G	0x0D0E	R/W	[7:0]	0x0	Yellow Point Green Delta
SRGB_YELLOW_B	0x0D0F	R/W	[7:0]	0x0	Yellow Point Blue Delta
SRGB_CYAN_R	0x0D10	R/W	[7:0]	0x0	Cyan Point Red Delta

Table 22: SRGB Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
SRGB_CYAN_G	0x0D11	R/W	[7:0]	0x0	Cyan Point Green Delta
SRGB_CYAN_B	0x0D12	R/W	[7:0]	0x0	Cyan Point Blue Delta
SRGB_MAGENTA_R	0x0D13	R/W	[7:0]	0x0	Magenta Point Red Delta
SRGB_MAGENTA_G	0x0D14	R/W	[7:0]	0x0	Magenta Point Green Delta
SRGB_MAGENTA_B	0x0D15	R/W	[7:0]	0x0	Magenta Point Blue Delta
SRGB_WHITE_R	0x0D16	R/W	[7:0]	0x0	White Point Red Delta
SRGB_WHITE_G	0x0D17	R/W	[7:0]	0x0	White Point Green Delta
SRGB_WHITE_B	0x0D18	R/W	[7:0]	0x0	White Point Blue Delta
SRGB_GAMMA_A_RED_A	0x0D19	R/W	[7:0]	0x0	Parametric A Gamma A Red, Gamma
SRGB_GAMMA_A_RED_B	0x0D1A	R/W	[7:0]	0x0	Parametric A Gamma B Red, Contrast
SRGB_GAMMA_A_RED_C	0x0D1B	R/W	[7:0]	0x0	Parametric A Gamma C Red, Brightness
SRGB_GAMMA_A_GREEN_A	0x0D1C	R/W	[7:0]	0x0	Parametric A Gamma A Green, Gamma
SRGB_GAMMA_A_GREEN_B	0x0D1D	R/W	[7:0]	0x0	Parametric A Gamma B Green, Contrast
SRGB_GAMMA_A_GREEN_C	0x0D1E	R/W	[7:0]	0x0	Parametric A Gamma C Green, Brightness
SRGB_GAMMA_A_BLUE_A	0x0D1F	R/W	[7:0]	0x0	Parametric A Gamma A Blue, Gamma
SRGB_GAMMA_A_BLUE_B	0x0D20	R/W	[7:0]	0x0	Parametric A Gamma B Blue, Contrast
SRGB_GAMMA_A_BLUE_C	0x0D21	R/W	[7:0]	0x0	Parametric A Gamma C Blue, Brightness
SRGB_GAMMA_B_RED_A	0x0D22	R/W	[7:0]	0x0	Parametric B Gamma A Red, Gamma
SRGB_GAMMA_B_RED_B	0x0D23	R/W	[7:0]	0x0	Parametric Gamma B Red, Contrast
SRGB_GAMMA_B_RED_C	0x0D24	R/W	[7:0]	0x0	Parametric Gamma C Red, Brightness
SRGB_GAMMA_B_GREEN_A	0x0D25	R/W	[7:0]	0x0	Parametric Gamma A Green, Gamma
SRGB_GAMMA_B_GREEN_B	0x0D26	R/W	[7:0]	0x0	Parametric Gamma B Green, Contrast
SRGB_GAMMA_B_GREEN_C	0x0D27	R/W	[7:0]	0x0	Parametric Gamma C Green, Brightness
SRGB_GAMMA_B_BLUE_A	0x0D28	R/W	[7:0]	0x0	Parametric Gamma A Blue, Gamma
SRGB_GAMMA_B_BLUE_B	0x0D29	R/W	[7:0]	0x0	Parametric Gamma B Blue, Contrast
SRGB_GAMMA_B_BLUE_C	0x0D2A	R/W	[7:0]	0x0	Parametric Gamma C Blue, Brightness

2.19 OSD Block

Introduction

The integrated on-screen display (OSD) controller is a character-based overlay with a high level of features and over 100Kbyte of on-board dedicated RAM storage.

Features

- 15 row by 30 column character-mapped display
- Four user-definable windows
- 12x18-pixel characters with optional horizontal and vertical doubling on a row-by-row basis
- Two 16-entry 24-bit RGB user-definable color maps
- 192 RAM-based monochrome 1bpp characters
- 64 RAM-based graphics 4bpp characters
- Text character attributes: foreground/background color, blinking

- Graphics character attributes: per-pixel color, vertical/horizontal mirroring
- Row attributes: double width, double height
- Window attributes: window visibility, position, size, border shadow, color table
- Global attributes: OSD visibility, OSD screen position, alpha fade in/fade out, global size doubling, rotation in ninety-degree increments
- Single-bit enable/disable

For information on OSD programming, see the OSD Programming Manual.

OSD Access via I2C

The OSD uses a dedicated memory space accessible through an I2C port. The data stream sent to the OSD register starts with two header bytes. These specify the type of transfer and the row/column position for screen map transfers, the character index for font definition transfers, or the color index for color map transfers.

A stream of OSD writes to the OSD I2C register can fill in a segment of the OSD memory space with an internal auto-incrementing index register. The protocol is as follows:

1. Issue a start sequence with the R/W bit set to W.
2. Write to the OSD register. The first byte transferred is the index of the first internal OSD register to be written. The next byte contains the data to be written to that register. Subsequent bytes are written to successive internal OSD registers.
3. Continue writing data bytes until the desired range of OSD internal registers has been written (the ADE3XXX device will issue an ACK on each transfer).
4. Issue an I2C stop sequence.

Character Display

There are two 96-character monochrome fonts and two 32-character four-bit color fonts, a total of 256 characters. The four bits of color are an index into one of two 16 entry color look-up tables. Entries in the color look-up table specify a 24-bit RGB color. All fonts and the color look-up table are RAM-based and must be downloaded to the OSD's internal RAM before use. Font addressing is as follows: character indexes 0x00-0x1F refer to color font 0, 0x20-0x7F refer to monochrome font 0, 0x80-0x9F refer to color font 1 and 0xA0-0xFF refer to monochrome font 1.

Screen Map

The OSD uses a character map of 15 rows x 30 columns. Each character occupies one byte. The value of each byte indicates the character to display.

The OSD character map is addressed by specifying the row and column as part of the data transfer.

Attribute Map

The attribute map is defined as 16 rows by 31 columns. It has an extra row and an extra column compared to the screen map.

The values corresponding to printable row/column addresses provide character attributes. Each character on the screen has an attribute byte specifying (in the case of monochrome fonts) three bits of background color, four bits of foreground color, and a blink on/off bit.

Blinking, when enabled, has a period of 100 frames (50 frames on, 50 frames off).

Column 31 of each row contains row attributes. These include the fourth bit of the background color and two bits controlling double-height and double-width text.

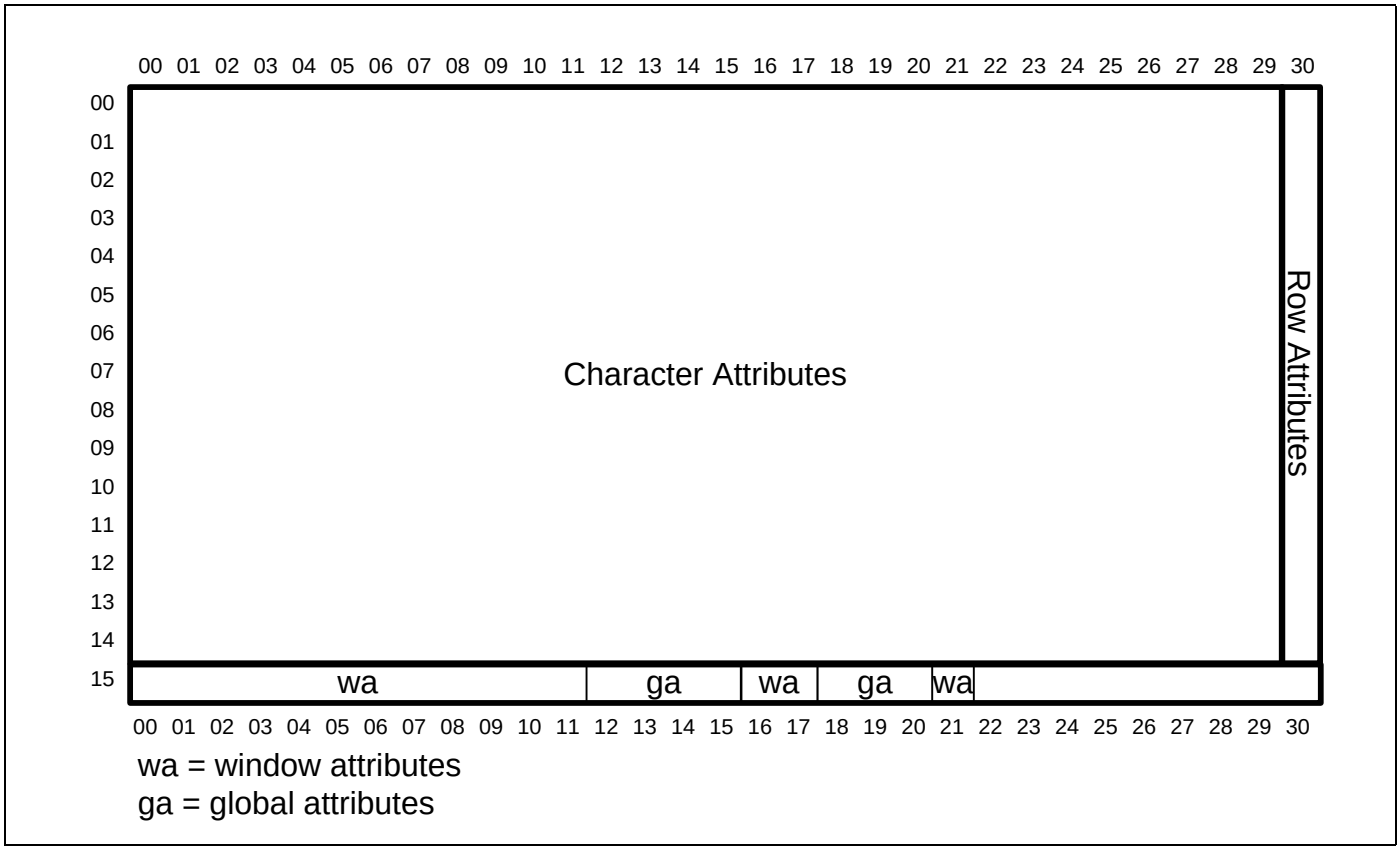
Row 15 contains global attributes, including vertical and horizontal OSD position on the screen, alpha blending, shadow/bordering, OSD rotation, color map selection, and normal/double size. Alpha blending allows the OSD display to be mixed with the incoming video signal for transparency

effects. An alpha value of 255 makes the OSD opaque, while a value of 0 makes the OSD invisible, with a linear ramp of transparency between these two endpoints. Separate registers control alpha for foreground and background pixels.

A fade-in/fade-out feature ramps the alpha values every six frames, starting from their current value and going up or down the sequence: 0, 16, 32, 64, 128, 192, 224, 240, 255.

Row 15 also contains definitions for the four display windows. These windows define regions on the screen to which borders and shadows can be applied. (They are not analogous to windows in a GUI display, in that they do not represent four independent data displays. There is only one character map. The windows essentially define an area around which a border can be drawn or to which attributes can be assigned.) Windows also determine which of the two color tables will be used for the characters inside. Windows have a fixed precedence: window 0 has the highest precedence and window 3 the lowest. When windows overlap, the precedence determines which borders will be displayed and which color tables will be used in the overlapping area.

Figure 9: Character Attribute Map



Monochrome and color fonts are affected differently by attribute bytes. Monochrome characters are affected by shadows and borders, and have their color specified by the foreground/background attributes. Color characters interpret the attribute byte differently than monochrome characters, using it to define blinking and 90-degree rotations rather than blinking, foreground color, and background color.

Color Tables

There are two color tables, each containing sixteen entries by three bytes each, giving a 24-bit RGB value for each entry. Entry 0 is used for the shadow color for monochrome characters and borders. Color-table selection is made on a window-by-window basis.

When writing the color table, the “row” value in the first header byte is interpreted as the color table index, while the “column” value in the second header byte encoded to select the color table (0 or 1)

and the primary color (red, green, or blue). The data byte following the second header byte is written to the selected (table, index, primary) location.

Font Data

Font data is sent to the OSD through burst transfers. The first header byte selects the transfer type and provides three bits of the character index, while the second header byte selects transfer type “C” and gives the remaining five bits of offset. The data bytes for the character follow, given from top to bottom and left to right in the character cell.

A monochrome character is 27 bytes long, with two scan-lines occupying three bytes. A color character is four times as long as a monochrome character (108 bytes), with each byte containing two four-bit pixels. Both color and monochrome fonts are 12 pixels wide and 18 high.

Transfer Formats

The transfer format consists of two header bytes and a variable number of data bytes. The header bytes determine the type of transfer (character, attribute, monochrome font, color font, or color table). Addressing is by row and column in the case of character or attribute transfers, and by character index in the case of font transfers.

When writing to the color table, the “column” field determines the color table and R/G/B selection.

Table 23: OSD Access Header Definition

Header Byte	Bits	Description
First	[7:4]	Type of data transfer. Valid values are: 0x8: screen map 0x9: color LUT 0xA: attribute map 0xC: font data all others: Reserved
	[3:0]	For screen map or attribute map access, this is the row index. For color LUT access, this is the color index. For font data access, bits [2:0] are the MSB’s of the character index.
Second	[7:6]	Type of data burst: 0x0: A/B modes: Only one data byte follows this header byte. 0x1: C mode: All bytes following this header byte are data bytes until the serial interface indicates an end-of-transmission. The OSD internally auto-increments after each byte. In screen and attribute map access modes the column number is incremented after each byte, wrapping to the beginning of the next row once column 29 is passed and wrapping to row 0 if row 14 is passed. Either mode may be used for display and character attribute modes, except for the off-screen attributes in column 15 and row 30, which must use mode A/B. Font definition mode must use mode C.
	[5]	must be set to zero
	[4:0]	In screen and attribute map access modes, this is the column number. In font data access mode, this gives the 5 lsb’s of the character index. In color LUT access mode, it selects the table number and color to be written: 0x0: LUT 0, red 0x1: LUT 0, green 0x2: LUT 0, blue 0x3: LUT 1, red 0x4: LUT 1, green 0x5: LUT 1, blue 0x6 - 0x7: Reserved

Table 24: OSD Attribute Map Definition (Sheet 1 of 2)

Row	Column	Bits	Description
15	12	[7:0]	vertical OSD position / 4
15	13	[7:0]	horizontal OSD position / 5
15	15	[7]	0: OSD off 1: OSD on
		[6:5]	0x0: Plain Characters 0x1: Border Characters 0x2: Shadow Characters 0x3: Reserved
		[4:3]	Reserved
		[2]	0: normal 1: flip OSD
		[1]	0: Fade Off 1: Fade On
		[0]	0: Normal Size 1: Double Size
15	19	[7:0]	Foreground Alpha Blending
15	20	[7:0]	Background Alpha Blending
15	0	[7:4]	Window 0 Row Start
		[3:0]	Window 0 Row End
15	3	[7:4]	Window 1 Row Start
		[3:0]	Window 1 Row End
15	6	[7:4]	Window 2 Row Start
		[3:0]	Window 2 Row End
15	9	[7:4]	Window 3 Row Start
		[3:0]	Window 3 Row End
15	1	[7:3]	Window 0 Column Start
		[2]	Window 0 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 0 Shadow Enable
15	4	[7:3]	Window 1 Column Start
		[2]	Window 1 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 1 Shadow Enable
15	7	[7:3]	Window 2 Column Start
		[2]	Window 2 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 2 Shadow Enable

Table 24: OSD Attribute Map Definition (Sheet 2 of 2)

Row	Column	Bits	Description
15	10	[7:3]	Window 3 Column Start
		[2]	Window 3 Visibility 0: Off 1: On
		[1]	Reserved
		[0]	Window 3 Shadow Enable
15	2	[7:3]	Window 0 Column End
		[2:0]	Reserved
15	5	[7:3]	Window 1 Column End
		[2:0]	Reserved
15	8	[7:3]	Window 2 Column End
		[2:0]	Reserved
15	11	[7:3]	Window 3 Column End
		[2:0]	Reserved
15	16	[7:6]	Window 3 Shadow Width
		[5:4]	Window 2 Shadow Width
		[3:2]	Window 1 Shadow Width
		[1:0]	Window 0 Shadow Width
15	17	[7:6]	Window 3 Shadow Height
		[5:4]	Window 2 Shadow Height
		[3:2]	Window 1 Shadow Height
		[1:0]	Window 0 Shadow Height
15	21	[7:4]	Reserved
		[3]	Window 3 Color LUT Select
		[2]	Window 2 Color LUT Select
		[1]	Window 1 Color LUT Select
		[0]	Window 0 Color LUT Select
0 to 14	30	[7:3]	Reserved
		[2]	MSB of Background Color for the Row
		[1]	Double High Enable for the Row
		[0]	Double Wide Enable for the Row
0 to 14	0 to 29	[7:5]	3 LSBs of Background Color for 1bpp Chars No Function for 4bpp Color Chars
		[4]	Blink Enable
		[3:0]	Foreground Color For 1bpp Chars For 4bpp Color Chars [3:2]: Reserved [1]: Flip Vertical [0]: Flip Horizontal

Table 25: OSD Register

Register Name	Addr	Mode	Bits	Default	Description
OSD_PORT	0C02	R/W	[7:0]	0	OSD access port

2.20 Flicker Block

The Flicker block computes correlations of the image data with potential inversion patterns of the LCD which in turn allows the microcontroller to modify the polarity signal to cancel large area flicker. This function is only useful in SmartPanel applications.

The incoming image is scored against 8 vertical Walsh functions. All patterns are considered to be vertically, where horizontally the pixels are assumed to be alternating its RGB components.

The scores (0 to 7) are 32-bit unsigned quantities that reflect the correlation of the programmed window area with the 8 Walsh functions.

The horizontal inversion of the LCD drivers must be programmed into FLICKER_CTRL0[2:0]. The most common setting is +-+ or -+- (RGB).

A calculation is completed after the number of frames programmed into the FRAME_CNT_MAX reg (0xCA03). With each frame, the calculation is performed on only a vertical strip. The width of that strip (in pixels) is determined by the value programmed in the HBLOCK_SIZE reg (0xCA02) with the following relation: strip width = 2 ^ (3 + HBLOCK_SIZE).

The FREE_RUN/FREEZE_SCORES bit (FLICKER_CTRL0[4]) enables the final calculation to be captured easily by the microntroller. The internal flicker calculation continues to run -- only the update of the I2C registers is blocked when this bit is set to prevent corrupution during readout.

Table 26: Flicker Registers (Sheet 1 of 3)

Register Name	Addr	Mode	Bits	Default	Description
FLK_CTRL	0x0CA1	R/W	[7:6]	0x0	Reserved
		W	[5]	0x1	0: straight line uniform function 1: straight line hill function (normal)
		R/W	[4]	0x0	0: free run 1: freeze scores Set to a 1 when the microcontroller is reading multibyte scores to prevent update corruption.
		R/W	[2:0]	0x25	Horizontal Subpixel Polarity Inversion Pattern of LCD (even/odd pixels) 0x0: -R-G-B / +R+G+B 0x1: -R-G+B / +R+G-B 0x2: -R+G-B / +R-G+B (normal) 0x3: -R+G+B / +R-G-B 0x4: +R-G-B / -R+G+B 0x5: +R-G+B / -R+G-B (normal) 0x6: +R+G-B / -R-G+B 0x7: +R+G+B / -R-G-B
FLK_HBLOCK_SIZE	0x0CA2	R/W	[7:4]		Reserved
			[3:0]	0x0	Width in pixels of the per frame scored area = 2 ^ (3+ HBLOCK_SIZE)

Table 26: Flicker Registers (Sheet 2 of 3)

Register Name	Addr	Mode	Bits	Default	Description
FLK_FRAME_CNT_MAX	0x0CA3	R/W	[7:0]	0x8	Number of Frames to complete one measurement total number of pixels in a line is: FRAME_CNT_MAX x (2 ^ (3 + HBLOCK_SIZE)) example: HBLOCK_SIZE = 4; FRAME_CNT_MAX = 8; In each frame only one portion of the image is being scored. The width of that portion is 2 ^ (3 + HBLOCK_SIZE) = 128 pixels and the height is the full height of the image. Thus the total scored area after 8 frames is 128 x 8 = 1024 pixels wide.
FLK_MEAS0_0	0x0CB1	R/W	[7:0]	0x0	Score for Pattern 0
FLK_MEAS0_1	0x0CB2	R/W	[7:0]		
FLK_MEAS0_2	0x0CB3	R/W	[7:0]		
FLK_MEAS0_3	0x0CB4	R/W	[7:0]		
FLK_MEAS1_0	0x0CB5	R/W	[7:0]	0x0	Score for Pattern 1
FLK_MEAS1_1	0x0CB6	R/W	[7:0]		
FLK_MEAS1_2	0x0CB7	R/W	[7:0]		
FLK_MEAS1_3	0x0CB8	R/W	[7:0]		
FLK_MEAS2_0	0x0CB9	R/W	[7:0]	0x0	Score for Pattern 2
FLK_MEAS2_1	0x0CBA	R/W	[7:0]		
FLK_MEAS2_2	0x0CBB	R/W	[7:0]		
FLK_MEAS2_3	0x0CBC	R/W	[7:0]		
FLK_MEAS3_0	0x0CBD	R/W	[7:0]	0x0	Score for Pattern 3
FLK_MEAS3_1	0x0CBE	R/W	[7:0]		
FLK_MEAS3_2	0x0CBF	R/W	[7:0]		
FLK_MEAS3_3	0x0CC0	R/W	[7:0]		
FLK_MEAS4_0	0x0CC1	R/W	[7:0]	0x0	Score for Pattern 4
FLK_MEAS4_1	0x0CC2	R/W	[7:0]		
FLK_MEAS4_2	0x0CC3	R/W	[7:0]		
FLK_MEAS4_3	0x0CC4	R/W	[7:0]		
FLK_MEAS5_0	0x0CC5	R/W	[7:0]	0x0	Score for Pattern 5
FLK_MEAS5_1	0x0CC6	R/W	[7:0]		
FLK_MEAS5_2	0x0CC7	R/W	[7:0]		
FLK_MEAS5_3	0x0CC8	R/W	[7:0]		
FLK_MEAS6_1	0x0CC9	R/W	[7:0]	0x0	Score for Pattern 6
FLK_MEAS6_2	0x0CCA	R/W	[7:0]		
FLK_MEAS6_3	0x0CCB	R/W	[7:0]		
FLK_MEAS6_4	0x0CCC	R/W	[7:0]		

Table 26: Flicker Registers (Sheet 3 of 3)

Register Name	Addr	Mode	Bits	Default	Description
FLK_MEAS7_0	0x0CCD	R/W	[7:0]	0x0	Score for Pattern 7
FLK_MEAS7_1	0x0CCE	R/W	[7:0]		
FLK_MEAS7_2	0x0CCF	R/W	[7:0]		
FLK_MEAS7_3	0x0CD0	R/W	[7:0]		

2.21 Gamma Block

The Gamma block performs an 8 bit to 10 bit lookup table on the 3 x 8 bits (R, G, B) color data coming from SCALER.

Table 27: Gamma Registers

Register Name	Addr	Mode	Bits	Default	Description
GAMMA_CTRL	0x0C10	R/W	[7:4]	0x0	Reserved
			[3]	0x0	0: Normal 1: Disable RAM access
			[2]	0x0	0: Normal 1: Test Mode
			[1:0]	0x0	Gamma Mode Select 0x0: 10b linear bypass 0x1: 8b->10b gamma table (normal) 0x2: 8b linear bypass (no interpolation) 0x3: 8b->10b gamma table (normal)

The RAMs are individually programmable (read and write) using I2C access. The memory map is as follows:

I2C address 0x1000 - 0x11FF: red RAM

I2C address 0x1200 - 0x13FF: green RAM

I2C address 0x1400 - 0x15FF: blue RAM

Even addresses are the 8-bit LSBs of the 10-bit gamma value. Odd addresses are the 2 MSBs.

2.22 APC Block

APC (formerly known as Arithmos Perfect Color) dithers an input 10-bit video stream down to 4-8 output bits. The dithering is done in space and time in such a way that the eye does not perceive objectionable artifacts such as:

- fixed dither patterns,
- contours,
- flickering pixels
- phase correlated flickering, which creates wave patterns known as "swimming".

Table 28: APC Registers

Register Name	Addr	Mode	Bits	Default	Description
APC_APC0	0x0C20		[7]		Reserved
		R/W	[6:5]	0x0	Frame Modulation Period - 1
		R/W	[4:1]	0x0	0x0 - 0x3: 8b Out 0x4: 4-bit Output 0x5: 5-bit Output 0x6: 6-bit Output 0x7: 7-bit Output 0x8: 8-bit Output
		R/W	[0]	0x0	0: normal 1: disable APC -- truncate LSBs
APC_APC1	0x0C21		[7:2]		Reserved
		R/W	[1]	0x0	Offset the Phase LUT
		R/W	[0]	0x0	Offset the Dither LUT

2.23 Output Mux Block

Table 29: Output Mux Registers (Sheet 1 of 3)

Register Name	Addr	Mode	Bits	Default	Description
OMUX_CTRL_0	0x0C30	R/W	[7]	0x0	in 2 ppc, 0: data invert for A+B comb. 1: data invert A/B separate
		R/W	[6:4]	0x0	0x0 - 0x4: right shift per 8b R/G/B 0x5 - 0x7: Reserved
		R/W	[3]	0x0	0: normal 1: flip MSBs to LSBs
		R/W	[2]	0x0	0: normal 1: swap R and B data
		R/W	[1]	0x0	0: in 1 ppc, A channel active 0: in 2 ppc, Left on A, Right on B 1: in 1 ppc, B channel active 1: 2ppc, Left on B, Right on A
		R/W	[0]	0x0	0: single wide, one pix/clk (ppc) 1: double wide, two pix/clk
OMUX_CTRL_1	0x0C31	R/W	[7]	0x0	Vsync Output Polarity
		R/W	[6]	0x0	Hsync Output Polarity
		R/W	[5]	0x0	Data Enable Output Polarity
		R/W	[4]	0x0	Clock Output Invert
		R/W	[3]	0x0	Data Invert Output Polarity
		R/W	[2]	0x0	Data Invert Enable
		R/W	[1]	0x0	0: TCON outputs set to zero 1: TCON outputs active
		R/W	[0]	0x0	0: all data outputs set to zero 1: output enabled

Table 29: Output Mux Registers (Sheet 2 of 3)

Register Name	Addr	Mode	Bits	Default	Description
OMUX_CTRL_2	0x0C32	R/W	[7]	0x0	Seperate TCON Driven Invert Enable
		R/W	[6]	0x0	TCON Driven Invert Pin Enable
		R/W	[5]	0x0	RSDS enable
		R/W	[4]	0x0	Per Pin Delay Enable
		R/W	[3]	0x0	Resync on Vsync Falling Edge
		R/W	[2]	0x0	Resync on Vsync Rising Edge
		R/W	[1]	0x0	Resync on Hsync Falling Edge
		R/W	[0]	0x0	Resync on Hsync Rising Edge
OMUX_DLY_BA0	0x0C50	R/W	[7:4]	0x0	Delay for OBA1
		R/W	[3:0]	0x0	Delay for OBA0
OMUX_ DLY_BA2	0x0C4F	R/W	[7:4]	0x0	Delay for OBA3
		R/W	[3:0]	0x0	Delay for OBA2
OMUX_ DLY_BA4	0x0C4E	R/W	[7:4]	0x0	Delay for OBA5
		R/W	[3:0]	0x0	Delay for OBA4
OMUX_ DLY_BA6	0x0C4D	R/W	[7:4]	0x0	Delay for OBA7
		R/W	[3:0]	0x0	Delay for OBA6
OMUX_ DLY_GA0	0x0C4C	R/W	[7:4]	0x0	Delay for OGA1
		R/W	[3:0]	0x0	Delay for OGA0
OMUX_ DLY_GA2	0x0C4B	R/W	[7:4]	0x0	Delay for OGA3
		R/W	[3:0]	0x0	Delay for OGA2
OMUX_ DLY_GA4	0x0C4A	R/W	[7:4]	0x0	Delay for OGA5
		R/W	[3:0]	0x0	Delay for OGA4
OMUX_ DLY_GA6	0x0C49	R/W	[7:4]	0x0	Delay for OGA7
		R/W	[3:0]	0x0	Delay for OGA6
OMUX_ DLY_RA0	0x0C48	R/W	[7:4]	0x0	Delay for ORA1
		R/W	[3:0]	0x0	Delay for ORA0
OMUX_ DLY_RA2	0x0C47	R/W	[7:4]	0x0	Delay for ORA3
		R/W	[3:0]	0x0	Delay for ORA2
OMUX_ DLY_RA4	0x0C46	R/W	[7:4]	0x0	Delay for ORA5
		R/W	[3:0]	0x0	Delay for ORA4
OMUX_ DLY_RA6	0x0C45	R/W	[7:4]	0x0	Delay for ORA7
		R/W	[3:0]	0x0	Delay for ORA6
OMUX_ DLY_BB0	0x0C44	R/W	[7:4]	0x0	Delay for OBB1
		R/W	[3:0]	0x0	Delay for OBB0
OMUX_ DLY_BB2	0x0C43	R/W	[7:4]	0x0	Delay for OBB3
		R/W	[3:0]	0x0	Delay for OBB2
OMUX_ DLY_BB4	0x0C42	R/W	[7:4]	0x0	Delay for OBB5
		R/W	[3:0]	0x0	Delay for OBB4
OMUX_ DLY_BB6	0x0C41	R/W	[7:4]	0x0	Delay for OBB7
		R/W	[3:0]	0x0	Delay for OBB6
OMUX_ DLY_GB0	0x0C40	R/W	[7:4]	0x0	Delay for OGB1
		R/W	[3:0]	0x0	Delay for OGB0
OMUX_ DLY_GB2	0x0C3F	R/W	[7:4]	0x0	Delay for OGB3
		R/W	[3:0]	0x0	Delay for OGB2

Table 29: Output Mux Registers (Sheet 3 of 3)

Register Name	Addr	Mode	Bits	Default	Description
OMUX_ DLY_GB4	0x0C3E	R/W	[7:4]	0x0	Delay for OGB5
		R/W	[3:0]	0x0	Delay for OGB4
OMUX_ DLY_GB6	0x0C3D	R/W	[7:4]	0x0	Delay for OGB7
		R/W	[3:0]	0x0	Delay for OGB6
OMUX_ DLY_RB0	0x0C3C	R/W	[7:4]	0x0	Delay for ORB1
		R/W	[3:0]	0x0	Delay for ORB0
OMUX_ DLY_RB2	0x0C3B	R/W	[7:4]	0x0	Delay for ORB3
		R/W	[3:0]	0x0	Delay for ORB2
OMUX_ DLY_R_B4	0x0C3A	R/W	[7:4]	0x0	Delay for ORB5
		R/W	[3:0]	0x0	Delay for ORB4
OMUX_ DLY_R_B6	0x0C39	R/W	[7:4]	0x0	Delay for ORB7
		R/W	[3:0]	0x0	Delay for ORB6
OMUX_ DLY_TCON_0	0x0C38	R/W	[7:4]	0x0	Delay for TCON1
		R/W	[3:0]	0x0	Delay for TCON0
OMUX_ DLY_TCON_2	0x0C37	R/W	[7:4]	0x0	Delay for TCON3
		R/W	[3:0]	0x0	Delay for TCON2
OMUX_ DLY_TCON_4	0x0C36	R/W	[7:4]	0x0	Delay for TCON5
		R/W	[3:0]	0x0	Delay for TCON4
OMUX_ DLY_TCON_6	0x0C35	R/W	[7:4]	0x0	Delay for TCON7
		R/W	[3:0]	0x0	Delay for TCON6
OMUX_ DLY_VS_ENAB	0x0C34	R/W	[7:4]	0x0	Delay for VSYNC
		R/W	[3:0]	0x0	Delay for ENAB
OMUX_ DLY_CLK_HS	0x0C33	R/W	[7:4]	0x0	Delay for CLK
		R/W	[3:0]	0x0	Delay for HSYNC
OMUX_CTRL_3	0x0C51	R/W	[7:3]		Reserved
		R/W	[2]	0x0	PWM mux mode
		R/W	[1]	0x0	PWM enable
		R/W	[0]	0x0	TCON data invert enable, with computed data invert pin.
OMUX_REFCOUNT	0x0C52		[7:6]		Reserved
		R	[5:0]	0x0	returns a value that indicates the ADE gate speed -- a function of temp and voltage higher = faster logic

2.24 Pulse Width Modulation (PWM) Block

The PWM B block generates two signals to control backlight inverter switching power components directly. It is derived from XCLK and powered up independently of the DOTCLK and INCLK domains. Frequency, duty cycle, polarity and overlap/non-overlap are programmable. The output frequency can “free-run” or lock to output vsync.

Table 30: PWM Registers

Register Name	Addr	Mode	Bits	Default	Description
PWM_CTRL0	0x01A0	R	[7]	0x0	PWM status 0: unlocked 1: locked
		R/W	[6]	0x0	0: lock to CYCLES_PER_FRAME from the free run state machine 1: lock to CYCLES_PER_FRAME register setting
		R/W	[5]	0x0	PWM_A polarity 0: active low 1: active high
		R/W	[4]	0x0	PWM_B polarity 0: active low 1: active high
		R/W	[3]	0x0	0: normal operation 1: force PWM outputs to polarity settings
		R/W	[2]	0x0	0: change period or duty cycle at the end of the current cycle 1: smooth change, period or duty cycle increment/decrement every PWM_STEP_DELAY cycle
		R/W	[1]	0x0	0: free run 1: lock to out_vsync
		R/W	[0]	0x0	0: disable PWM output 1: enable PWM output
PWM_CTRL1	0x01A1	R/W	[7:4]	0x0	Lock 2^{nd} order gain (power of 2) 0x0 = max 0x3 = typical 0xF = min
		R/W	[3:0]	0x0	Lock gain (power of 2) 0x0 = max 0x6 = typical 0xF = min
PWM_PERIOD_L	0x01A2	R/W	[7:0]	0x0	Period-2 in Free-running mode, in XCLKs
PWM_PERIOD_H	0x01A3	R/W	[7:0]		
PWM_DUTY_L	0x01A4	R/W	[7:0]	0x0	Duty cycle of PWM in XCLKs
PWM_DUTY_H	0x01A5	R/W	[7:0]		
PWM_OVERLAP_L	0x01A6	R/W	[7:0]	0x0	Non-overlap of PWMs in XCLKs
PWM_OVERLAP_H	0x01A7	R/W	[7:0]		
PWM_STEP_DELAY	0x01A8	R/W	[7:0]	0x0	In smooth change mode, the number of cycles skipped before the period/duty registers are incremented/decremented
PWM_CYCLES_PER_FRAME_L	0x01A9	R/W	[7:0]	0x0	The number of cycles per frame in frame lock mode when not using the internally generated cycles per frame from a previous freerun mode
PWM_CYCLES_PER_FRAME_H	0x01AA	R/W	[7:0]		

2.25 DFT Block

Table 31: DFT Registers (Sheet 1 of 2)

Register Name	Addr	Mode	Bits	Default	Description
DFT_TEST_MODE	0x0F00		[7:4]		Reserved
		R/W	[3]	0x0	trigger video bus MFSR
		R/W	[2]	0x0	enable output pin MFSR
		R/W	[1]	0x0	clear output pin MFSR
		R/W	[0]	0x0	output pin test override
DFT_MUX_OUT_MODE	0x0F01		[7:6]		Reserved
		R/W	[5:0]	0x0	mux selector for output porta/b and syncs
DFT_FLOP_OUT_MODE	0x0F02		[7:6]		Reserved
		R/W	[5:0]	0x0	mux selector for synchronous digital debug bus
DFT_CLK_0UT_MODE	0x0F03	R/W	[7:6]	0x0	divide-by selector for clocks to OCLK pin fout = selected clock / (2 ^ value)
		R/W	[5:0]	0x0	mux selector for clocks to OCLK pin
DFT_CLK_1_MODE	0x0F04	R/W	[7:6]	0x0	divide-by selector for clocks to CLKOUT pin fout = selected clock / (2 ^ value)
DFT_CLK_2_MODE	0x0F05	R/W	[5:0]	0x0	mux selector for clocks to CLKOUTpin
DFT_OUT_DISAB_0	0x0F06	R/W	[7:0]	0x0	disable porta red output in test mode
DFT_OUT_DISAB_1	0x0F07	R/W	[7:0]	0x0	disable porta green output in test mode
DFT_OUT_DISAB_2	0x0F08	R/W	[7:0]	0x0	disable porta blue output in test mode
DFT_OUT_DISAB_3	0x0F09	R/W	[7:0]	0x0	disable portb red output in test mode
DFT_OUT_DISAB_4	0x0F0A	R/W	[7:0]	0x0	disable portb green output in test mode
DFT_OUT_DISAB_5	0x0F0B	R/W	[7:0]	0x0	disable portb blue output in test mode
DFT_OUT_DISAB_6	0x0F0C	R/W	[7:3]	0x0	disable tcon bits [4:0] in test mode
		R/W	[2]	0x0	disable vert sync output in test mode
		R/W	[1]	0x0	disable data enab output in test mode
		R/W	[0]	0x0	disable horz sync output in test mode
DFT_OUT_DISAB_7	0x0F0D		[7:5]		Reserved
		R/W	[4]	0x0	disable CLKOUT output in test mode
		R/W	[3]	0x0	disable OCLK output in test mode
		R/W	[2:0]	0x0	disable tcon bits [7:5] in test mode
DFT_STIM_CTRL	0x0F0E		[7:6]		Reserved
		R/W	[0]	0x0	internal stimulus bus enable
DFT_STIM_EN_0	0x0F0F	R/W	[7]	0x0	SCL test stimulus enable
		R/W	[6]		HDCP test stimulus enable
		R/W	[5]		DVI test mode enable
		R/W	[4]		DVI blue test stimulus enable
		R/W	[3]		DVI green test stimulus enable
		R/W	[2]	0x0	DVI red test stimulus enable
		R/W	[1]	0x0	ADC test stimulus enable
		R/W	[0]	0x0	YUV test stimulus enable

Table 31: DFT Registers (Sheet 2 of 2)

Register Name	Addr	Mode	Bits	Default	Description
DFT_STIM_EN_1	0x0F10		[7:6]		Reserved
		R/W	[5]	0x0	TCON test bypass
		R/W	[4]	0x0	OMUX test stimulus enable
		R/W	[3]	0x0	APC test stimulus enable
		R/W	[2]	0x0	OSD test stimulus enable
		R/W	[1]	0x0	SCL bypass
		R/W	[0]	0x0	PGEN test stimulus enable
DFT_BIST_STATUS	0x0F11		[7:6]		Reserved
		R	[5]		gamma RAM BIST end
		R	[4]		OSD CS RAM BIST end
		R	[3]		OSD DRB RAM BIST
		R	[2]		OSD MB RAM BIST end
		R	[1]		SCL coeff. RAM BIST end
		R	[0]		SCL line buffer RAM BIST end
DFT_BIST_RESULT_0	0x0F12		[7:6]		Reserved
		R	[5]		SCL coeff RAM 2 BIST fail
		R	[4]		SCL coeff RAM 1 BIST fail
		R	[3]		SCL line buffer 4 BIST fail
		R	[2]		SCL line buffer 3 BIST fail
		R	[1]		SCL line buffer 2 BIST fail
		R	[0]		SCL line buffer 1 BIST fail
DFT_BIST_RESULT_1	0x0F13		[7]		Reserved
		R	[6]		Gamma blue RAM BIST fail
		R	[5]		Gamma green RAM BIST fail
		R	[4]		Gamma red RAM BIST fail
		R	[3]		OSD CS RAM1 BIST fail
		R	[2]		OSD CS RAM 2 BIST fail
		R	[1]		OSD DRB RAM BIST fail
		R	[0]		OSD MB RAM BIST fail
DFT_MFSR_DONE	0x0F14		[7:1]		Reserved
		R	[0]		done signal
DFT_MFSR_SIG_0	0x0F15	R	[7:0]	0x0	Video Bus MFSR
DFT_MFSR_SIG_1	0x0F16	R	[7:0]		
DFT_MFSR_SIG_2	0x0F17	R	[7:0]		
DFT_MFSR_SIG_3	0x0F18	R	[7:0]		

2.26 I²C RAM Addresses

Table 32: I²C RAM Addresses

Name	Start Addr.	End Addr.	Description
GAM_RED	0x1000	0x11FF	Gamma LUT, Red, LSB0,MSB0,LSB1,... (256x10)
GAM_GREEN	0x1200	0x13FF	Gamma LUT, Green, (256x10)
GAM_BLUE	0x1400	0x15FF	Gamma LUT, Blue, (256x10)

Table 32: I²C RAM Addresses

Name	Start Addr.	End Addr.	Description
OSD_MB	0x1700	0x175F	OSD Color LUTs (32x24)
OSD_CS	0x3000	0x5F3F	OSD Character Map (1344x36x2 copies)
OSD_DRB	0x6000	0x647F	OSD Screen Map (1152x8)
SCL_COEFF	0x9000	0x98FF	Scaler Coefficient RAM (256x36x2 copies)
SCL_LINE1	0x9900	0xA7FF	Scaler Line Buffer 1 (1280x24)
SCL_LINE2	0xA800	0xB6FF	Scaler Line Buffer 2 (1280x24)
SCL_LINE3	0xB700	0xC5FF	Scaler Line Buffer 3 (1280x24)
SCL_LINE4	0xC600	0xD4FF	Scaler Line Buffer 4 (1280x24)

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
AVDD18 DVDD18 XVDD18 LVDD18	Supply Voltage			1.95	V
AVDD33 DVDD33	Supply Voltage			3.6	V
VIN	Max voltage on 5 volt tolerant input pins			6.1	V
T_{STG}	Storage Temperature	-40		+150	°C

3.2 Power Consumption Matrices

Table 33: ADE3100

Symbol	Parameter	Min	Typ*	Max**	Unit
	Supply Current (Analog Input, XGA@75Hz, 78.75MHz)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})		188	197	mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})		213	240	mA
I_{AVDD33}	3.3V analog supply ($_{IAVDD33}$)		109	113	mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})		64	69	mA
	Supply Current (DVI Input, XGA@75Hz, 78.75MHz)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})		57	67	mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})		222	250	mA
I_{AVDD33}	3.3V analog supply (I_{AVDD33})		109	115	mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})		59	67	mA
	Supply Current (Stand By Mode)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})	3.4		3.9	mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})	3.9		5.4	mA
I_{AVDD33}	3.3V analog supply (I_{AVDD33})	0.5		3.9	mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})	2.5		3.0	mA
P_{TOTANA}	Total Power Consumption (Analog Input, XGA@75Hz, 78.75MHz)		1.55	1.85	W
P_{TOTDVI}	Total Power Consumption (DVI Input, XGA@75Hz, 78.75MHz)		1.4	1.73	W
$P_{STANDBY}$	Total Power Consumption (Stand By Mode)	23.2		39.4	mW

* *Measured at nominal voltage supplies*

** *Measured at +10% voltage supplies*

Table 34: ADE3300

Symbol	Parameter	Min	Typ*	Max**	Unit
	Supply Current (Analog Input, XGA@75Hz, 135MHz)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})		193	199	mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})		346	380	mA
I_{AVDD33}	3.3V analog supply ($_{IAVDD33}$)		109	113	mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})		67	82	mA
	Supply Current (DVI Input, XGA@75Hz, 135MHz)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})		58	68	mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})		371	415	mA
I_{AVDD33}	3.3V analog supply (I_{AVDD33})		114	120	mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})		77	94	mA
	Supply Current (Stand By Mode)				
I_{AVDD18}	1.8V analog supply (I_{AVDD18})	3.4			mA
I_{DVDD18}	1.8V digital supply (I_{DVDD18})	3.9			mA
I_{AVDD33}	3.3V analog supply (I_{AVDD33})	3.9			mA
I_{DVDD33}	3.3V digital supply (I_{DVDD33})	3.9			mA
P_{TOTANA}	Total Power Consumption (Analog Input, XGA@75Hz, 135MHz)		1.55	1.85	W
P_{TOTDVI}	Total Power Consumption (DVI Input, XGA@75Hz, 135MHz)		1.4	1.73	W
$P_{STANDBY}$	Total Power Consumption (Stand By Mode)		38.9		mW

** Measured at nominal voltage supplies*

*** Measured at +10% voltage supplies*

3.3 Nominal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVDD18 DVDD18 XVDD18 LVDD18	Supply Voltage	1.71	1.8	1.89	V
AVDD33 DVDD33	Supply Voltage	3.135	3.3	3.465	V
f_{XTAL}	Crystal Frequency		27		MHz
T_{OPER}	Ambient Operating Temperature	0		+70	°C

3.4 Preliminary Thermal Data

Symbol	Parameter	Min	Typ	Max	Unit
R_{thJA}	Junction-to-Ambient Thermal Resistance			25	°C/W

3.5 Preliminary DC Specifications

Test Conditions: DVDD33 = AVDD33 = 3.3V, DVDD18 = AVDD18 = XVDD18 = LVDD18 = 1.8V, and T_{AMB} = 25°C

3.5.1 LVTTL 5 Volt Tolerant Inputs With Hysteresis

YUV[0:7], YUVCLK, HSYNC, VSYNC, CSYNC, TCON_IN, SCL, RESETN

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input voltage		2.0			V
V_{IL}	Low Level Input voltage				0.8	V
V_{HYST}	Schmitt trigger hysteresis		0.4			V

3.5.2 LVTTL 5 Volt Tolerant Inputs

XCLK_EN

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input voltage		2.0			V
V_{IL}	Low Level Input voltage				0.8	V

3.5.3 LVTTL 5 Volt Tolerant I/O With Hysteresis

SDA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input voltage		2.0			V
V_{IL}	Low Level Input voltage				0.8	V
V_{HYST}	Schmitt trigger hysteresis		0.4			V

3.5.4 LVTTL Outputs

OBA[0:7], OGA[0:7], ORA[0:7], OBB[0:7], OGB[0:7], ORB[0:7], OHS, OVS, ODE, OCLK

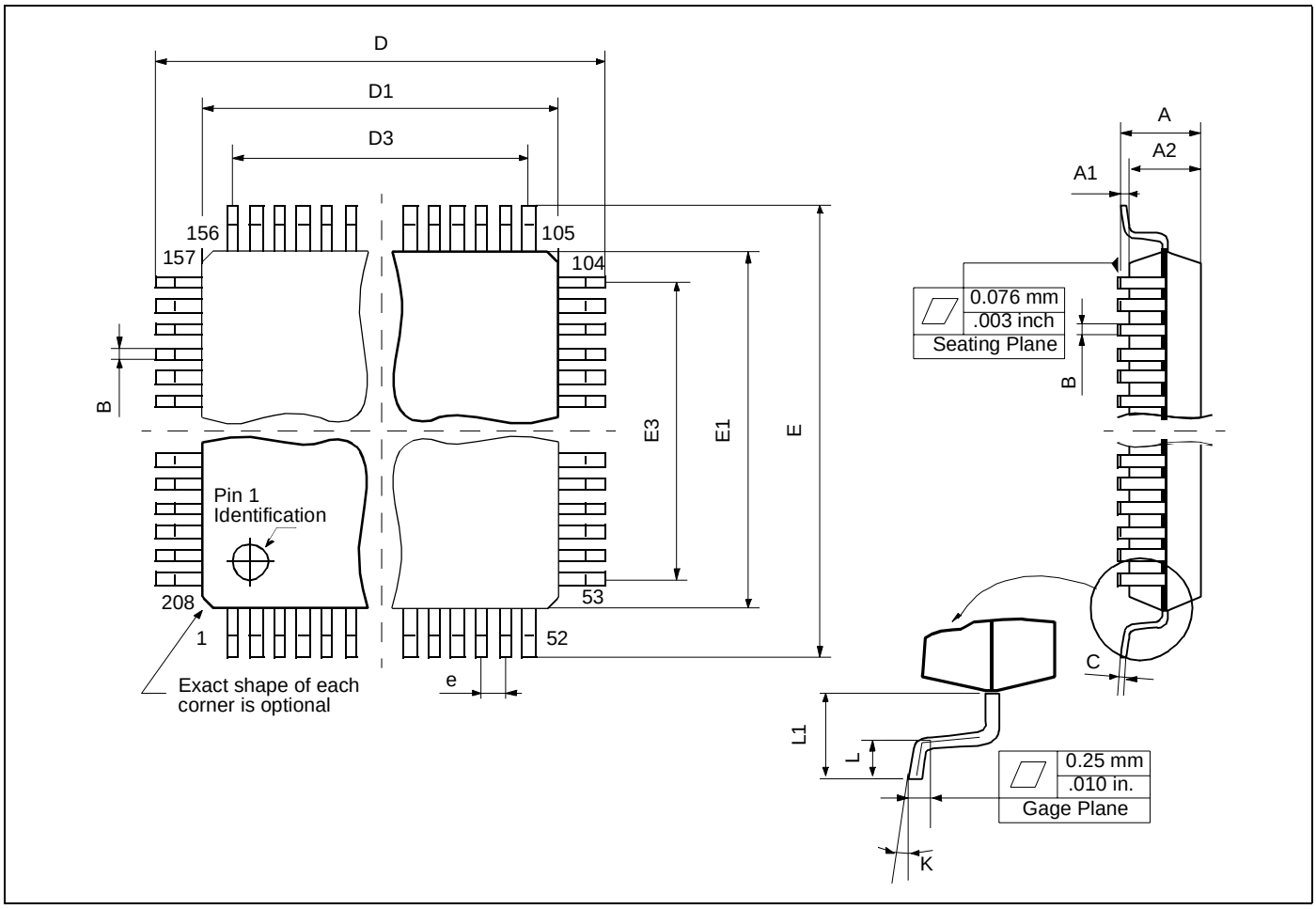
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input voltage		2.0			V
V_{IL}	Low Level Input voltage				0.8	V
I_{IH}	High Level Input current	VIN = VDD			-10	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}	Low Level Input current	VIN = 0V			10	µA

3.6 Preliminary AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
fDVI	DVI input pixel frequency		20		140	MHz
Vdvi_diff	DVI differential input voltage		150		1200	mV
Vdvi_icm	DVI input common mode voltage		AVDD33 - 0.3		AVDD33 - 0.037	V
Vdvi_vin	DVI input voltage	When Tx disabled or disconnected	AVDD33 - 0.01		AVDD33 + 0.01	V
Idvi_leak	DVI input leackage current	RX powered down			10	µA
Rdvi_term	DVI input termination resistance	Rext = 470 Ohms	45	50	55	Ohm
Vrsds_diff	RSDS differential output voltage	RSDS mode	100	200	400	mV
Vrsrs_cm	RSDS common mode output voltage	680 ohm + 50 ohm external termination to 1.3V	1.1	1.3	1.5	V
Trise, Tfall	RSDS transition time to 90%	CL = 30pF			3	ns
INL	ADC integral nonlinearity (9b)			1.5		LSB
DNL	ADC differential nonlinearity (9b)	no missing codes		1.5		LSB
Vadc_in	ADC input voltage range		0.5		1	Vp-p
ENOB	ADC effective number of bits	135MSPS Input = 65MHz sine at 95% FS		7.5		bits
Radc_in	ADC input resistance			200		Kohms
Cadc_in	ADC input capacitance				8	pF
Fadc	ADC sample frequency		20		140	MHz
ADC gain step	ADC gain step size			0.05		dB
ADC offset step	ADC offset step size			4		mV
Cadc_ext	ADC external AC coupling cap			0.1		uF

4 Package Mechanical Data



	Dimensions (mm)			Dimensions (inches)		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A			4.10			0.161
A1	0.25	0.30	0.40	0.010		
A2	3.20	3.40	3.60	0.126	0.134	0.142
B	0.17		0.27	0.007		0.011
C	0.09		0.20	0.003		0.008
D		30.60			1.205	
D1		28.00			1.102	
D3		25.50			1.004	
e		0.50			0.020	
E		30.60			1.205	
E1		28.00			1.102	
E3		25.50			1.004	
L	0.45	0.60	0.75	0.018	0.024	0.029
L1		1.30			0.051	
K	0° (min.), 3.5°(typ.), 7°(max.)					

Note: Exact shape of each corner is optional

5 Revision History

Table 35: Summary of Modifications

Version	Date	Description of Modification
0.1	22 Oct. 2002	First Issue
1.0	25 Nov 2002	Update of registers SMEAS_V_CTRL, SMUX_CTRL0 and FLK_CTRL.
1.1	05 Feb 2003	Changed "Projection Display Engine" to "LCD Display Engine" on page 1. Changed header name “ADE3500X/3600X” to “ADE3XXX” on page 2.
1.2	18 Apr 2003	Deletion of YUV port information.
1.3	10 July 2003	Inclusion of Section 3.2: Power Consumption Matrices on page 82.
1.4	17 July 2003	Re-insertion of YUV port information.

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