

20V Complementary MOSFET

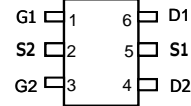
Product Summary

N-Channel	P-Channel
$V_{DS} = 20V$	-20V
$I_D = 3.4A$ ($V_{GS} = 4.5V$)	-2.5A ($V_{GS} = -4.5V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 65m Ω ($V_{GS} = 4.5V$)	< 75m Ω ($V_{GS} = -4.5V$)
< 75m Ω ($V_{GS} = 2.5V$)	< 105m Ω ($V_{GS} = -2.5V$)
< 100m Ω ($V_{GS} = 1.8V$)	< 180m Ω ($V_{GS} = -1.8V$)

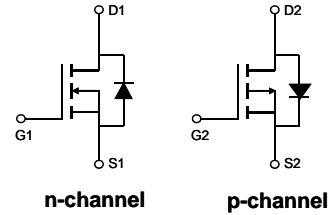
FEATURE

- High power and current handing capability
- Lead free product is acquired
- Surface mount package

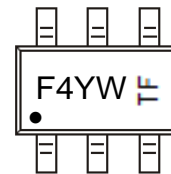
SOT-23-6L



Equivalent Circuit



MARKING



Y :year code W :week code

Absolute Maximum Ratings $T = 25^\circ C$ unless otherwise noted					
Parameter		Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	± 8	± 8	V
Continuous Drain Current	$T_A = 25^\circ C$	I_D	3.4	-2.5	A
	Pulsed Drain Current ^C		I_{DM}	13	
Power Dissipation ^B	$T_A = 25^\circ C$	P_D	1.1	1.1	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		$^\circ C$
Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	78	110	$^\circ C/W$
	Steady-State		106	150	
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	64	80	$^\circ C/W$



SHENZHEN TUOFENG SEMICONDUCTOR TECHNOLOGY CO.,LTD
N and P-Channel Enhancement Mode Power MOSFET

6604

N-Channel Electrical Characteristics (T_j=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±8V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.4	0.7	1	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	13			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =3.4A		51	65	mΩ
		V _{GS} =2.5V, I _D =3A		58	75	mΩ
		V _{GS} =1.8V, I _D =2A		68	100	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =3.4A		16		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				1.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V, f=1MHz	205	260	320	pF
C _{oss}	Output Capacitance		33	48	63	pF
C _{rss}	Reverse Transfer Capacitance		16	27	38	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.5	3	4.5	Ω
SWITCHING PARAMETERS						
Q _{g(4.5V)}	Total Gate Charge	V _{GS} =4.5V, V _{DS} =10V, I _D =3.4A		2.9	3.8	nC
Q _{gs}	Gate Source Charge		0.4		nC	
Q _{gd}	Gate Drain Charge		0.6		nC	
t _{D(on)}	Turn-On DelayTime	V _{GS} =5V, V _{DS} =10V, R _L =2.95Ω, R _{GEN} =3Ω		2.5		ns
t _r	Turn-On Rise Time		3.2		ns	
t _{D(off)}	Turn-Off DelayTime		21		ns	
t _f	Turn-Off Fall Time		3		ns	
t _{rr}	Body Diode Reverse Recovery Time	I _F =3.4A, dI/dt=100A/μs		14	19	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3.4A, dI/dt=100A/μs		3.8		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_j=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

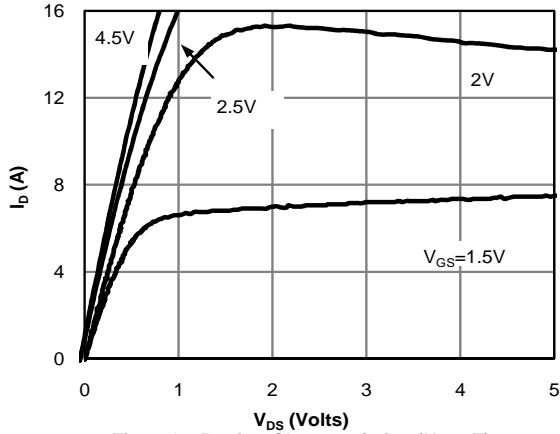


Fig 1: On-Region Characteristics (Note E)

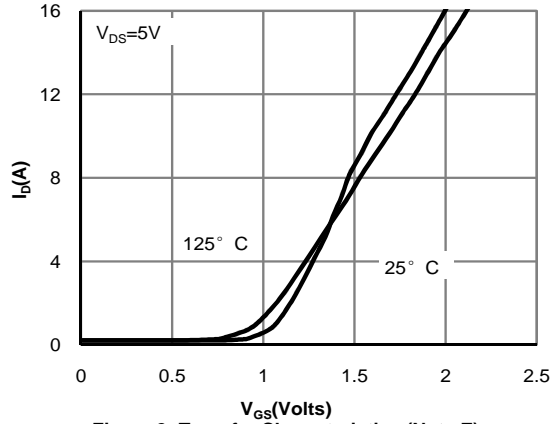


Figure 2: Transfer Characteristics (Note E)

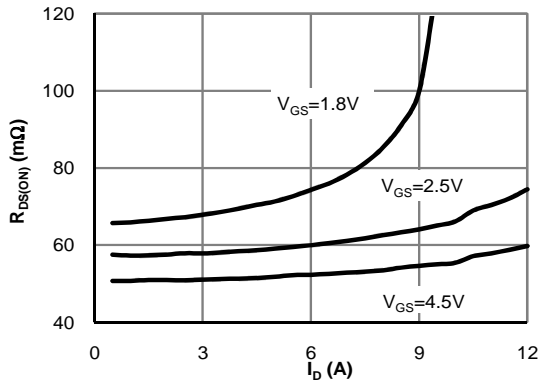


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

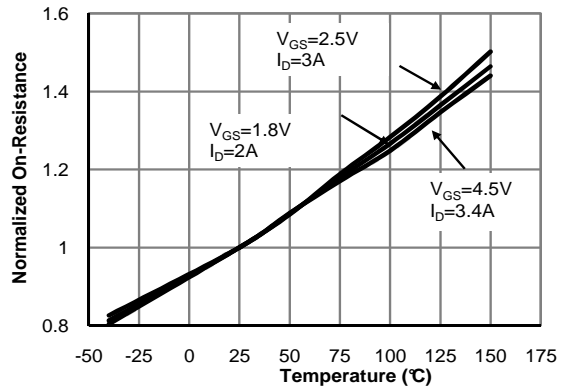


Figure 4: On-Resistance vs. Junction Temperature (Note E)

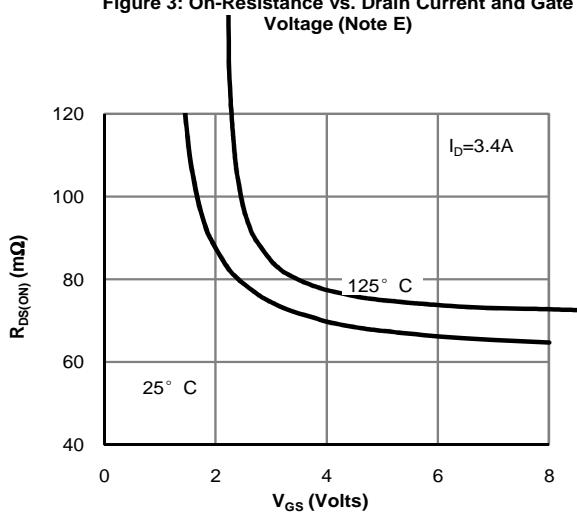


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

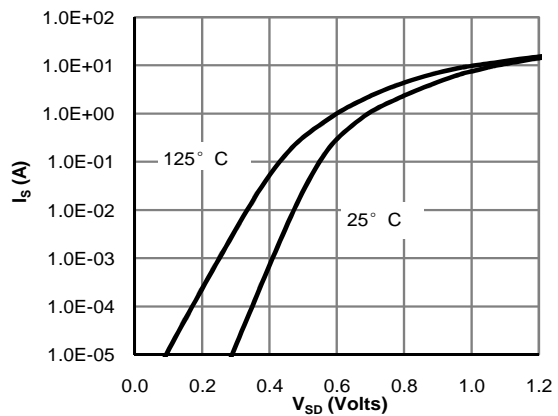


Figure 6: Body-Diode Characteristics (Note E)

N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

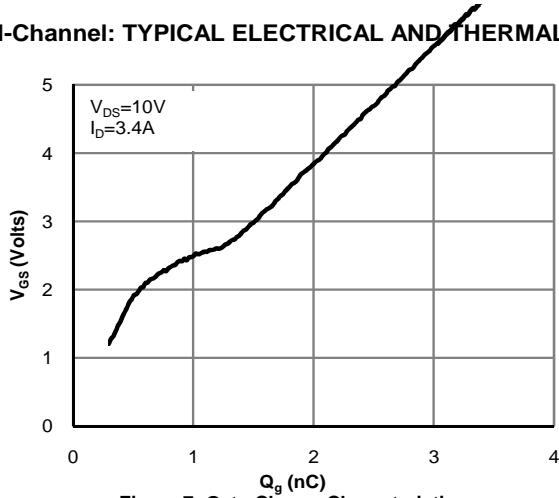


Figure 7: Gate-Charge Characteristics

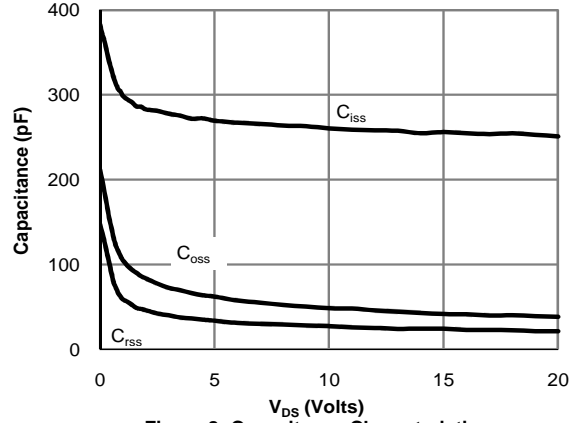


Figure 8: Capacitance Characteristics

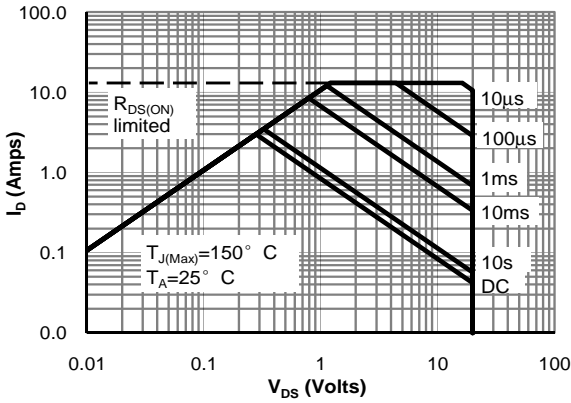


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

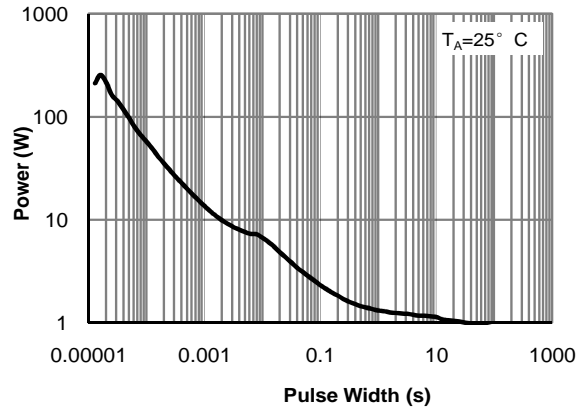


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

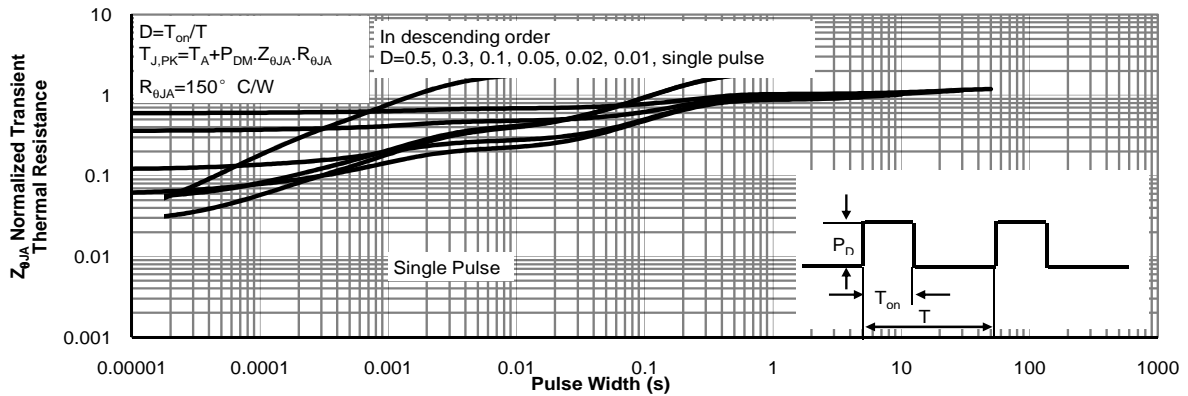
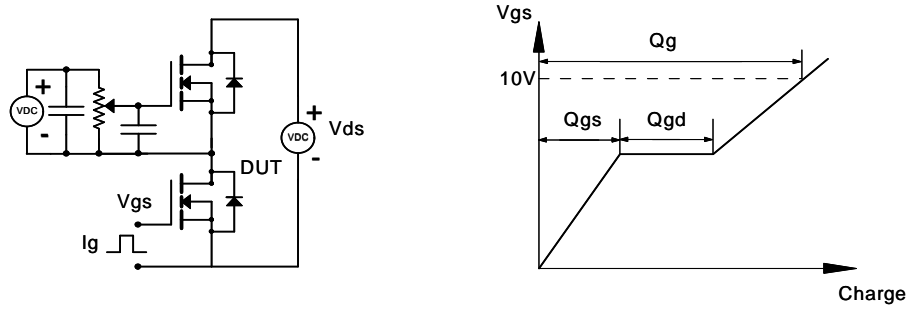
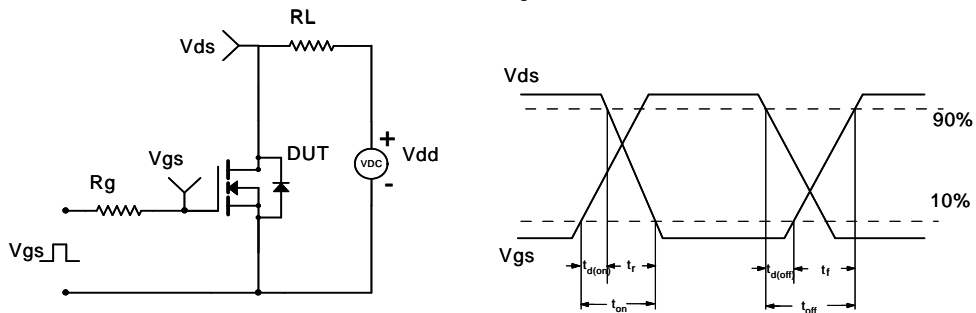


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

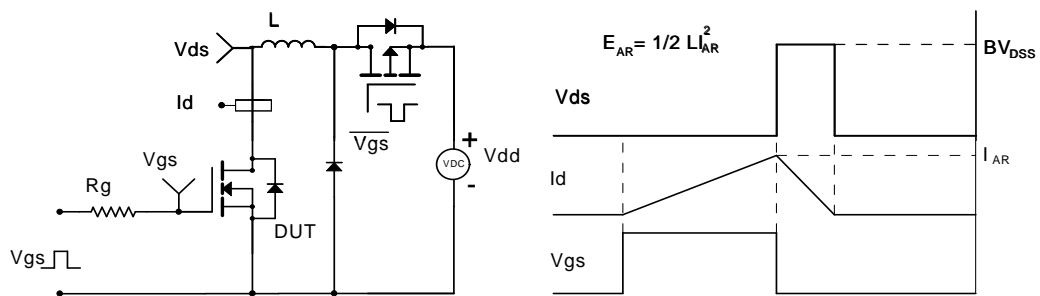
Gate Charge Test Circuit & Waveform



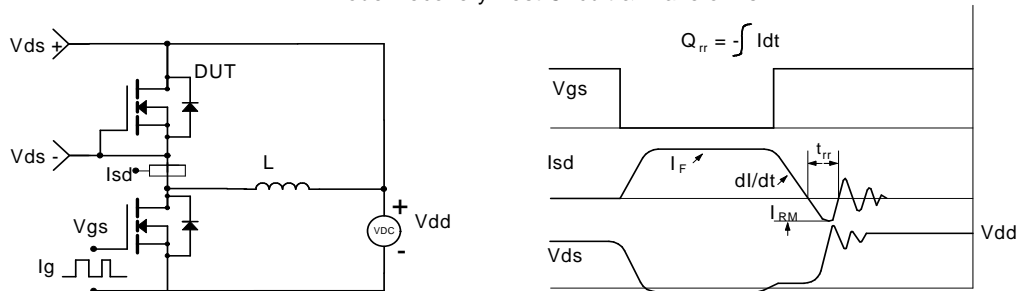
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms





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N and P-Channel Enhancement Mode Power MOSFET

6604

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V			-1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±8V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.4	-0.65	-1	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-13			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-2.5A		65	75	mΩ
		V _{GS} =-2.5V, I _D =-2A		95	105	mΩ
		V _{GS} =-1.8V, I _D =-1A		170	180	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-2.5A		13		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1	V
I _S	Maximum Body-Diode Continuous Current				-1.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		560	745	pF
C _{oss}	Output Capacitance			80		pF
C _{rss}	Reverse Transfer Capacitance			70		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		15	23	Ω
SWITCHING PARAMETERS						
Q _g (4.5V)	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-2.5A		8.5	11	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			2.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-4.5V, V _{DS} =-10V, R _L =4Ω, R _{GEN} =6Ω		7.2		ns
t _r	Turn-On Rise Time			36		ns
t _{D(off)}	Turn-Off DelayTime			53		ns
t _f	Turn-Off Fall Time			56		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-2.5A, dI/dt=100A/μs		37	49	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-2.5A, dI/dt=100A/μs		27		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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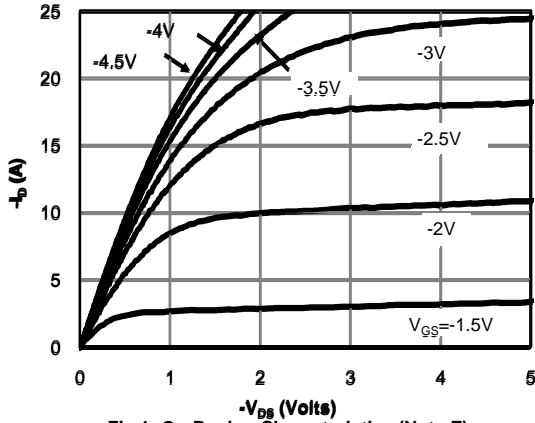


Fig 1: On-Region Characteristics (Note E)

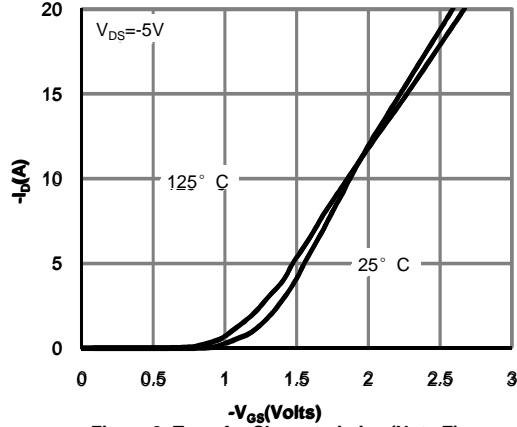


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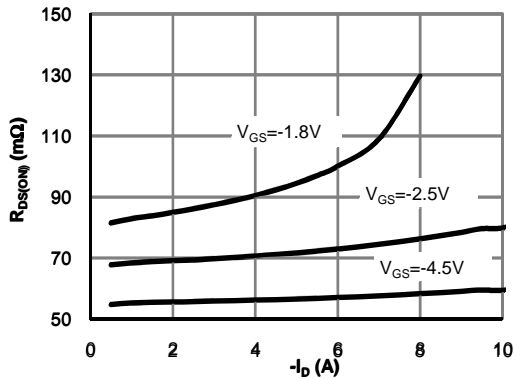


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

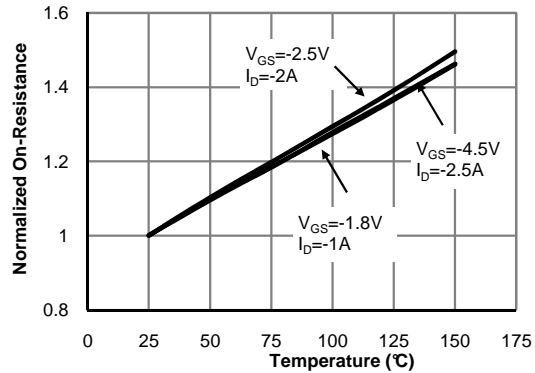


Figure 4: On-Resistance vs. Junction Temperature (Note E)

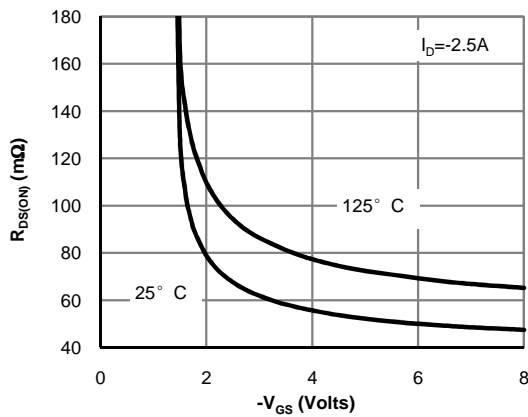


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

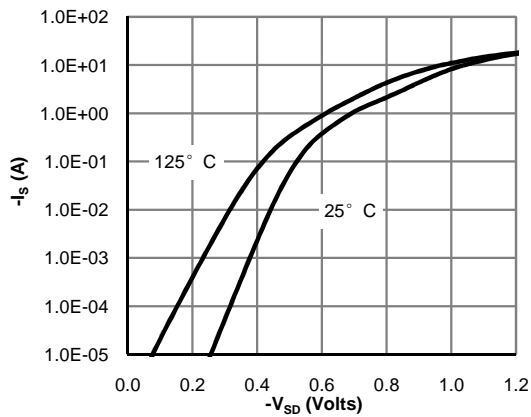


Figure 6: Body-Diode Characteristics (Note E)

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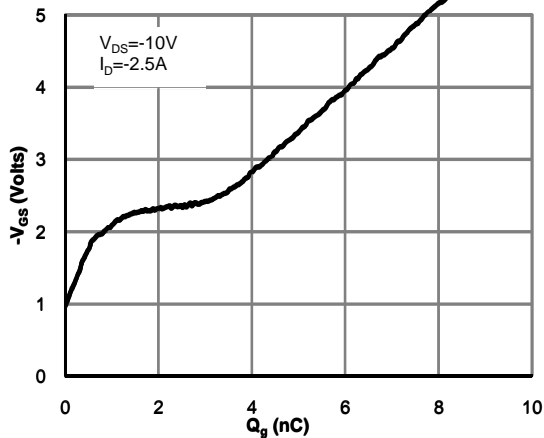


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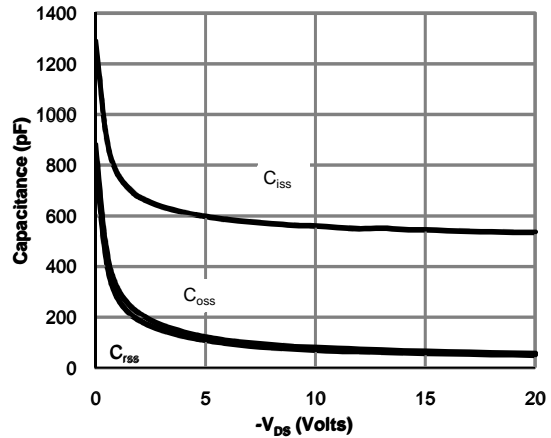


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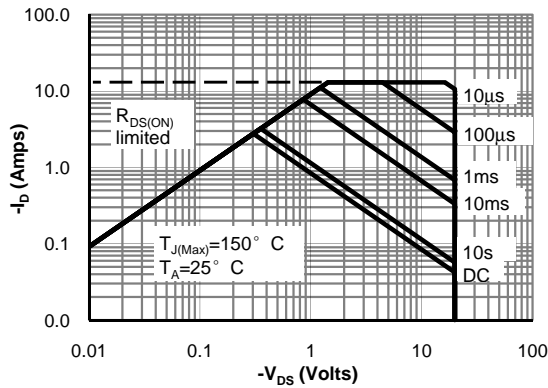


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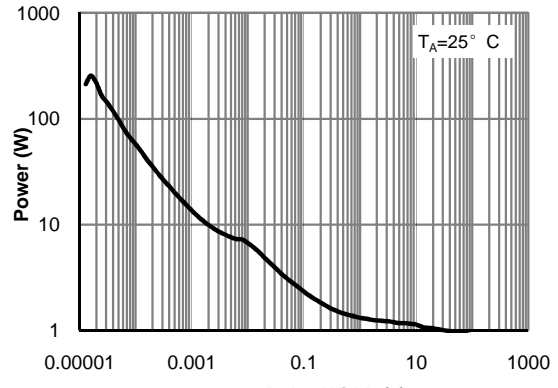


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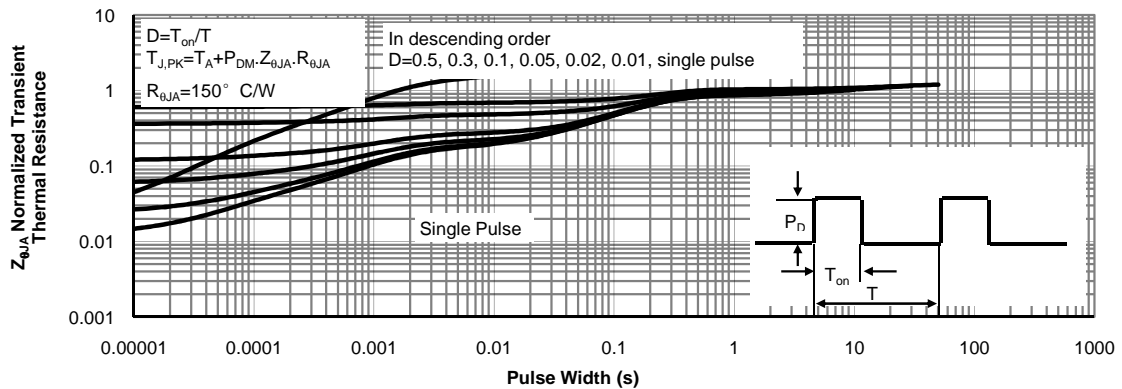
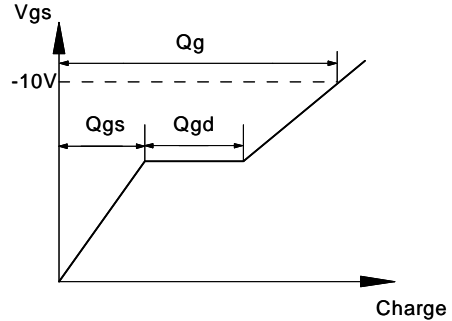
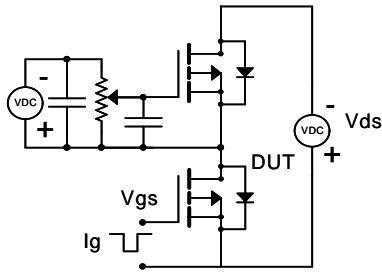
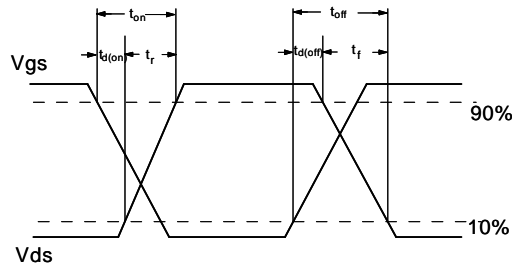
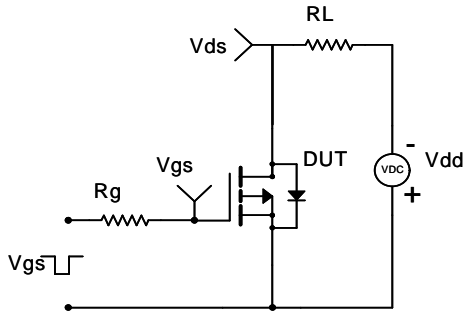


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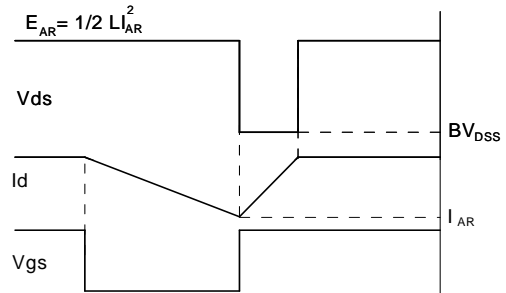
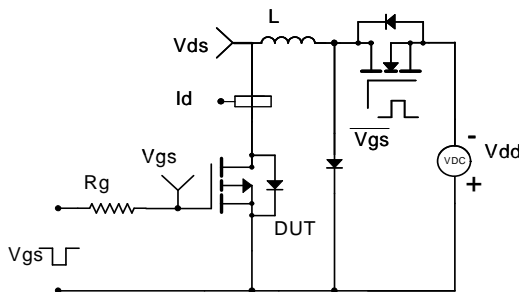
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

