HiPerClockS™ Application Note

3.3V LVPECL DRIVER TERMINATION

This application note provides termination examples for HiPerClockS™ 3.3V LVPECL drivers. The HiPerClockS™ 3.3V LVPECL driver is an open source/emitter driver as shown in Figure 1. Proper termination is required to ensure proper function of the device and signal integrity. There are many different termination schemes for the LVPECL drivers. This application note includes standard direct termination and AC coupled termination. The following termination approaches are only general recommendations under ideal conditions. Board designers should consult with their signal integrity engineers or verify through simulations in their system environment. The trace length and physical location of the components can affect signal integrity. The 50-Ohm transmission lines in the following diagrams indicate whether the components should be located near the driver or near the receiver.

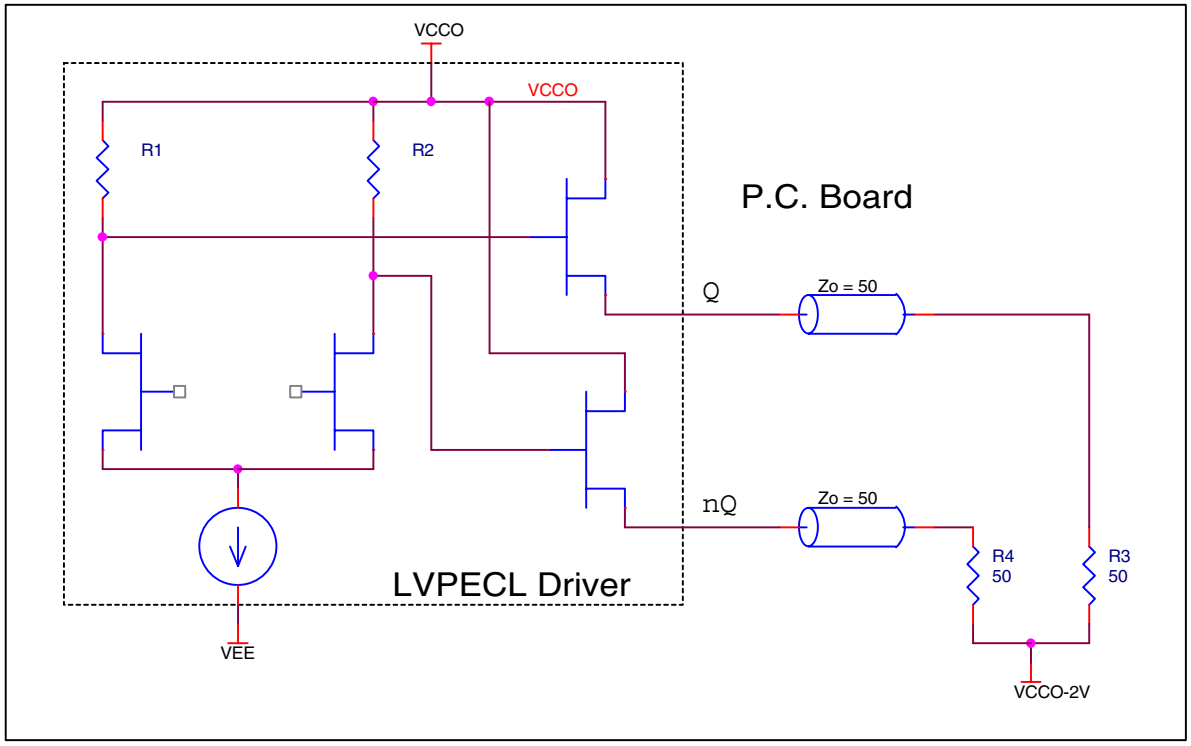


Figure 1 HiPerClockS™ LVPECL driver

Direct LVPECL Termination

The standard 3.3V LVPECL termination is shown in Figure 2. This termination scheme is used in characterization. The draw back of using this termination scheme in real applications is that it requires an additional power supply V_{CCO}-2V = 1.3V. In actual applications, the terminations shown in Figure 3 and Figure 4 are commonly used. These termination approaches eliminate the need of 1.3V power supply. In Figure 5, R1 and R2 located near the driver serve as current paths for the LVPECL outputs. The R3=100 Ohm located near the receiving serves as matched load termination for the transmission lines.

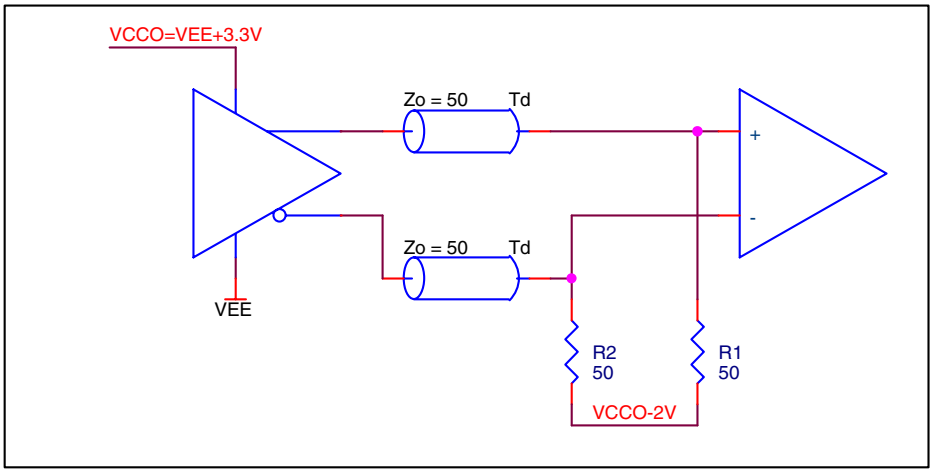


Figure 2 Standard 3.3V LVPECL Termination

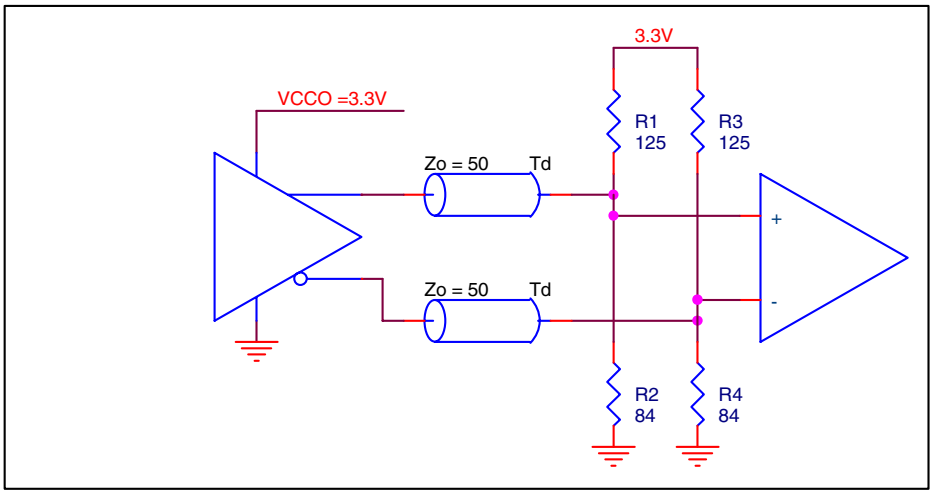


Figure 3 Equivalent 3.3V LVPECL Termination

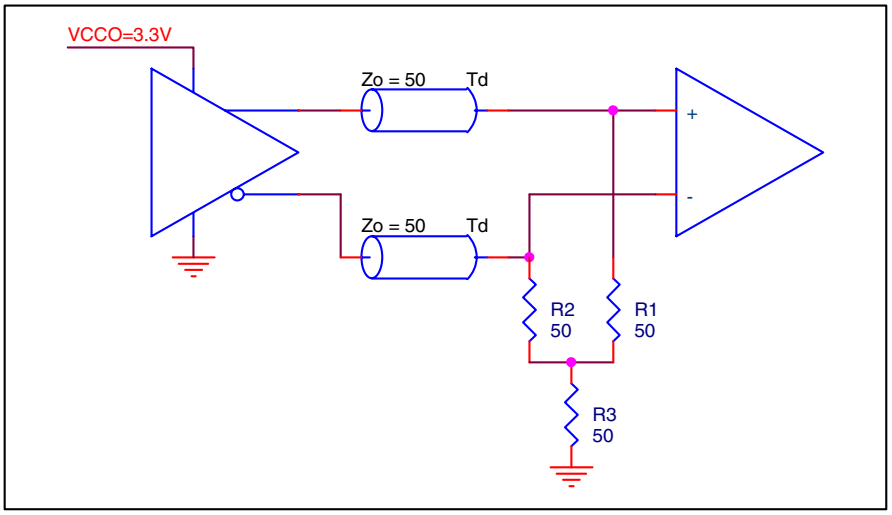


Figure 4 Equivalent 3.3V LVPECL Termination

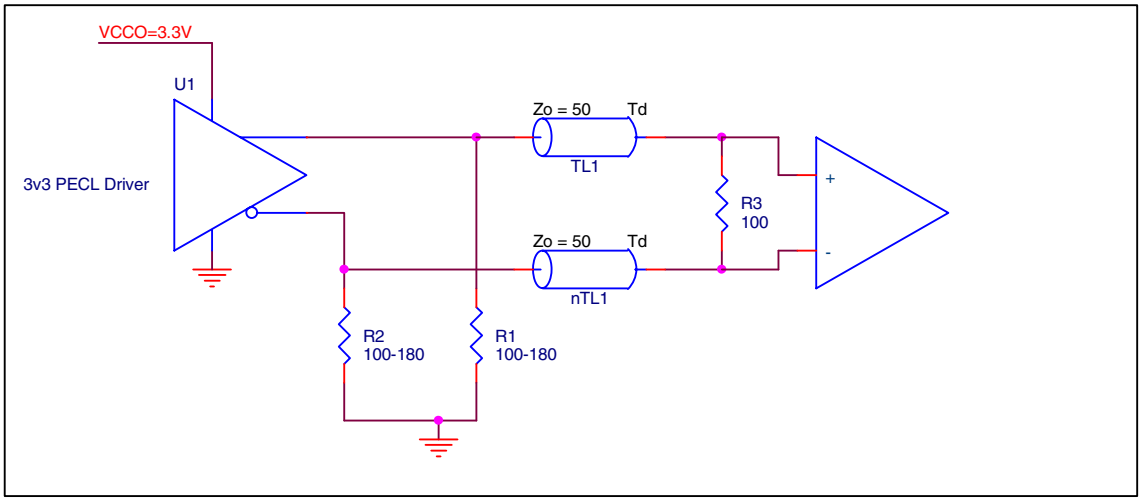


Figure 5 Termination with 100-Ohm resistor across the differential input

AC Coupled Termination

For AC termination, the offset level needs to be taken care of after the AC capacitors. A bias circuit might be required. The board design engineer needs to verify what type of receiver is being driven. A few examples of AC couple termination are shown in this section.

In Figure 6, the R3 and R4 at the driver pins provide a current path for the LVPECL driver. R1 and R2 serve as matched load termination. The power supply V_{BB} controls the offset level so that the signal offset fall within the VCMR input requirement of the receiver. Figure 7 and Figure 8 are equivalent to Figure 5. The Figure 7 is equivalent to $V_{BB}=V_{CC}-2V$. This offset is suitable for interfacing with HiPerClockS™ CLK/nCLK input. Figure 8 is equivalent to $V_{BB}=V_{CC}-1.3V$. This offset is suitable for interfacing with HiPerClockS™ PCLK/nPCLK input. Figure 9 shows AC termination with the offset bias voltage V_{BB} provided at the receiving end. Figure 10 shows AC termination with the offset bias voltage V_{BB} provided by the receiver device. In some cases, for the receiver with built-in bias resistors R1 and R2, the termination is shown in Figure 11.

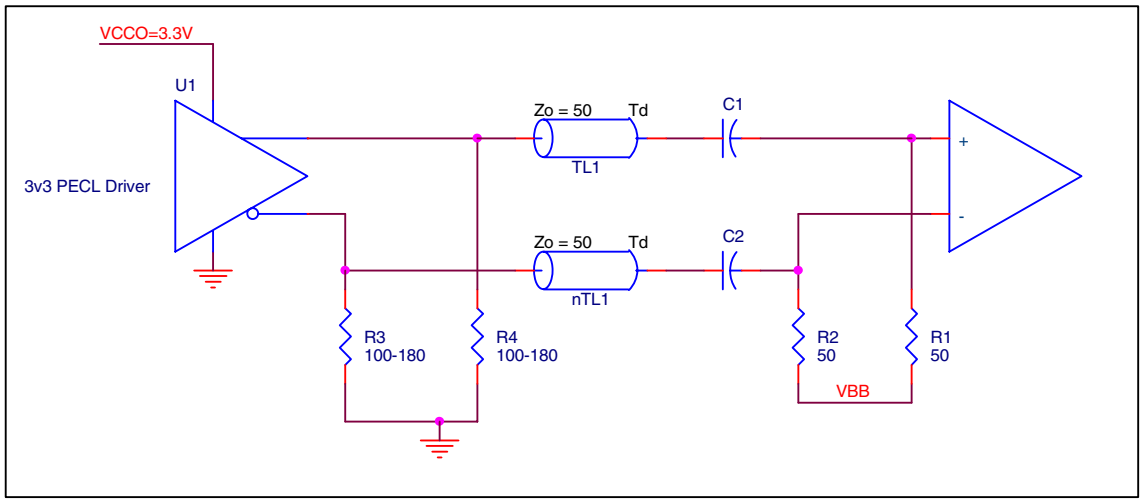


Figure 6 AC Coupled with V_{BB} power supply provided at the receiving end

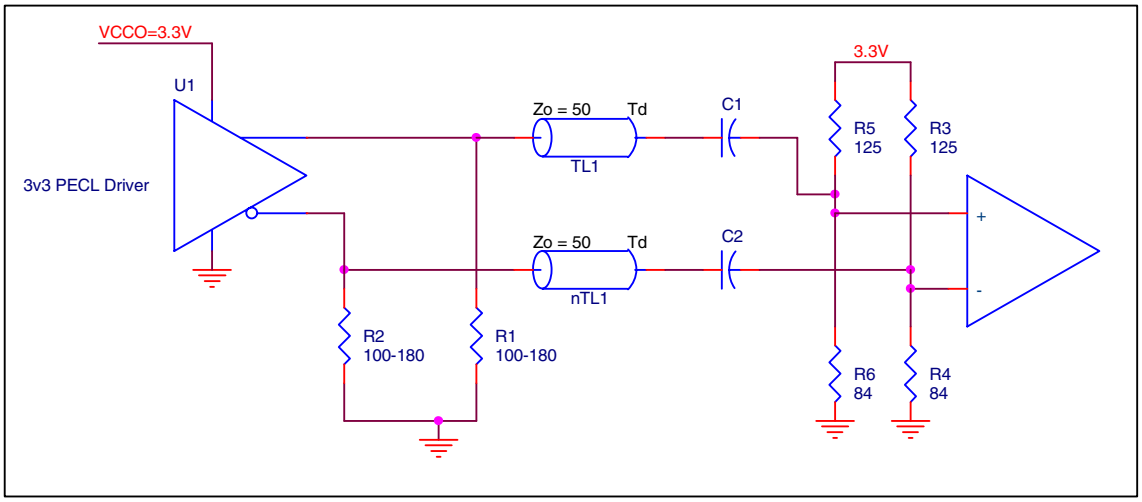


Figure 7 AC Coupled with bias offset at V_{cc} - 2V (Suitable for interface with HiPerClockS CLK/nCLK input)

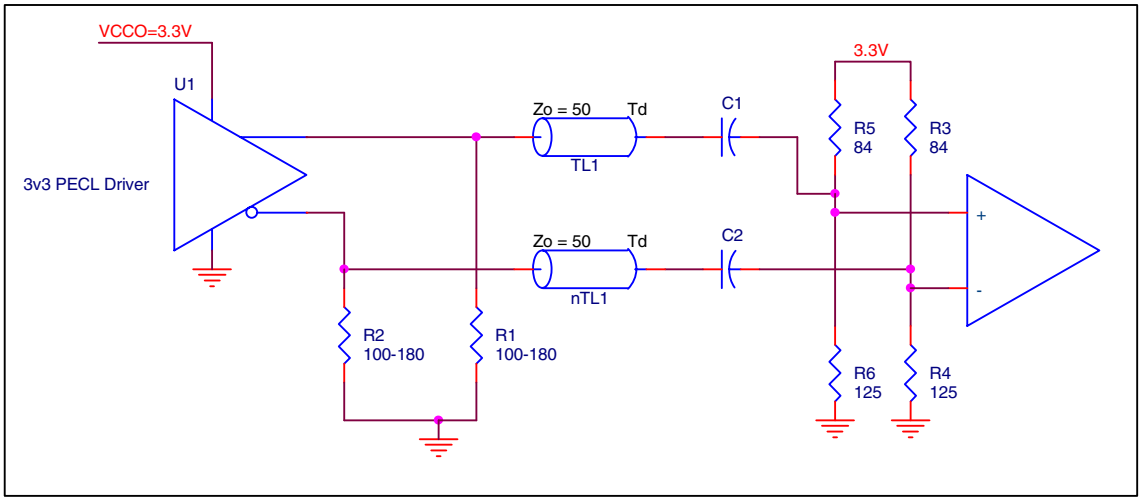


Figure 8 AC coupled with bias offset at V_{cc} - 1.3V (Suitable for AC Couple with ICS HiPerClockS PCLK/nPCLK input)

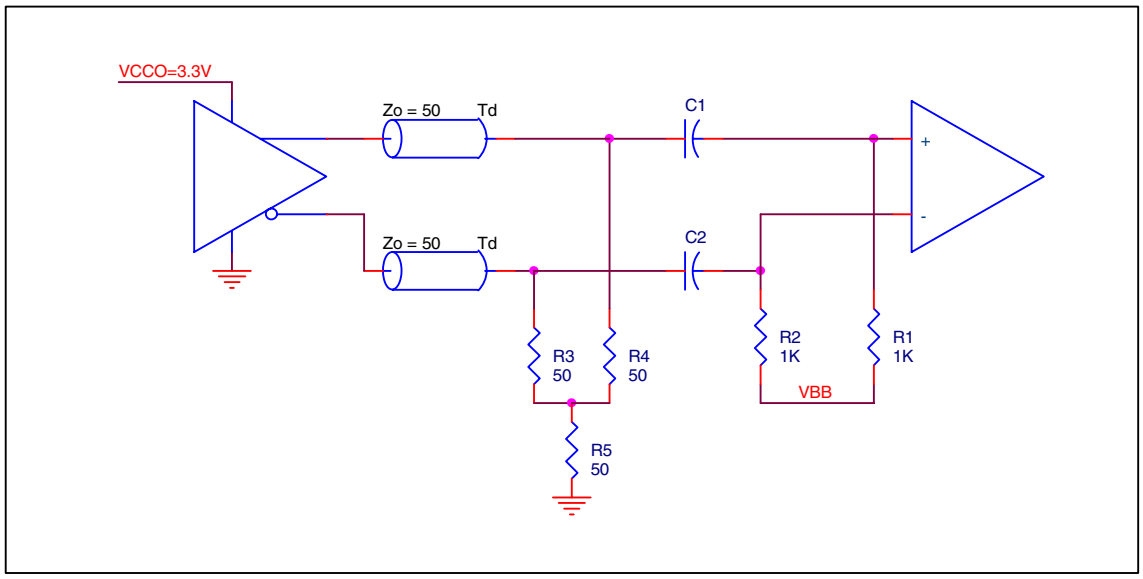


Figure 9 AC Coupled Termination with V_{BB} bias level provided at the receiver

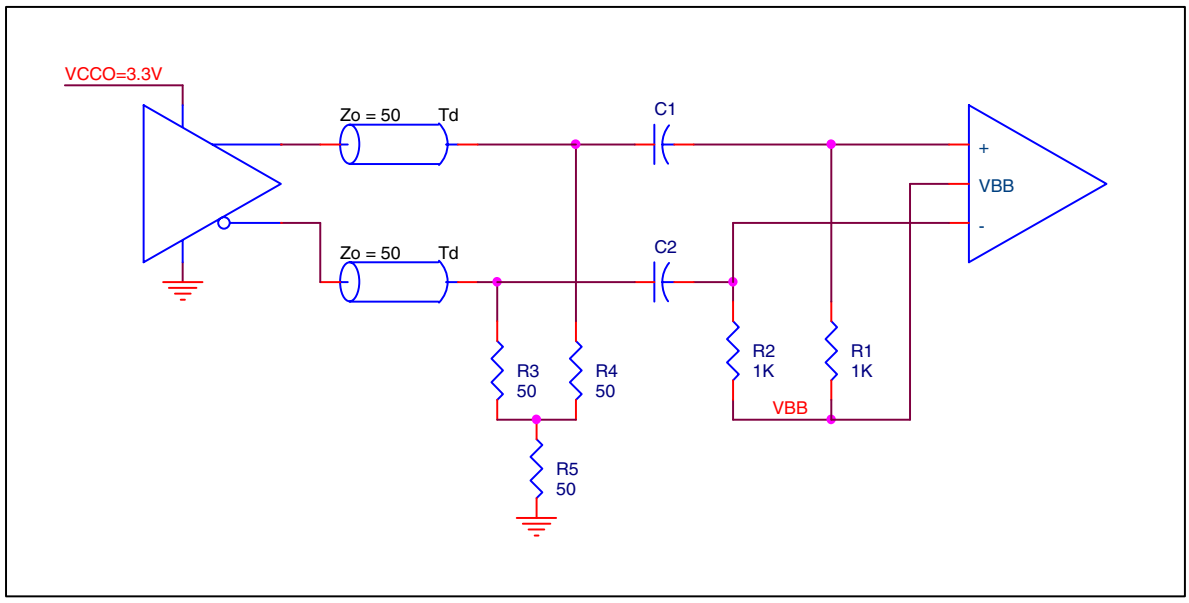


Figure 10 AC Coupled Termination with V_{BB} bias provided by the receiver

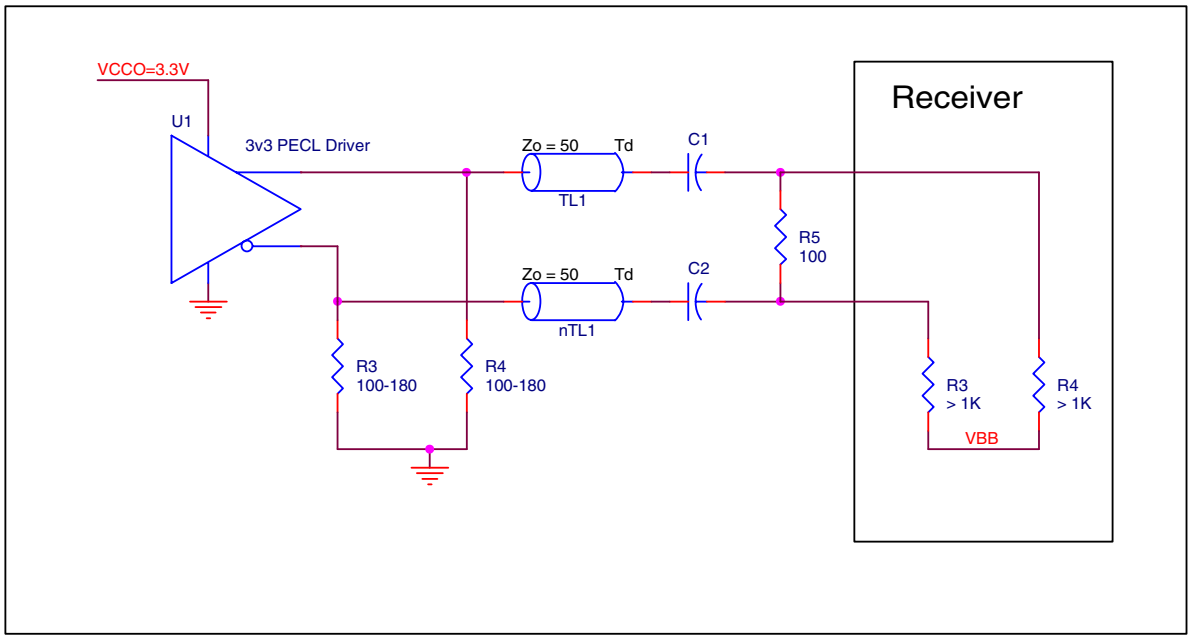


Figure 11 AC coupled for the receiver with built-in bias circuit