OLED Push Switches

64x48 Monochrome (0.66") OLED Switches Snap-In Type YOD2A

DISTINCTIVE CHARACTERISTICS

- Organic LED Technology
- Wide View Angle of 160°
- Exceptional Contrast and Brightness: 50times greater Brightness than previous LCD Products, four times more enhanced Resolution
- High Resolution provides sharp, clear Images of very small Characters
- Single Power / Built in DC to DC Converter for OEL Panel
- Distinct, Long travel of 5mm
- Sophisticated Housing for Assembly easily
- Support Parallel and Serial Interface

GERNERAL SPECIFICATIONS

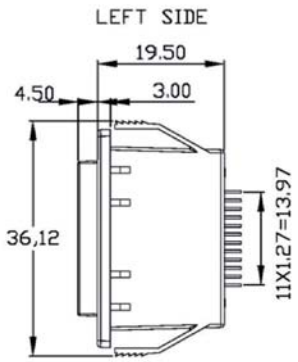
Dispaly Specifications
- Display Type: OLED
- Display Mode: Passive Matrix
- Display Color: ;onochrome (Blue Light)
- Drive Duty: 1/48 Duty
- Number of Pixels: 64x48
- Pixel Size: 0.19x0.19 mm
- Pixel Pitch: 0.21x0.21 mm
- Active Area: 13.42x10.06 mm

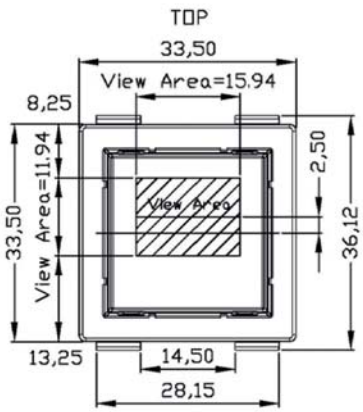
Mechanical Specifications
- Dimension: 33.50x36.12x24.0 mm (LxWxH)
- Window Size: 15.97x11.97 mm (LxW)
- Active Area: 13.42x10.06 mm
- Assembly: Pitch 1.27mm/12Pin Connector*2

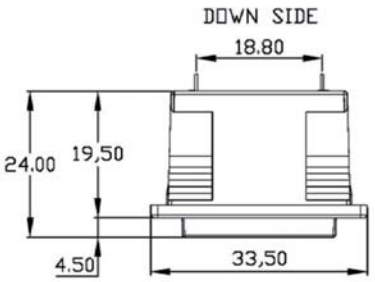
Assembly on PCB Easy & Removable & Flexible

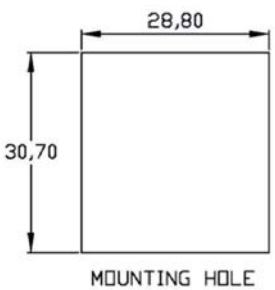
Electrical Characteristic
- Supply Voltage: 2.4 ~ 3.3 V
- Single Voltage Control Display Module
- Built-in DC to DC Power Supply to Drive OLED
- Driver IC: SSD1306
- Interface: Parallel/Serial/68xx/80xx/4-wire SPI/I^2C

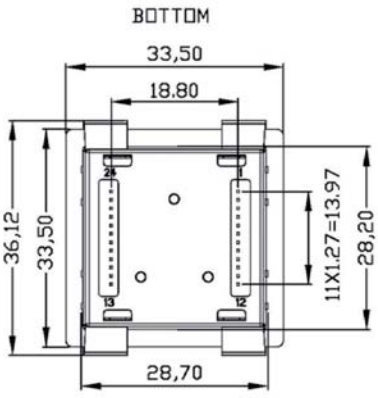
TYPICAL SWITCH DIMENSIONS











64x48 Monochrome (0.66") OLED Switches Snap-In Type YOD2A

PIN ASSIGNMENTS

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Type</th><th>Function</th></tr>
<tr><td>1</td><td>VDD</td><td>P</td><td>Power Supply for Core VDD
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>2</td><td>VSS</td><td>G</td><td>Ground for System
This is a ground pin. It must be connected to external source.</td></tr>
<tr><td>3</td><td>SW</td><td>I</td><td>Terminal of Switch Normally Open</td></tr>
<tr><td>4</td><td>SW</td><td>I</td><td>Terminal of Switch Normally Open</td></tr>
<tr><td>5
6</td><td>BS1
BS2</td><td>I</td><td>Communication Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>68XX-parallel</td><td>80XX-parallel</td><td>Serial</td><td>I²C</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>7</td><td>CS#</td><td>I</td><td>Chip Select
This is the chip select input. The chip is enable for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>8</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Drive
This is reset signal input. When the pin is low , initialization of the chip is executed.</td></tr>
<tr><td>9</td><td>D/C#</td><td>I</td><td>Data/ Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D0~D7 is treated as display data. When the pin is pulled low, the input at D0~D7 will be transferred to the command register.</td></tr>
<tr><td>10</td><td>W/R#
(R/W#)</td><td>I</td><td>Write or Read/Write Select
When 80xx interface mode is selected, the pin will be the Write (WR#) input.
When interfacing to a 68xx-series microprocessor, the pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.</td></tr>
<tr><td>11</td><td>RD#(E)</td><td>I</td><td>Read or Read/Write Enable
When 80xx interface mode is selected, the pin will be the Read (RD#) input.
When interfacing to a 68xx-series microprocessor, the pin will be used as the Enable (E) signal. Read/Write operation is initiated when this pin is pulled high and the CS# is pulled low.</td></tr>
<tr><td>12</td><td>NC</td><td>-</td><td>Reserved Pin</td></tr>
<tr><td>13~20</td><td>D0~D7</td><td>I</td><td>Host Data Input /Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and the D0 will be the serial clock input SCLK. When 12C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.</td></tr>
<tr><td>21</td><td>VSS</td><td>G</td><td>Ground for System
This is a ground pin. It must be connected to external source.</td></tr>
<tr><td>22</td><td>VCC-CTL</td><td>I</td><td>OLED Driver Power Supply ON/ OFF Control
When this pin is pulled high, the panel power supply will be turned ON.
When this pin is pulled low, the panel power supply will be turned OFF.</td></tr>
<tr><td>23</td><td>NC</td><td>-</td><td>Reserved Pin</td></tr>
<tr><td>24</td><td>VCC</td><td>P</td><td>Voltage Output High Level for COM Signal
This pin is OLED driver power supply. When VCC-CTL is pulled high, the pin will be output about 9V voltage (Built in Panel Power Supply).</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1,2
Supply Voltage for Display	Vcc	0	15	V	1,2
Operating Temperature	T_{OP}	-30	70	℃	-
Storage Temperature	T_{STG}	-40	80	℃	-

Note1：All the about voltages are on the basis of "VSS = 0V".

Note2：When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also for normal operations, it is desirable to use this module under the conditions according to Section 6. "Electrical Characteristics", if this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Characteristics	Symbol	Conditions	Min	TYP	Max	Unit
Supply Voltage for Logic	V_{DD}		2.4	2.8	3.5	V
Supply Voltage for Display	V_{CC}	Note 3	8.5	9	9.5	V
High Level Input	V_{IH}	Iout=100μA,3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	Iout=100μA,3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	Iout=100μA,3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	Iout=100μA,3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}	Note 4 Note 5	- -	180 180	300 300	μA μA
Operating Current for V_{CC}	I_{CC}	Note 4 Note 5	- -	1.5 2.5	2.2 3.5	mA mA
Sleep Mode Current for V_{DD}	I_{DD}, SLEEP		-	1	5	μA
Sleep Mode Current for V_{CC}	I_{CC}, SLEEP		-	1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{DD} = 2.8V, V_{CC} = 8.5V, 50% Display Area Turn on.
Note 5: V_{DD} = 2.8V, V_{CC} = 8.5V, 100% Display Area Turn on.

2. Optics Characteristics

Characteristics	Symbol	Conditions	Min	TYP	Max	Unit
Brightness	Lbr	With Polarizer (Note 3)	40	60	-	Cd/m^2
C.I.E.(Blue)	(x) (y)	Without Polarizer	0.12 0.22	0.16 0.26	0.20 0.30	Cd/m^2
Dark Room Contrast	CR		-	>2000:1	-	"Cd/m^2
View Angle			>160	-		degree

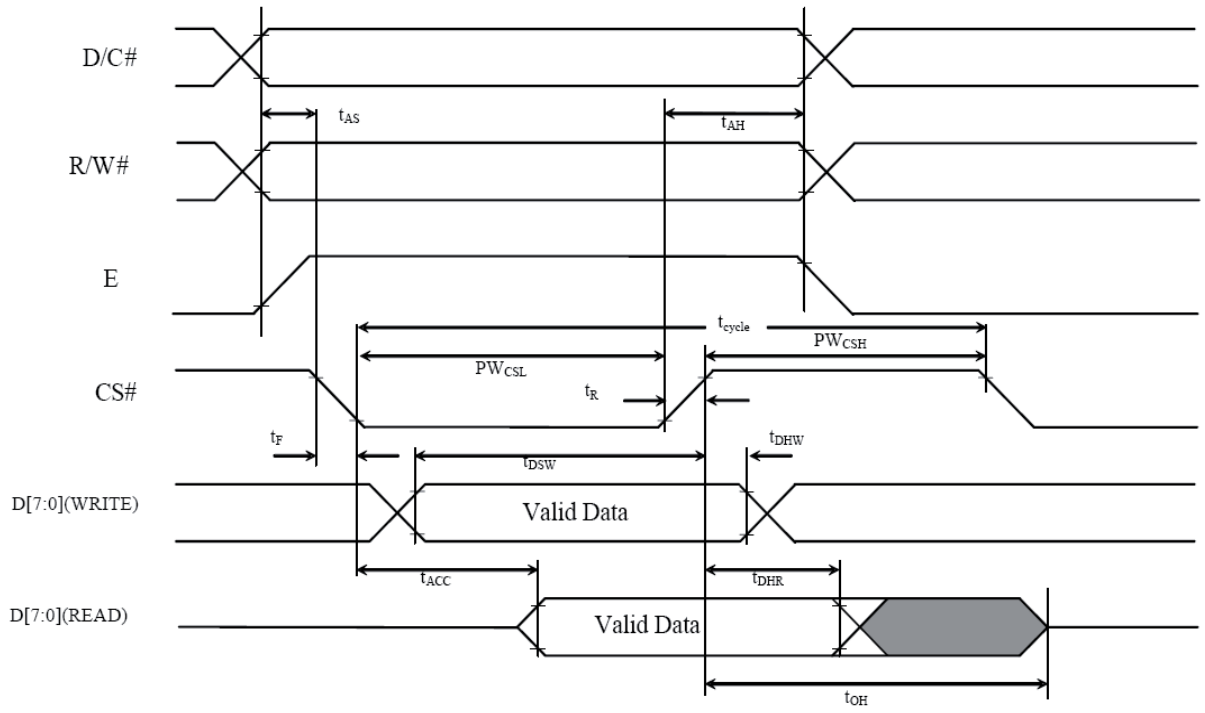
* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 8.5V

TIMING CHART

1. 68XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	System Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60	-	
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60	-	
t_R	Rise Time		15	ns
t_F	Fall Time		15	ns

*(VDD – VSS = 2.4V to 3.5V, Ta = 25℃)



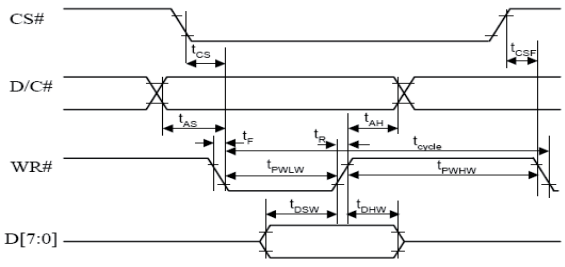
TIMING CHART

2. 80XX -Series MPU Parallel Interface Timing Characteristics

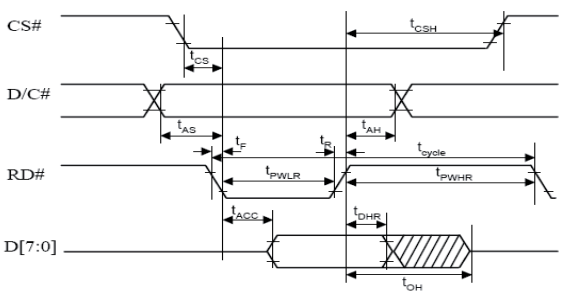
Symbol	Description	Min	Max	Unit
tcycle	Control Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60		ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time		15	ns
t_F	Fall Time		15	ns

*(V_{DD}-V_{SS}=2.4V to 3.5V, T_A=25°C)

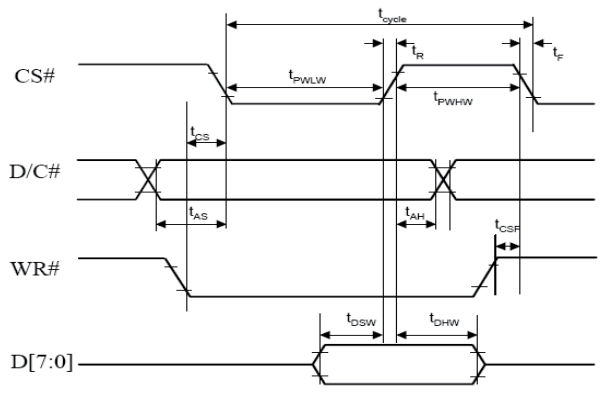
Write cycle (Form 1)



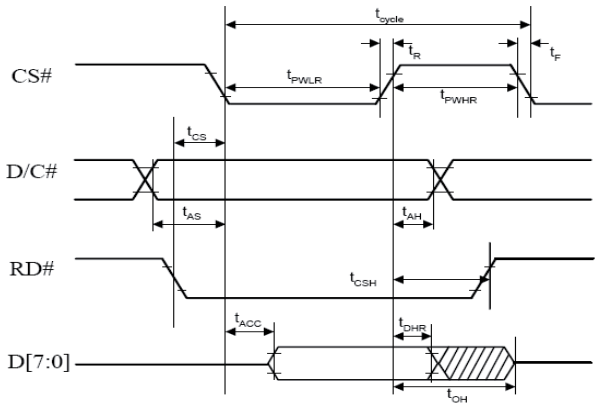
Read cycle (Form 1)



Write cycle (Form 2)



Read cycle (Form 2)

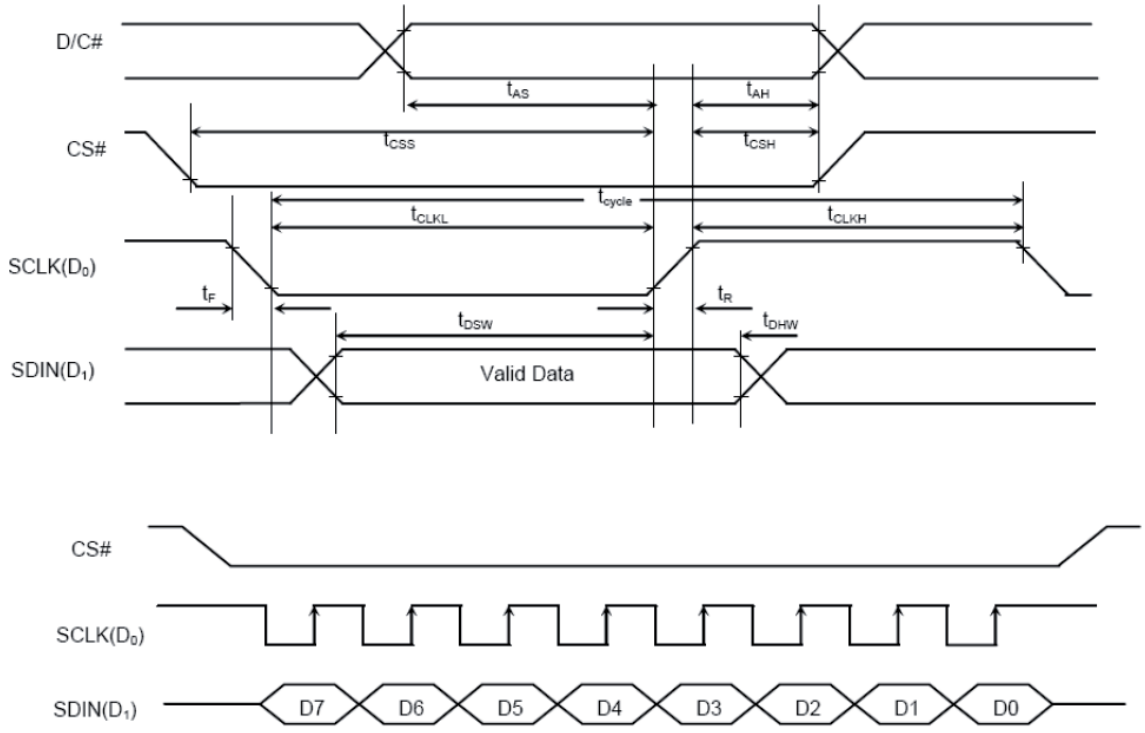


TIMING CHART

3 Series Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
tcss	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Tim	50	-	ns
t_{DHW}	Write Data Hold Tim	15	-	ns
t_{CLKL}	Serial Clock Low Time	100	-	ns
t_{CLKH}	Serial Clock High Time	100		ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

*(VDD – VSS = 2.4V to 3.5V, Ta = 25℃)

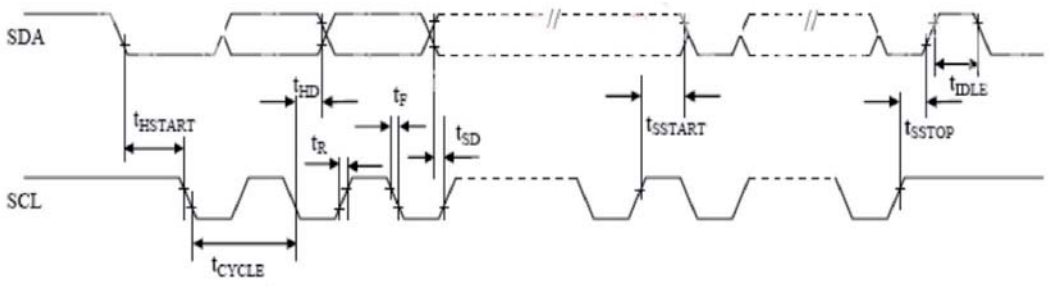


TIMING CHART

4 I²C Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3		us

*($V_{DD} - V_{SS}$ = 2.4V to 3.5V, Ta = 25℃)



FUNCTION SPECIFICATION

1 Command

Refer to the Technical Manual for the SSD1306 – Revision 1.2

2 Power Down and Power up Sequence

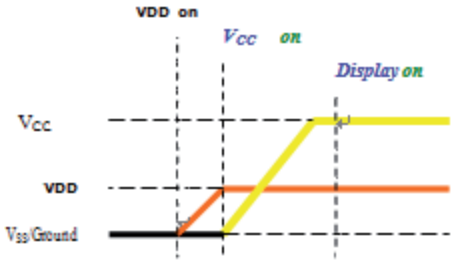
To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

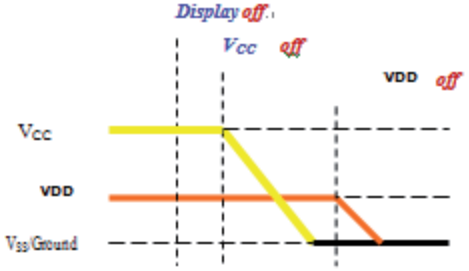
Power up Sequence

1. Power up V_{DD}
2. Send Display off Command
3. Initialization
4. Clear Screen
5. Power up Vcc
6. Delay 100ms (When V_{DD} is stable)
7. Send Display on Command

Power down Sequence

1. Send Display off command
2. Power down Vcc
3. Delay 100ms (When Vcc is reach 0 and panel is completely discharges)
4. Power down V_{DD}





3 Reset Status

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 132×64 Display mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h
9. Normal display mode (Equivalent to A4h command)

COMMAND APPLICATION EXAMPLE

Command usage and explanation of an actual example

<Initialization>

```
OLED_VCC_CTL=0;                 //Off power up Panel Vcc
OLED_RESET=0;                   //Reset driver IC for 100ms
Delay_100ms (1);
OLED_RESET=1;
Set_Display_Off (0xAE, 0x00);   // Display Off (0x00/0x01)
Set_Display_Clock (0xD5, 0x80); // Set Clock as 100 Frames/Sec
Set_Multiplex_Ratio(0xA8, 0x2F); // 1/48 Duty (0x0F~0x3F)
Set_Display_Offset(0xD3, 0x00); // Shift Mapping RAM Counter (0x00~0x3F)
Set_Start_Line(0x40,0x00);      // Set Mapping RAM Display Start Line 0x00~0x3F)
Set_Master_Config(0xAD, 0x8E);  // Disable Embedded DC/DC Converter
Set_Addressing_Mode(0x20, 0x02); // Set Page Addressing Mode
Set_Segment_Remap(0xA1,0x01);   // Set SEG/Column Mapping
Set_Common_Remap(0xC8);         // Set COM/Row Scan Direction
Set_Common_Config(0xDA, 0x12);  // Set Alternative Configuration
Set_Contrast_Control(0x81, 0xCF); // Set SEG Output Current
Set_Precharge_Period(0xD9, 0xD2); // Set Pre-Charge as 13 Clocks & Discharge as 2 Cock
Set_VCOMH(0xDB, 0x34);          // Set VCOM Deselect Level
Set_Entire_Display(0xA4);       // Disable Entire Display On (0x00/0x01)
Set_Inverse_Display(0xA6);      // Disable Inverse Display On (0x00/0x01)
Fill_RAM(0x00);                 // Clear Screen
OLED_VCC=1;                     //Power up Vcc
Delay_100ms(1);                 //Dealy 100ms
Set_Display_On(0xAF);           // Display On (0x00/0x01)
```

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

RELIABILITY

1 Contents of Reliability Test

Item	Conditions	Criteria
High Temperature Operation	70℃, 240hrs	The operational functions work
Low Temperature Operation	-30℃, 240hrs	
High Temperature Storage	80℃, 240hrs	
Low Temperature Storage	-40℃, 240hrs	
High Temperature / Humidity Operation	60℃, 90% RH, 120hrs	
Thermal Shock	-40℃<=>85℃, 24 cycles 60 mins dwell	

*The samples used for the above test do not include polarizer.

*No moisture condensation is observed during test.

2 Lifetime

End of lifetime is specified as 50% of initial brightness

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	60 cd/m^2, 50% checkerboard	*
Storage Life Time	20,000	-	hr	Ta = 25℃, 50% RH	

*The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2hrs prior to conducting the failure test at 23±5°C; 55±15% RH.