High Speed, Dual MOSFET Driver

Features

- 10ns average rise and fall time with 1000pF load
- 2.0A peak output source/sink current
- 1.8 to 5.0V input CMOS compatible
- 4.5 to 13V total supply voltage
- Dual matched channels
- Reduced clock skew
- Low input capacitance
- Green packaging

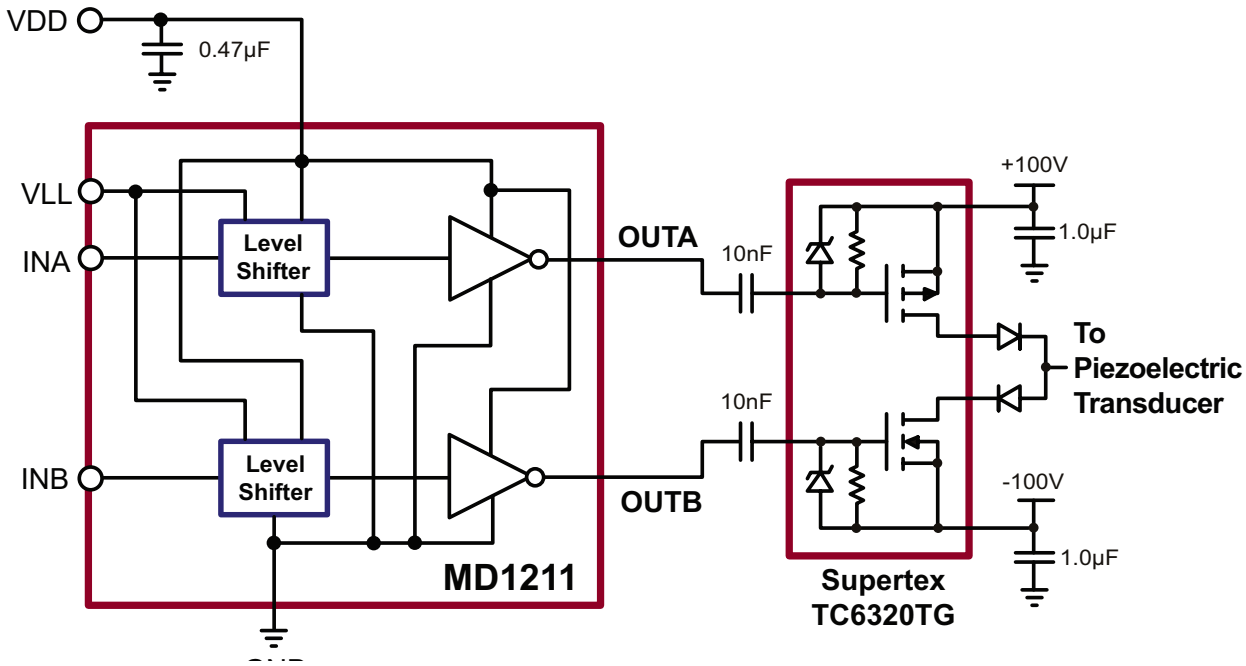
General Description

The Supertex MD1211 is a high speed dual MOSFET driver. It is designed to drive high voltage N and P-channel MOSFET transistors for medical ultrasound and other applications requiring a high output current for a capacitive load. The high-speed input stage of the MD1211 can operate from 1.8 to 5.0V logic interface with an optimum operating input signal range of 1.8 to 3.3V. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

Applications

- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Non-Destructive Testing (NDT)
- PIN diode driver
- High speed level translator
- Clock/line drivers

Typical Application Circuit

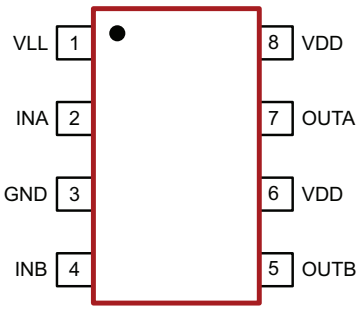


Ordering Information

Device	Package
	8-Lead SOIC (Narrow Body) *4.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*
MD1211	MD1211LG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



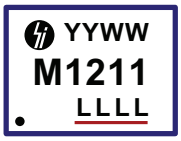
8-Lead SOIC (LG)
(top view)

Absolute Maximum Ratings

Parameter	Value
Logic supply voltage	-0.5V to +5.5V
Main supply voltage	-0.5V to +13.5V
Logic input levels	-0.5V to V_{LL}+0.5V
Maximum junction temperature	+125°C
Storage temperature	-65°C to +150°C
Operating temperature	-20°C to +85°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

DC Electrical Characteristics

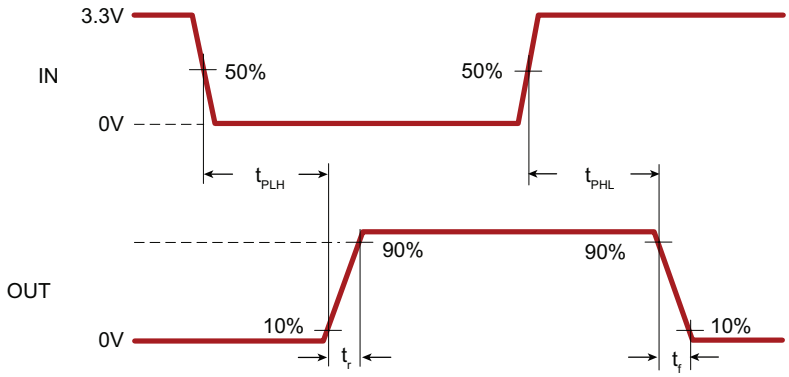
(Over operating conditions unless otherwise specified, V_{DD} = 12V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Main supply voltage	4.5	-	13	V	---
V_{LL}	Logic supply voltage	1.8	-	5.0	V	---
V_{IH}	Input logic voltage high	V_{LL} -0.3	-	V_{LL}	V	For Logic Inputs INA and INB
V_{IL}	Input logic voltage low	0	-	0.8	V	
I_{IH}	Input logic current high	-	-	10	µA	
I_{IL}	Input logic current low	-	-	10	µA	
C_{IN}	Logic input capacitance	-	5.0	10	pF	All Inputs
Outputs						
R_{SINK}	Output sink resistance	-	-	12	Ω	I_{SINK} = 50mA
R_{SOURCE}	Output source resistance	-	-	12	Ω	I_{SOURCE} = 50mA
I_{SINK}	Peak output sink current	-	2.0	-	A	---
I_{SOURCE}	Peak output source current	-	2.0	-	A	---

AC Electrical Characteristics

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{PLH}	Propagation delay when output is from low to high	-	10	-	ns	C_{LOAD} = 1000pF, (see timing diagram) Input signal rise/fall time 2ns
t_{PHL}	Propagation delay when output is from high to low	-	10	-	ns	
t_r	Output rise time	-	10	-	ns	
t_f	Output fall time	-	10	-	ns	
$\lvert t_r - t_f \rvert$	Rise and fall time matching	-	2.0	-	ns	For each channel
$\lvert t_{PLH} - t_{PHL} \rvert$	Propagation low to high and high to low matching	-	2.0	-	ns	
Δt_{dm}	Propagation delay match	-	3.0	-	ns	Device to device delay match

Timing Diagram



Power-Up Sequence

Step	Connection
1	VLL with logic signal low
2	VDD
3	Logic control signals

Power-Down Sequence

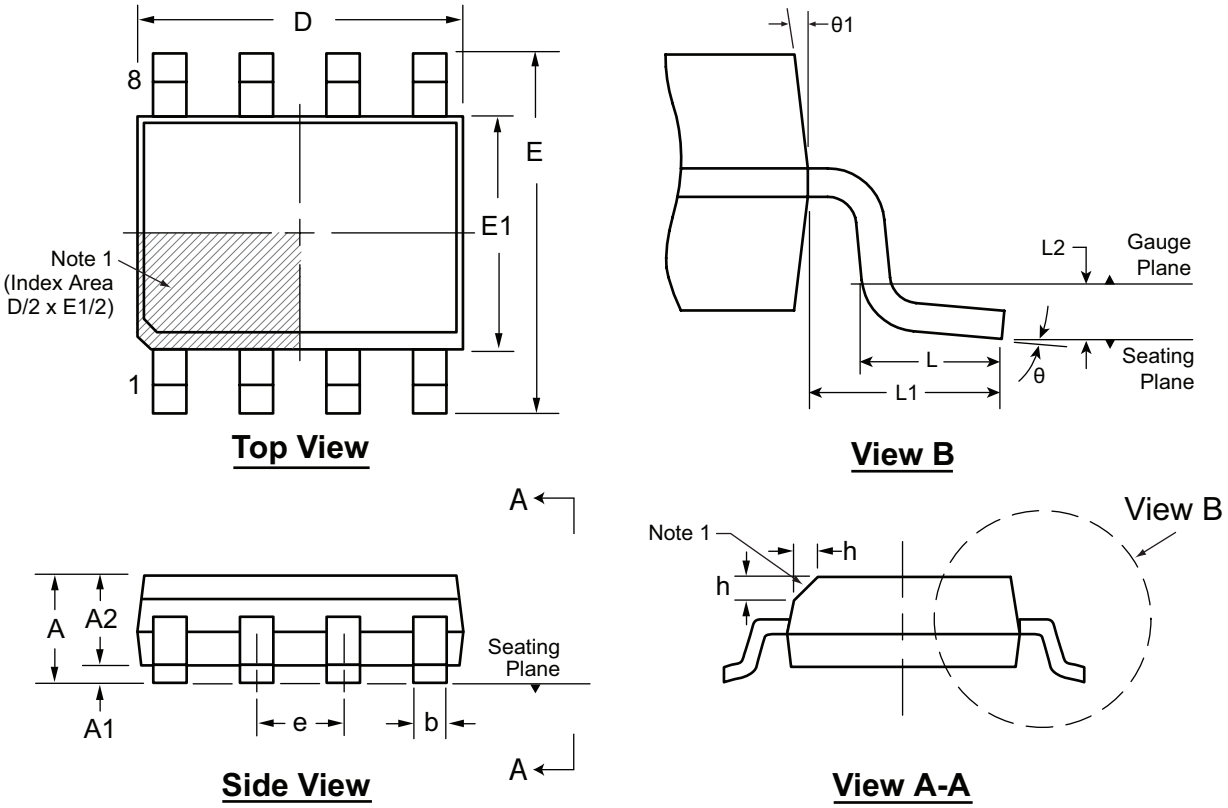
Step	Connection
1	All logic control signals go to low
2	VDD
3	VLL

Pin Description

Pin #	Name	Description
1	VLL	Logic supply voltage
2	INA	Logic input
3	GND	Device ground
4	INB	Logic input
5	OUTB	Output driver
6	VDD	Main supply voltage
7	OUTA	Output driver
8	VDD	Main supply voltage

8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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