Features

- ESD Protect for 4 high-speed I/O channels.
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±20kV (contact/air)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 30A (8/20μs)
  Cable Discharge Event (CDE)
- JEDEC SO-8 Package.
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V
- Fast turn-on and low clamping voltage.
- Low leakage current
- Low capacitance : 4pF typical
- Array of surge rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology.
- ***Green Part.***

Applications

- T1/E1 secondary IC side protection
- T3/E3 secondary IC side protection
- HDSL, SDSL secondary IC side protection
- WAN/LAN Device
- 10/100/1000 Ethernet
- Video lines protection
- Base stations
- I^2C Bus protection

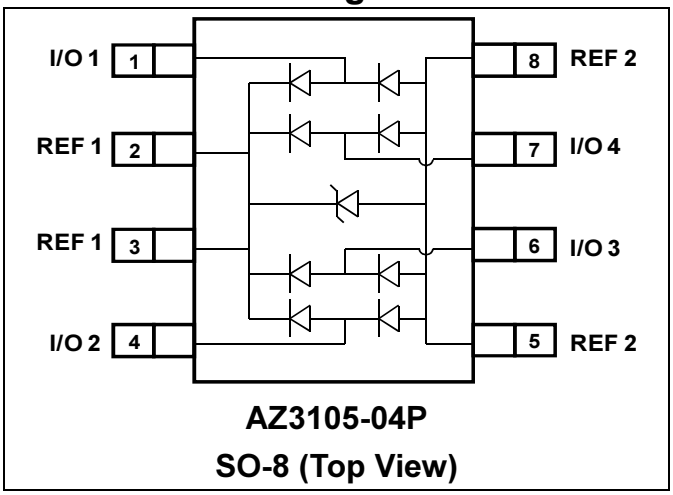
Description

AZ3105-04P is a high performance design which includes surge rated diode arrays. The AZ3105-04P family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZ3105-04P is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

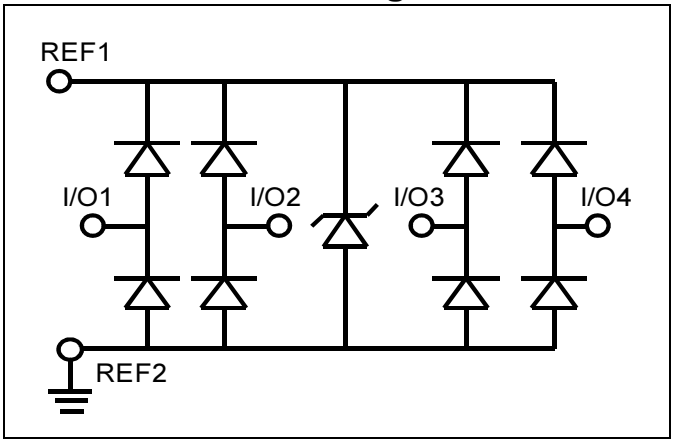
AZ3105-04P may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Pin Configuration



AZ3105-04P
SO-8 (Top View)

Circuit Diagram



SPECIFICATIONS

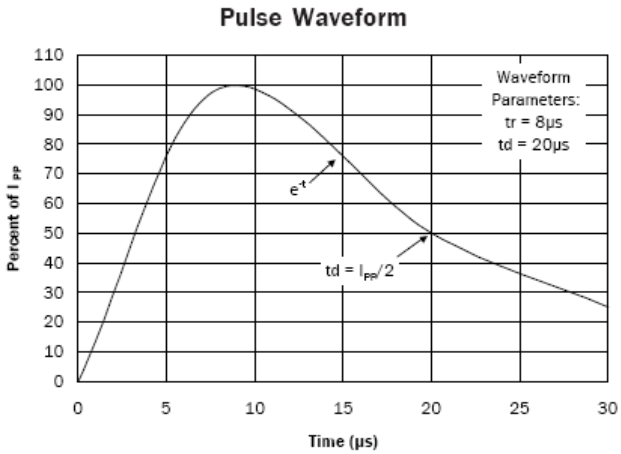
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs) for each differential line pair	I_{PP}	30	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact) for each differential line pair	V_{ESD}	±20 ±20	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

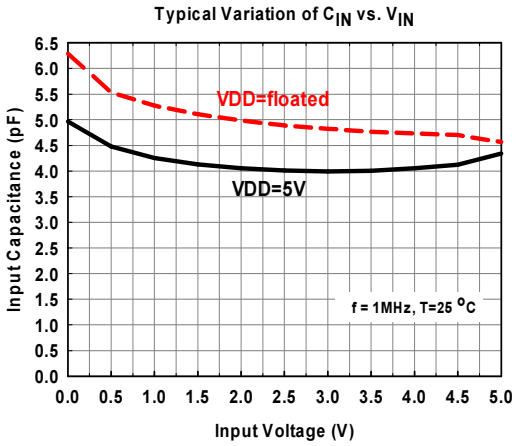
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	REF1 to REF2, T=25 °C			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, REF1 to REF2			5	μA
Channel Leakage Current	$I_{CH-Leak}$	V_{REF1} = 5V, V_{REF2} = 0V, T=25 °C, Any Channel pin to REF2			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, REF1 to REF2	6		9.5	V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, REF2 to REF1		0.8	1.2	V
ESD Clamping Voltage –I/O (Note 1)	V_{clamp_io}	IEC 61000-4-2 +8kV, T=25 °C, Contact mode, any Channel pin to REF2		9.0		V
ESD Clamping Voltage –VDD (Note 1)	V_{clamp_VDD}	IEC 61000-4-2 +8kV, T=25 °C, Contact mode, REF1 to REF2		7.5		V
ESD Dynamic Turn on Resistance –I/O	$R_{dynamic\_io}$	IEC 61000-4-2 0~+8kV,T=25 °C, Contact mode, any Channel pin to REF2		0.15		Ω
ESD Dynamic Turn on Resistance –VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, REF1 to REF2		0.09		Ω
Surge Clamping Voltage	$V_{CL-Surge}$	I_{PP}=5A, tp=8/20μs, T=25 °C, any Channel pin to REF2		7.3		V
Surge Clamping Voltage	$V_{CL-Surge}$	I_{PP}=10A, tp=8/20μs, T=25 °C, any Channel pin to REF2		8		V
Surge Clamping Voltage	$V_{CL-Surge}$	I_{PP}=30A, tp=8/20μs, T=25 °C, any Channel pin to REF2		10.9		V
Channel Input Capacitance -1	C_{IN-1}	**V_{REF1} =5V,** V_{REF2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, any Channel pin to REF2		4.0	4.6	pF
Channel Input Capacitance - 2	C_{IN-2}	**V_{REF1}=floated**, V_{REF2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, any Channel pin to REF2		5.0	5.5	pF

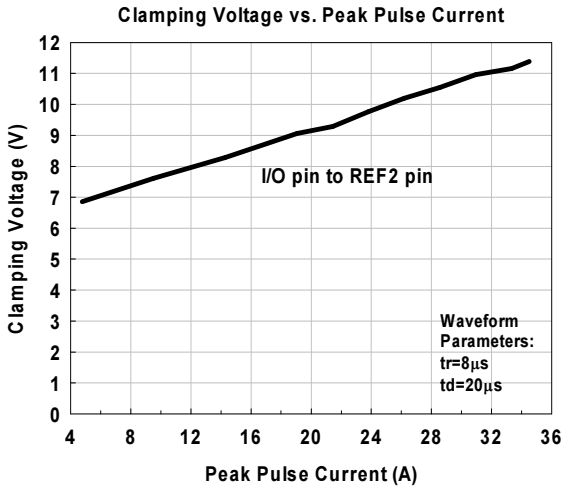
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

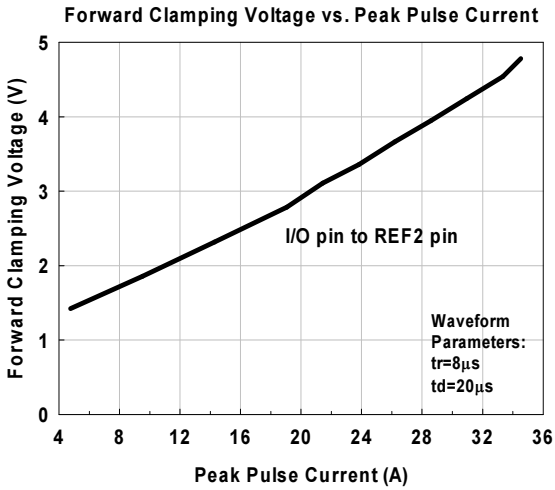
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

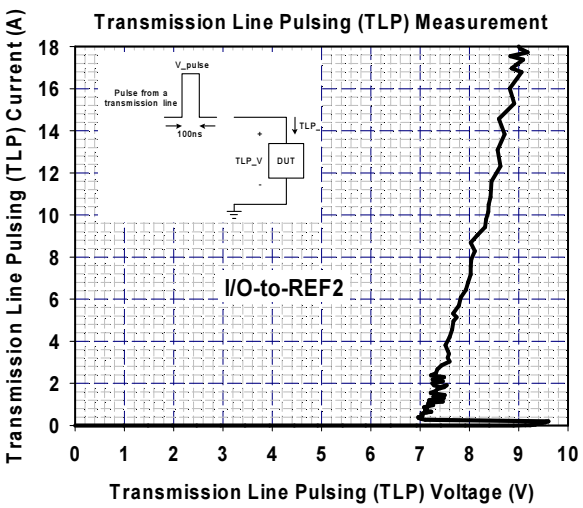
Typical Characteristics

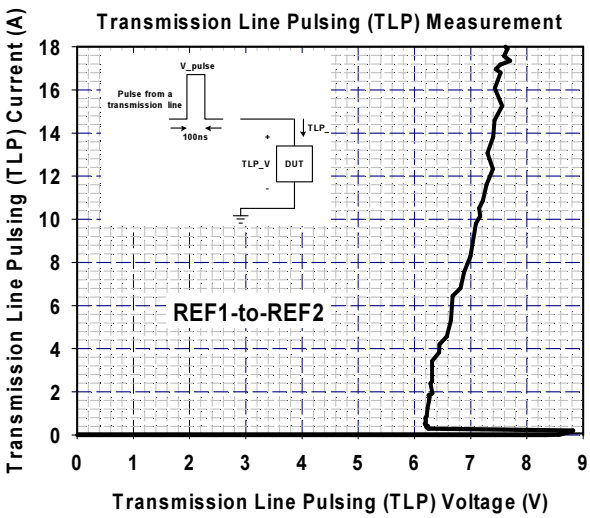












Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or 30/(1x10-9). So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZ3105-04P has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

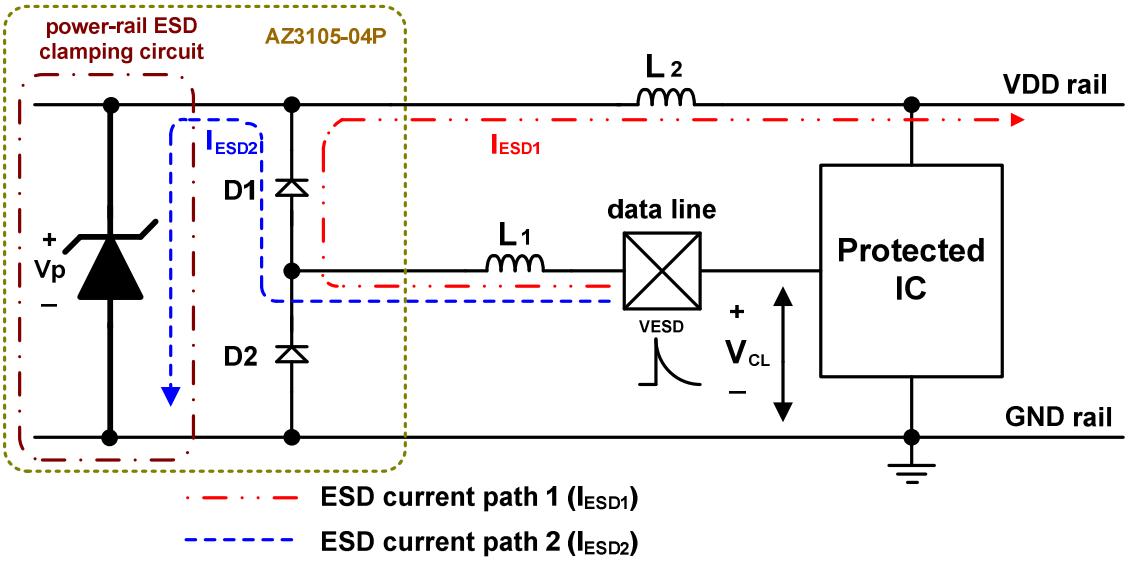


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZ3105-04P is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZ3105-04P is shown in the Fig. 2. In Fig. 2, the four protected data lines are connected to the ESD protection pins (pin1, pin4, pin6, and pin7) of AZ3105-04P. The ground pin (REF2) of AZ3105-04P is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (REF1) of AZ3105-04P is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ3105-04P.

AZ3105-04P can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ3105-04P.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (REF1) of AZ3105-04P can be left as floated. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

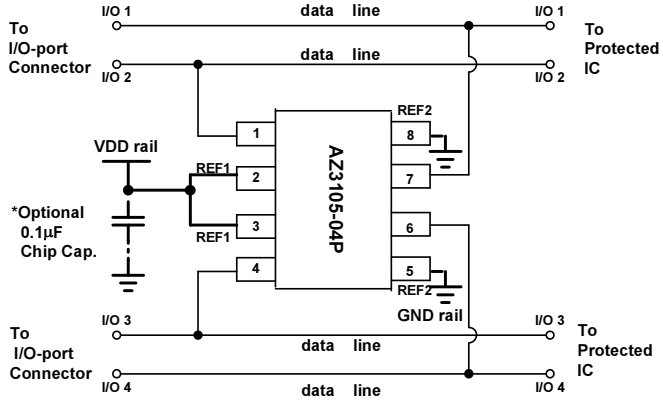


Fig. 2 Data lines and power rails connection of AZ3105-04P.

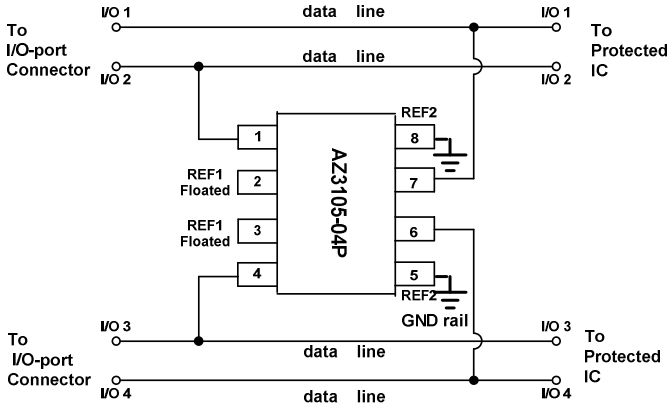


Fig. 3 Data lines and power rails connection of AZ3105-04P. REF1 is left as floating when no power rail presented on the PCB.

C. Applications

T1/E1 Interface Protection

The AZ3105-04P can be used as secondary IC side protection in T1/E1 interface. The ESD / Surge protection scheme for T1/E1 transceiver is shown in Fig. 3. Each data line (RTIP/RRING/TTIP/TRING) of T1/E1 transceiver is connected to the ESD protection pin of AZ3105-04P.

When ESD or Surge voltage pulse appears on the data line, the ESD / Surge pulse current will be conducted by AZ3105-04P away from the T1/E1 transceiver IC. Therefore, the common mode (Line-to-Ground) protection of T1/E1 interface is complementally protected with an AZ3105-04P.

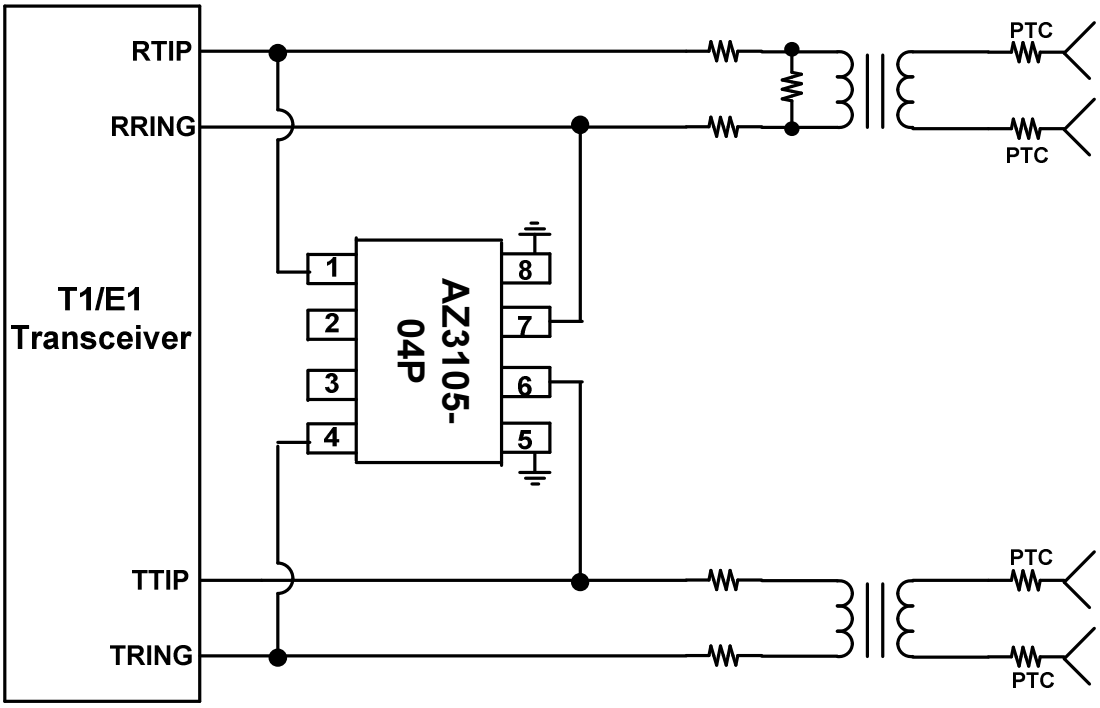


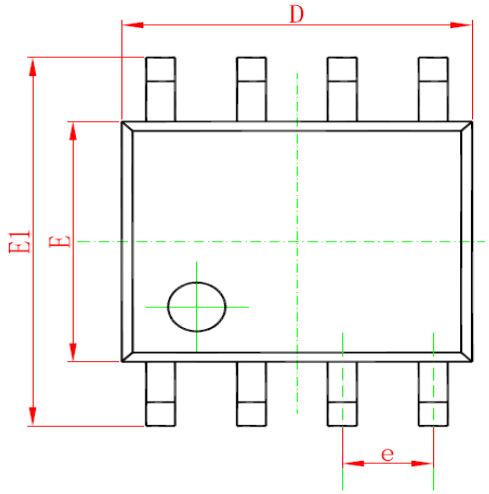
Fig. 3 Secondary side ESD Protection scheme for T1/E1 interface by using AZ3105-04P.

Mechanical Details

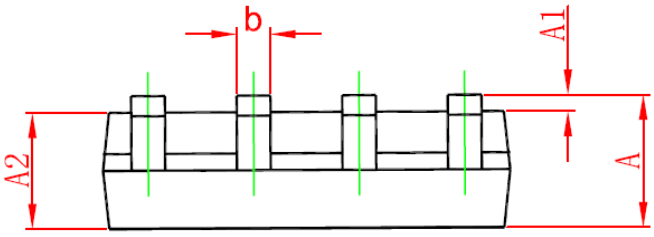
SO-8

PACKAGE DIAGRAMS

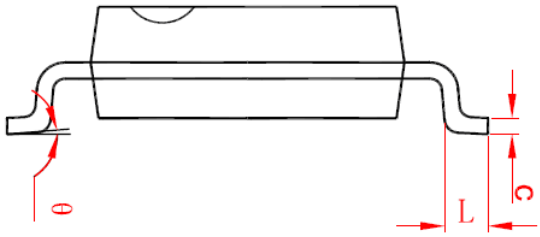
TOP VIEW



SIDE VIEW



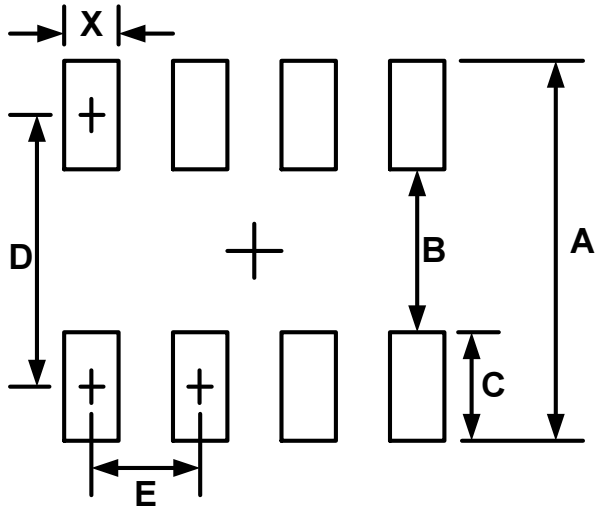
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	min	max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.049	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
Θ	0	8	0	8

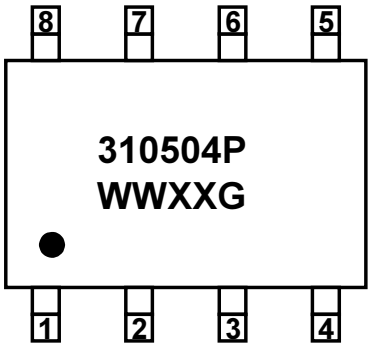
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	7.40	0.291
B	3.00	0.118
C	2.20	0.087
D	5.20	0.205
E	1.27	0.050
X	0.60	0.24

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



310504P = Device Code
WW = Date Code
XX = Control Code
G = Green Part Indication

Part Number	Marking Code
AZ3105-04P.RDG (Green Part)	**310504P WWXXG**

Note : Green means Pb-free, RoHS, and Halogen free compliant

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ3105-04P.RDG	Green	T/R	13 inch	2,500/reel	1 reel=2,500/box	5 boxes=12,500/carton

Revision History

Revision	Modification Description
Revision 2014/04/22	Preliminary Release.
Revision 2016/01/07	Update the description of marking code.
Revision 2017/05/11	Formal Release.