AK4383

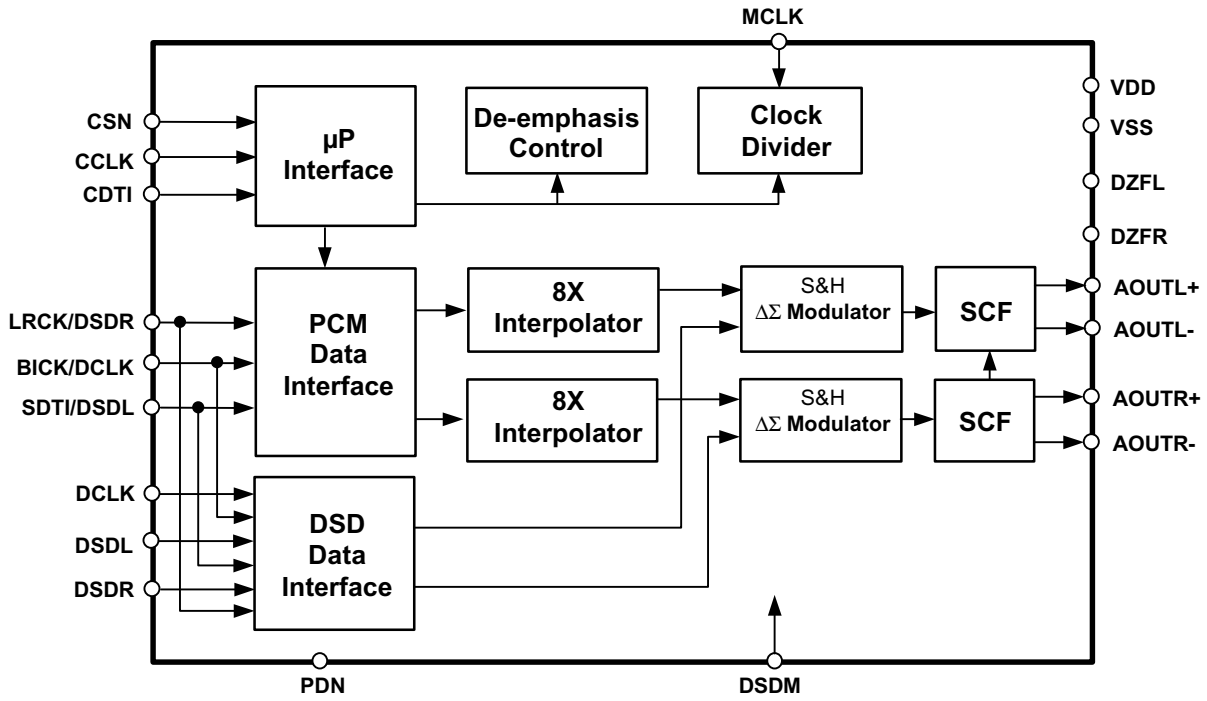
192kHz 24-Bit 2ch ΔΣ DAC with DSD input

GENERAL DESCRIPTION

The AK4383 offers the perfect mix for cost and performance based audio systems. Using AKM's multi bit architecture for its modulator the AK4383 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4383 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4383 accepts 192kHz PCM data and 1-Bit DSD data, ideal for a wide range of applications including DVD-Audio and SACD. The AK4383 is offered in a space saving 20pin TSSOP package.

FEATURES

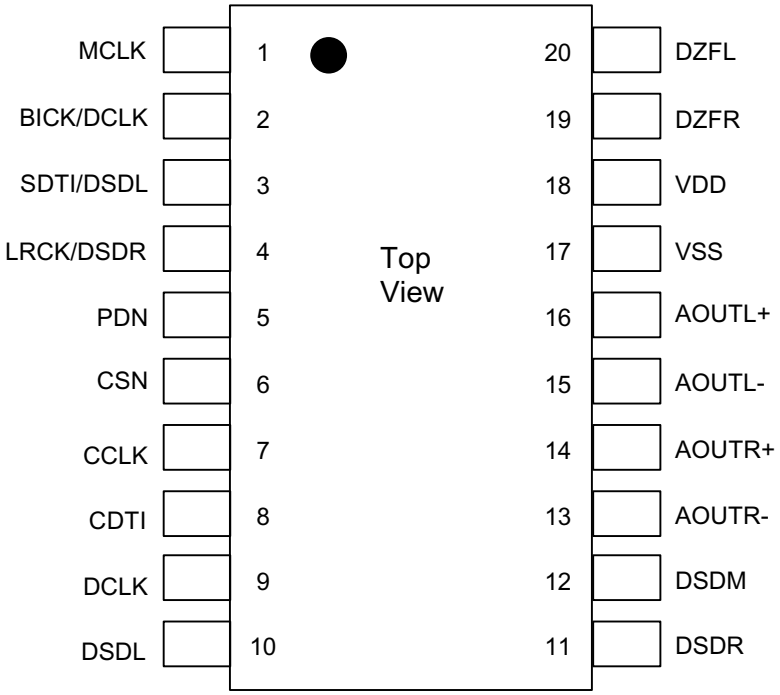
- ☐ **Sampling Rate Ranging from 8kHz to 192kHz**
- ☐ **24-Bit 8 times FIR Digital Filter**
- ☐ **On chip SCF**
- ☐ **Digital de-emphasis for 32k, 44.1k and 48kHz sampling**
- ☐ **Soft mute**
- ☐ **Digital Attenuator (Linear 256 steps)**
- ☐ **PCM I/F format: 24-Bit MSB justified, 24/20/16-Bit LSB justified or I^2S**
- ☐ **Master clock: 256fs, 384fs, 512fs or 768fs (PCM Normal Speed Mode)**
  128fs, 192fs, 256fs or 384fs (PCM Double Speed Mode)
  128fs or 192fs (PCM Quad Speed Mode)
  512fs or 768fs (DSD Mode)
- ☐ **THD+N: -94dB**
- ☐ **Dynamic Range: 110dB**
- ☐ **DSD Data Input Mode**
- ☐ **High Tolerance to Clock Jitter**
- ☐ **Power supply: 4.75 to 5.25V**
- ☐ **Very Small Package: 20pin TSSOP (0.65mm pitch)**
- ☐ **AK4382 Pin Compatible**



■ Ordering Guide

AK4383VT	-40 ~ +85°C	20pin TSSOP (0.65mm pitch)
AKD4383	Evaluation Board for AK4383	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK/DCLK	I	Audio Serial Data Clock Pin / DSD Clock Pin
3	SDTI/DSDL	I	Audio Serial Data Input Pin / DSD Lch Data Input Pin
4	LRCK/DSDR	I	L/R Clock Pin / DSD Rch Data Input Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4383 is in the power-down mode and is held in reset. The AK4383 should always be reset upon power-up.
6	CSN	I	Chip Select Pin
7	CCLK	I	Control Data Input Pin
8	CDTI	I	Control Data Input Pin in serial mode
9	DCLK	I	DSD Clock Pin (Pull-down Pin)
10	DSDL	I	DSD Lch Data Input Pin (Pull-down Pin)
11	DSDR	I	DSD Rch Data Input Pin (Pull-down Pin)
12	DSDM	I	DSD Mode Enable Pin (Pull-down Pin) "0": PCM data is input from Pin 2-4. And the mode can be switched between PCM and DSD mode by register. "1": DSD data is input from Pin 9-11.
13	AOUTR-	O	Rch Negative Analog Output Pin
14	AOUTR+	O	Rch Positive Analog Output Pin
15	AOUTL-	O	Lch Negative Analog Output Pin
16	AOUTL+	O	Lch Positive Analog Output Pin
17	VSS	-	Ground Pin
18	VDD	-	Power Supply Pin
19	DZFR	O	Rch Data Zero Input Detect Pin
20	DZFL	O	Lch Data Zero Input Detect Pin

Note: All input pins except pull-up pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	6.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	4.75	5.0	5.25	V

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=5.0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data;
Measurement frequency=20Hz ~ 20kHz; R_L ≥2kΩ; PCM Mode; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 3)						
THD+N	fs=44.1kHz	0dBFS		-94	-87	dB
	BW=20kHz	-60dBFS		-48	-	dB
	fs=96kHz	0dBFS		-92	-84	dB
	BW=40kHz	-60dBFS		-45	-	dB
	fs=192kHz	0dBFS		-92	-	dB
	BW=40kHz	-60dBFS		-45	-	dB
Dynamic Range (-60dBFS with A-weighted) (Note 4)			102	110		dB
S/N (A-weighted) (Note 5)			102	110		dB
Interchannel Isolation (1kHz)			90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DC Accuracy						
Gain Drift				100	-	ppm/°C
Output Voltage (Note 6)			±2.3	±2.5	±2.7	Vpp
Load Resistance (Note 7)			2			kΩ
Power Supplies						
Power Supply Current (VDD)						
Normal Operation (PDN = "H", fs≤96kHz)				20	34	mA
Normal Operation (PDN = "H", fs=192kHz)				25	42	mA
Power-Down Mode (PDN = "L") (Note 8)				10	100	μA

Notes: 3. Measured by Audio Precision (System Two). Refer to the evaluation board manual.
4. 100dB at 16bit data.
5. S/N does not depend on input bit length.
6. Full-scale voltage (0dB). Output voltage scales with the voltage of VREF,
AOUT (typ.@0dB)=(AOUT+)-(AOUT-)=±2.5Vpp × VREF/5.
7. For AC-load. 4kΩ for DC-load.
8. All digital inputs including clock pins (MCLK, BICK and LRCK) are held VDD or VSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.75 ~ 5.25V; fs = 44.1kHz; DEM = OFF; SLOW= "0"; PCM Mode)

Parameter			Symbol	min	typ	max	Units
Digital filter							
Passband	±0.05dB (Note 9)		PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband	(Note 9)		SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay	(Note 10)		GD	-	19.3	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	± 0.2	-	dB
	40.0kHz	fs=96kHz	FR	-	± 0.3	-	dB
	80.0kHz	fs=192kHz	FR	-	+0/-0.6	-	dB

Notes: 9. The passband and stopband frequencies scale with fs(system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

10. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75~5.25V; fs = 44.1kHz; DEM = OFF; SLOW = "1"; PCM Mode)

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.04dB (Note 11)		PB	0		8.1	kHz
	-3.0dB			-	18.2	-	kHz
Stopband	(Note 11)		SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay	(Note 10)		GD	-	19.3	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0/-5	-	dB
	40.0kHz	fs=96kHz	FR	-	+0/-4	-	dB
	80.0kHz	fs=192kHz	FR	-	+0/-5	-	dB

Note: 11. The passband and stopband frequencies scale with fs.
For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS

(Ta=25°C; VDD=4.75 ~ 5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
High-Level Output Voltage	(Iout=-80μA)	VOH	VDD-0.4	-	-	V
Low-Level Output Voltage	(Iout=80μA)	VOL	-		0.4	V
Input Leakage Current	(Note 12)	Iin	-	-	± 10	μA

Note: 12. DSDM, DCLK, DSDL and DSDR pins have internal pull-down devices, nominally 100kΩ.

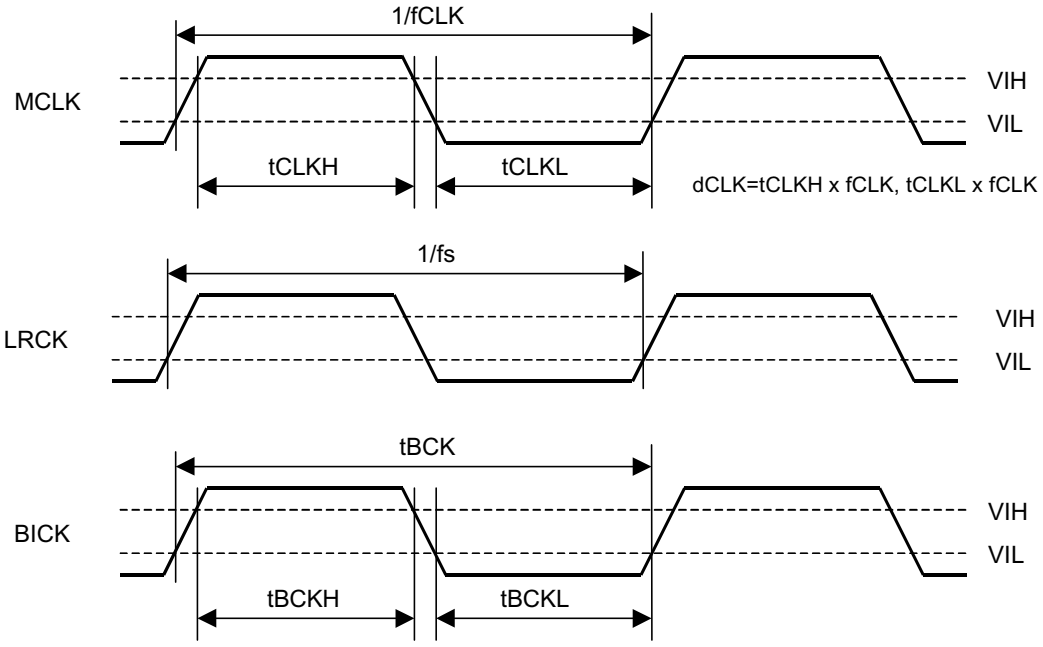
SWITCHING CHARACTERISTICS

(Ta = 25°C; VDD = 4.75 ~ 5.25V; C_L = 20pF)

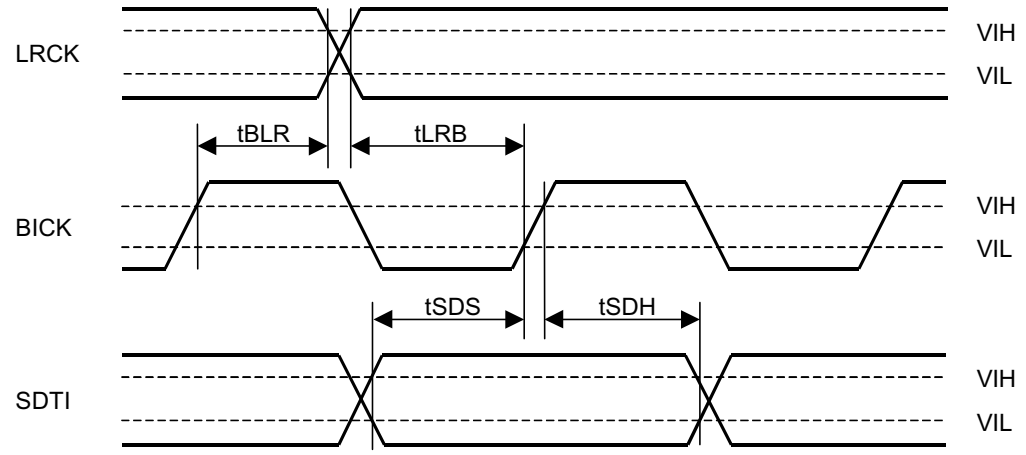
Parameter		Symbol	min	typ	max	Units
Master Clock Frequency		fCLK	2.048	11.2896	36.864	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency						
Normal Speed Mode		fsn	8		48	kHz
Double Speed Mode		fsd	60		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty	45		55	%
PCM Audio Interface Timing						
BICK Period						
Normal Speed Mode		tBCK	1/128fs			ns
Double/Quad Speed Mode		tBCK	1/64fs			ns
BICK Pulse Width Low		tBCKL	30			ns
Pulse Width High		tBCKH	30			ns
BICK "↑" to LRCK Edge	(Note 13)	tBLR	20			ns
LRCK Edge to BICK "↑"	(Note 13)	tLRB	20			ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns
DSD Audio Interface Timing						
DCLK Period		tDCK	1/64fs			ns
DCLK Pulse Width Low		tDCKL	160			ns
Pulse Width High		tDCKH	160			ns
DCLK Edge to DSDL/R	(Note 14)	tDDD	-20		20	ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	40			ns
CDTI Hold Time		tCDH	40			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 15)	tPD	150			ns

Notes: 13. BICK rising edge must not occur at the same time as LRCK edge.
14. DSD data transmitting device must meet this time.
15. The AK4383 can be reset by bringing PDN= "L".

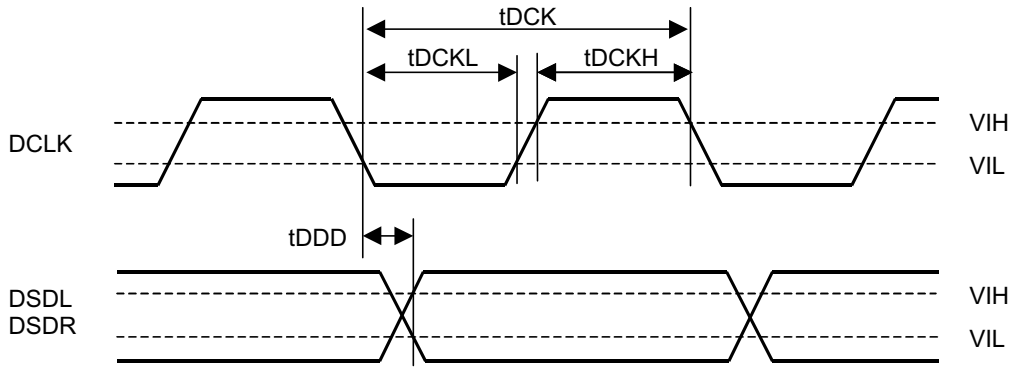
■ Timing Diagram



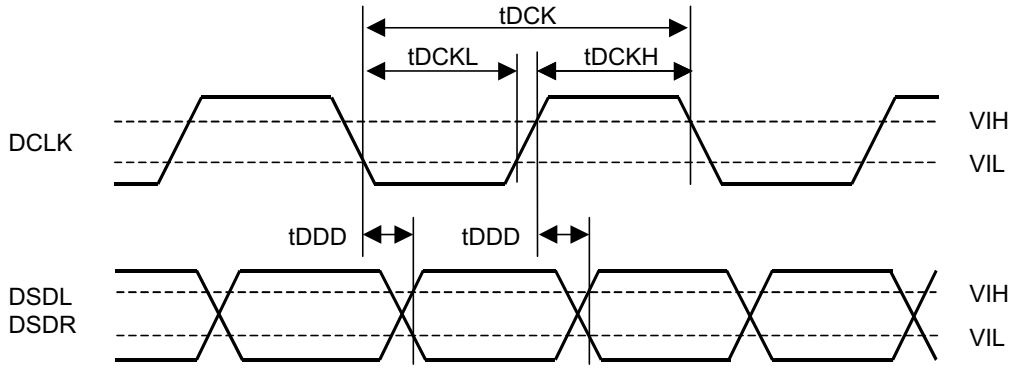
Clock Timing



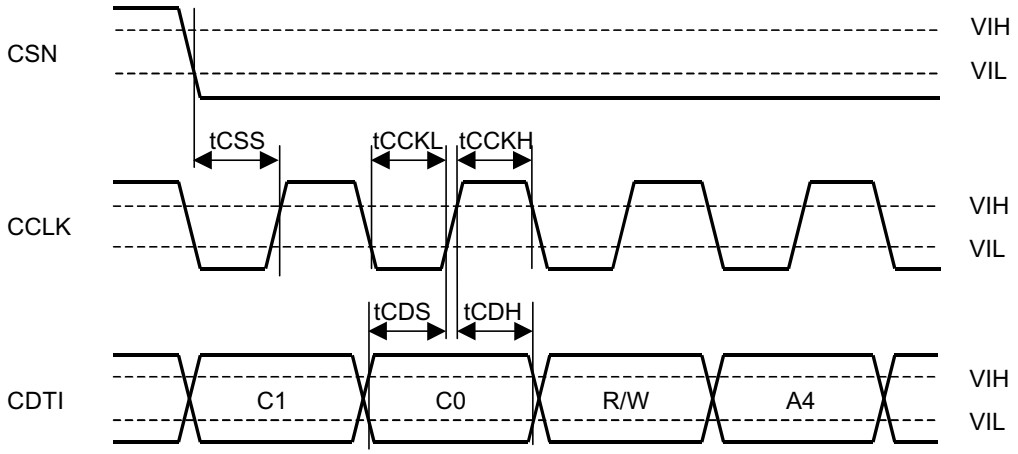
Audio Serial Interface Timing (PCM Mode)



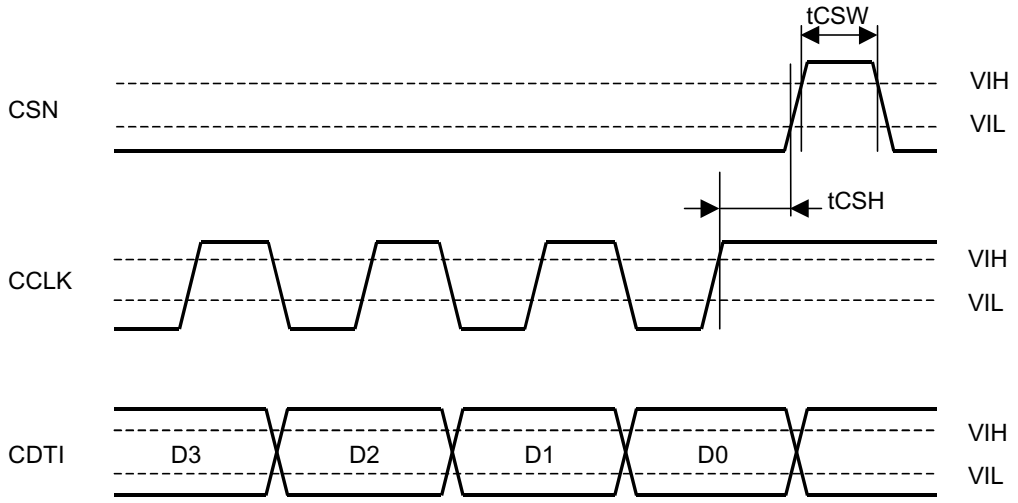
Audio Serial Interface Timing (DSD Normal Mode, DCKB = "0")



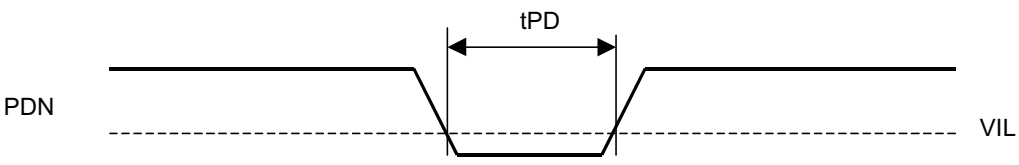
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB = "0")



WRITE Command Input Timing



WRITE Data Input Timing



Power-down Timing

OPERATION OVERVIEW

■ D/A Converion Mode

The AK4383 can perform D/A conversion for both PCM data and DSD data. When DSDM pin is "H", DSD data can be input from DCLK, DSDL and DSDR pins. PCM data can be input from BICK/DCLK, SDTI/DSDL and LRCK/DSDR pins by setting DSDM pin to "L". In this case, BICK/DCLK, SDTI/DSDL and LRCK/DSDR pins can accept DSD data by enabling DSD mode via the register (D/P = "1"). When PCM/DSD mode changes by DSDM pin or D/P bit, the AK4383 should be reset by PDN pin or RSTN bit. (Refer to D/A conversion mode switching timing.)

DSDM pin	D/P bit	Pin 2-4	Pin 9-11	DAC Output
L	0	PCM	*	PCM
	1	DSD	*	DSD
H	0	*	DSD	DSD
	1	*	DSD	DSD

Table 1. DSD/PCM Mode Control(* Don't care.)

■ System Clock

1) PCM Mode

The external clocks, which are required to operate the AK4383, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Register 00H), the sampling speed is set by DFS0/1(Table 2). The frequency of MCLK at each sampling speed is set automatically. (Table 3~5). In Auto Setting Mode (ACKS = "1": Default), as MCLK frequency is detected automatically (Table 6), and the internal master clock becomes the appropriate frequency (Table 7), it is not necessary to set DFS0/1.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4383 is in the normal operation mode (PDN= "H"). If these clocks are not provided, the AK4383 may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4383 should be reset by PDN= "L" after these clocks are provided. If the external clocks are not present, the AK4383 should be in the power-down mode (PDN= "L"). After exiting reset at power-up etc., the AK4383 is in the power-down mode until MCLK is input.

DFS1	DFS0	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	Default
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 2. Sampling Speed (Manual Setting Mode)

LRCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	11.2896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 5. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 6. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 7. System Clock Example (Auto Setting Mode)

2) DSD Mode

The external clocks, which are required to operate the AK4383, are MCLK and DCLK. The master clock (MCLK) should be synchronized with DSD clock (DCLK) but the phase is not critical. The frequency of MCLK is set by DCKS bit.

DCKS	0	1
MCLK	512fs	768fs
DCLK	64fs	64fs

Table 8. System Clock (fs=44.1kHz)

■ Audio Serial Interface Format

1) PCM Mode

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0-2 as shown in Table 7 can select five serial data modes. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI Format	BICK	Figure	
0	0	0	0	16bit LSB Justified	≥32fs	Figure 1	
1	0	0	1	20bit LSB Justified	≥40fs	Figure 2	
2	0	1	0	24bit MSB Justified	≥48fs	Figure 3	Default
3	0	1	1	24bit I^2S Compatible	≥48fs	Figure 4	
4	1	0	0	24bit LSB Justified	≥48fs	Figure 2	

Table 9. Audio Data Formats

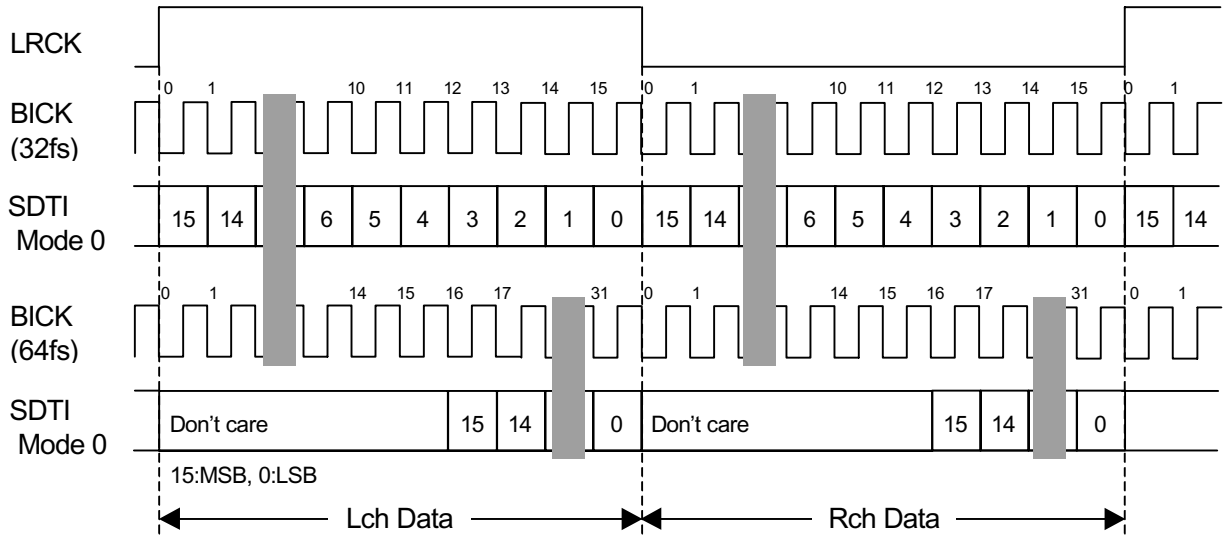


Figure 1. Mode 0 Timing

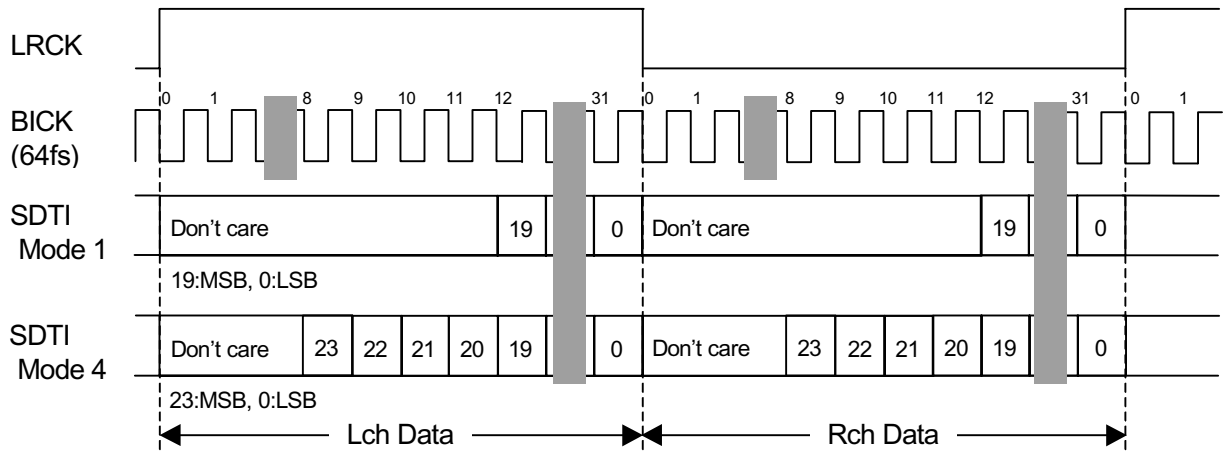


Figure 2. Mode 1,4 Timing

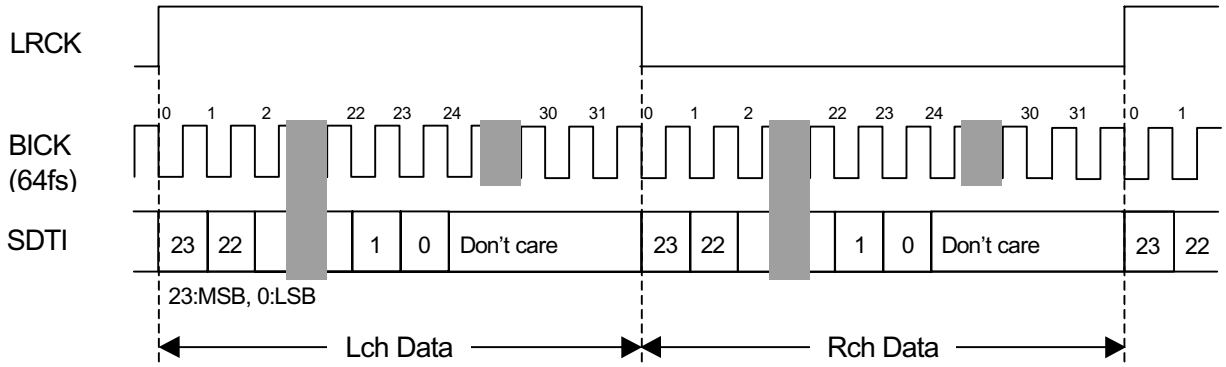


Figure 3. Mode 2 Timing

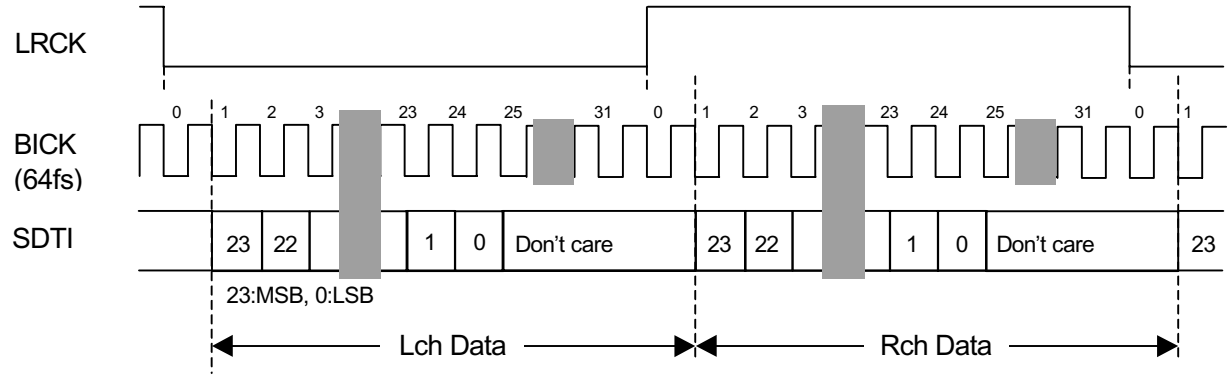


Figure 4. Mode 3 Timing

2) DSD Mode

In case of DSD mode, DIF0-2 are ignored. The frequency of DCLK is fixed to 64fs. DCKB bit can invert the polarity of DCLK.

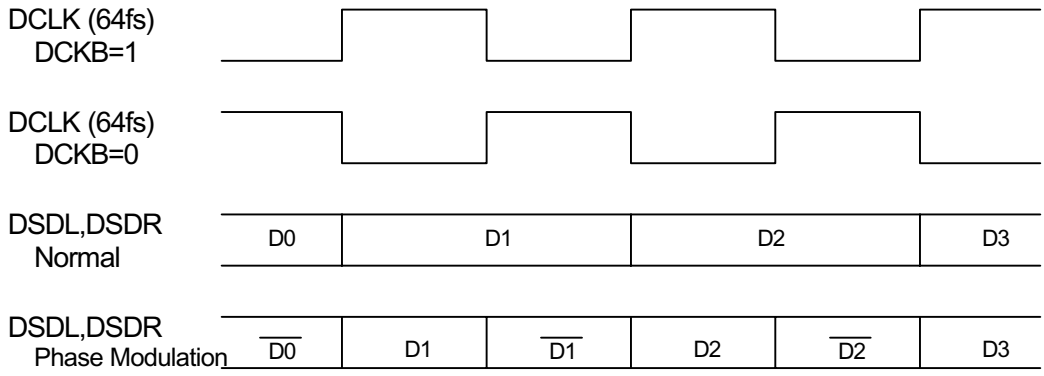


Figure 5. DSD Mode Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM0 and DEM1. In case of double speed and quad speed mode, the digital de-emphasis filter is always off.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 8. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume

The AK4383 includes channel independent digital output volumes (ATT) with 256 levels at linear step including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to –48dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. Table 11 shows transition times of 1 level and 256 levels. The setting value of the register is held when switching between PCM mode and DSD mode. The transition time at DSD mode is the same as Normal Speed Mode.

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

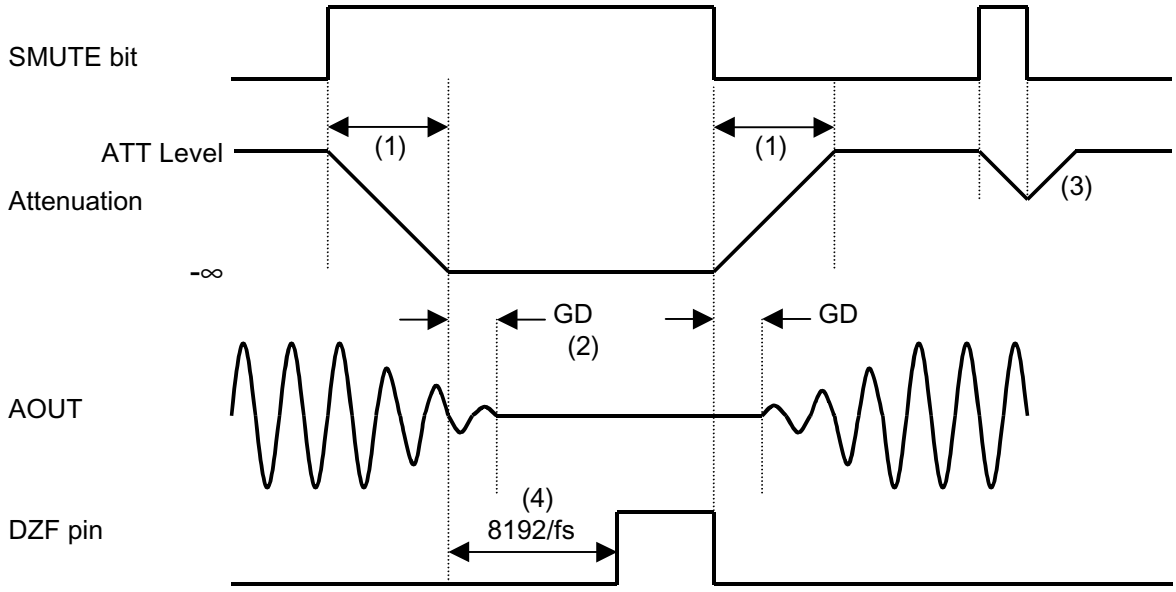
Table 11. ATT Transition Time

■ Zero Detection

The AK4383 has channel-independent zeros detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to “H”. DZF pin of each channel immediately goes to “L” if input data of each channel is not zero after going DZF “H”. If RSTN bit is “0”, DZF pins of both channels go to “H”. DZF pins of both channels go to “L” at 2~3/fs after RSTN bit returns to “1”. If DZFM bit is set to “1”, DZF pins of both channels go to “H” only when the input data at both channels are continuously zeros for 8192 LRCK cycles. Zero detect function can be disabled by DZFE bit. In this case, DZF pins of both channels are always “L”. DZFB bit can invert the polarity of DZF pin.

■ Soft Mute Operation

Soft mute operation is performed at digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 11) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 11). For example, in Normal Speed Mode, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255.

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF "H".

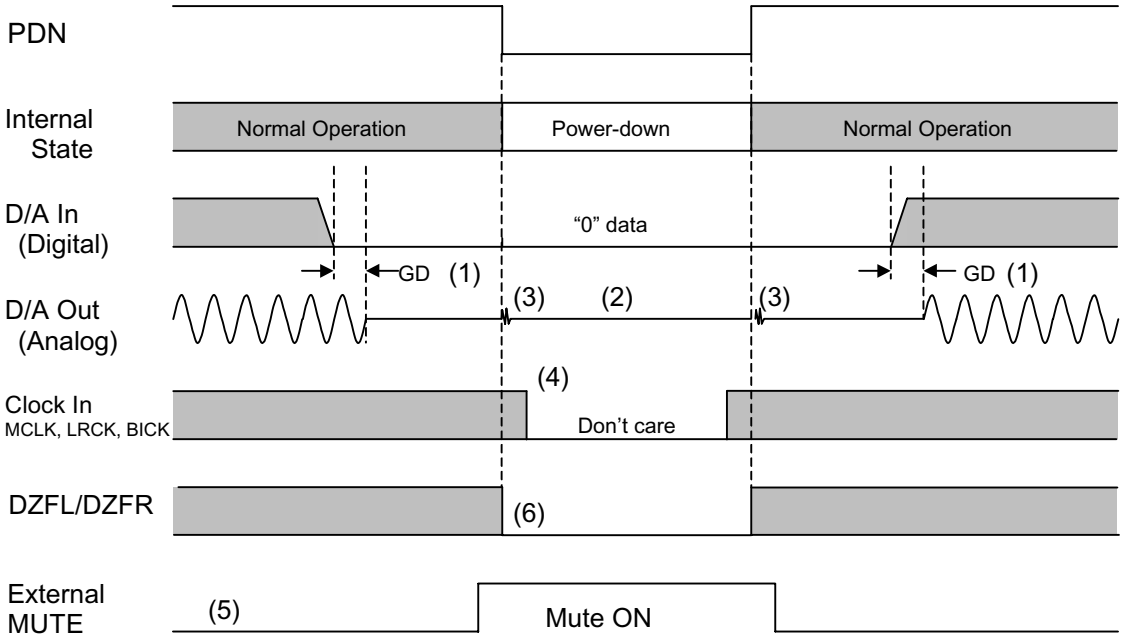
Figure 6. Soft Mute and Zero Detection

■ System Reset

The AK4383 should be reset once by bringing PDN= ”L” upon power-up. The analog section exits power-down mode by MCLK input and then the digital section exits power-down mode after the internal counter counts MCLK during 4/fs.

■ Power-down

The AK4383 is placed in the power-down mode by bringing PDN pin “L” and the anlog outputs are floating (Hi-Z). Figure 7 shows an example of the system timing at the power-down and power-up.



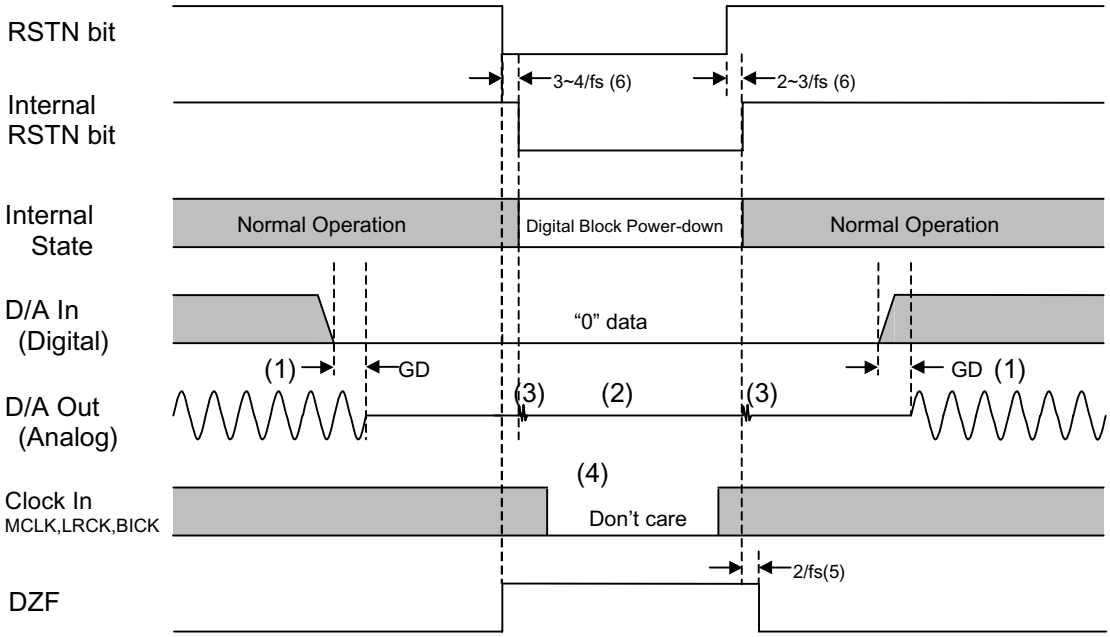
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = “L”).
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.
(6) DZF pins are “L” in the power-down mode (PDN = “L”).

Figure 7. Power-down/up Sequence Example

■ Reset Function

When RSTN=0, DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZFL/DZFR pins go to "H". Figure 8 shows the example of reset by RSTN bit.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage.
(3) Click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN = "L").
(5) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 2/fs after RSTN bit becomes "1".
(6) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN "1".

Figure 8. Reset Sequence Example

■ D/A conversion mode switching timing

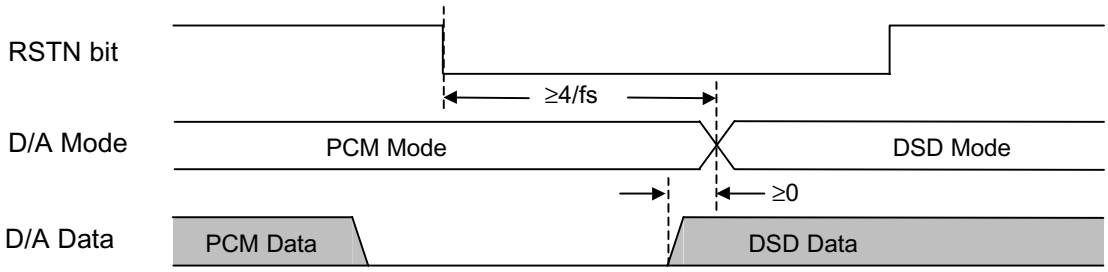


Figure 9. D/A Mode Switching Timing (PCM to DSD)

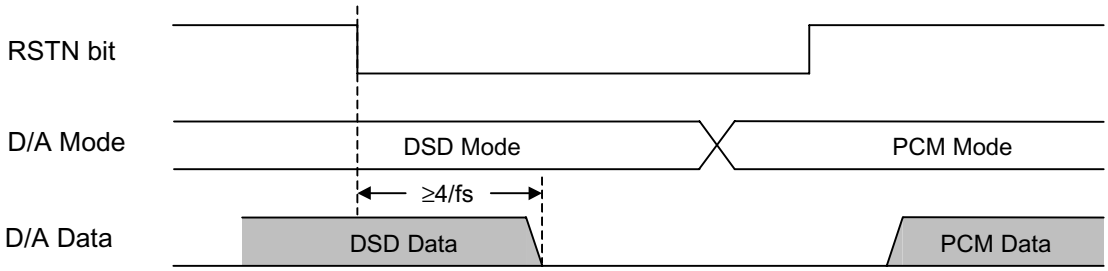


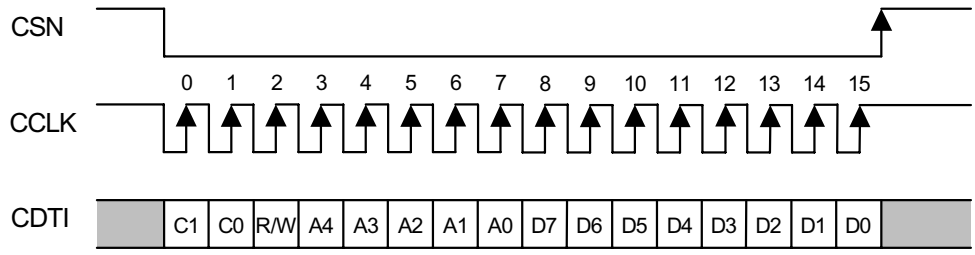
Figure 10. D/A Mode Switching Mode Timing (DSD to PCM)

Caution: In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

■ Mode Control Interface

Internal registers may be written by 3-wire μP interface pins, CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). The AK4383 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz (max). The CSN and CCLK must be fixed to "H" when the register does not be accessed.

PDN = "L" resets the registers to their default values. The internal timing circuit is reset by RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 11. Control I/F Timing

*The AK4383 does not support the read command and chip address. C1/0 and R/W are fixed to "011"
*When the AK4383 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	0	0	DCKS	D/P	DCKB	DZFB	0	0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:

For addresses from 05H to 1FH, data must not be written.
When PDN pin goes "L", the registers are initialized to their default values.
When RSTN bit goes "0", the only internal timing is reset and the registers are not initialized to their default values.
All data can be written to the register even if PW or RSTN bit is "0".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
default		1	0	0	0	1	0	1	1

RSTN: Internal timing reset control
0: Reset. All registers are not initialized.
1: Normal Operation
When MCLK frequency or DFS changes, the AK4383 should be reset by PDN pin or RSTN bit.

PW: Power down control
0: Power down. All registers are not initialized.
1: Normal Operation

DIF2-0: Audio data interface formats (see Table 9, PCM only)
Initial: "010", Mode 3

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM only)
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS1-0 are ignored. When this bit is "0", DFS1-0 set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft-muted

DEM1-0: De-emphasis Response (see Table 10, PCM only)
Initial: "01", OFF

DFS1-0: Sampling speed control (PCM only)
00: Normal Speed Mode
01: Double Speed Mode
10: Quad Speed Mode
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

SLOW: Slow Roll-off Filter Enable (PCM only)
0: Sharp Roll-off Filter
1: Slow Roll-off Filter

DZFE: Data Zero Detect Enable
0: Disable
1: Enable
Zero detect function can be disabled by DZFE bit "0". In this case, the DZF pins of both channels are always "L".

DZFM: Data Zero Detect Mode
0: Channel Separated Mode
1: Channel ANDed Mode
If the DZFM bit is set to "1", the DZF pins of both channels go to "H" only when the input data at both channels are continuously zeros for 8192 LRCK cycles.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	0	0	DCKS	D/P	DCKB	DZFB	0	0
default		0	0	0	0	0	0	0	0

DZFB: Inverting Enable of DZF
0: DZF goes "H" at Zero Detection
1: DZF goes "L" at Zero Detection

DCKB: Polarity of DCLK (DSD only)
0: DSD data is output from DCLK falling edge
1: DSD data is output from DCLK rising edge

D/P: DSD/PCM Mode Select
0: PCM Mode. SCLK, SDTI, LRCK input on Pin 2-4.
1: DSD Mode. DCLK, DSDL, DSDR input on Pin 2-4.
When D/P changes, the AK4383 should be reset by PDN pin or RSTN bit.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs
1: 768fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
default		1	1	1	1	1	1	1	1

ATT = 20 log (ATT_DATA / 255) [dB]
00H: Mute

SYSTEM DESIGN

Figure 12 shows the system connection diagram. An evaluation board (AKD4383) is available in order to allow an easy study on the layout of a surrounding circuit.

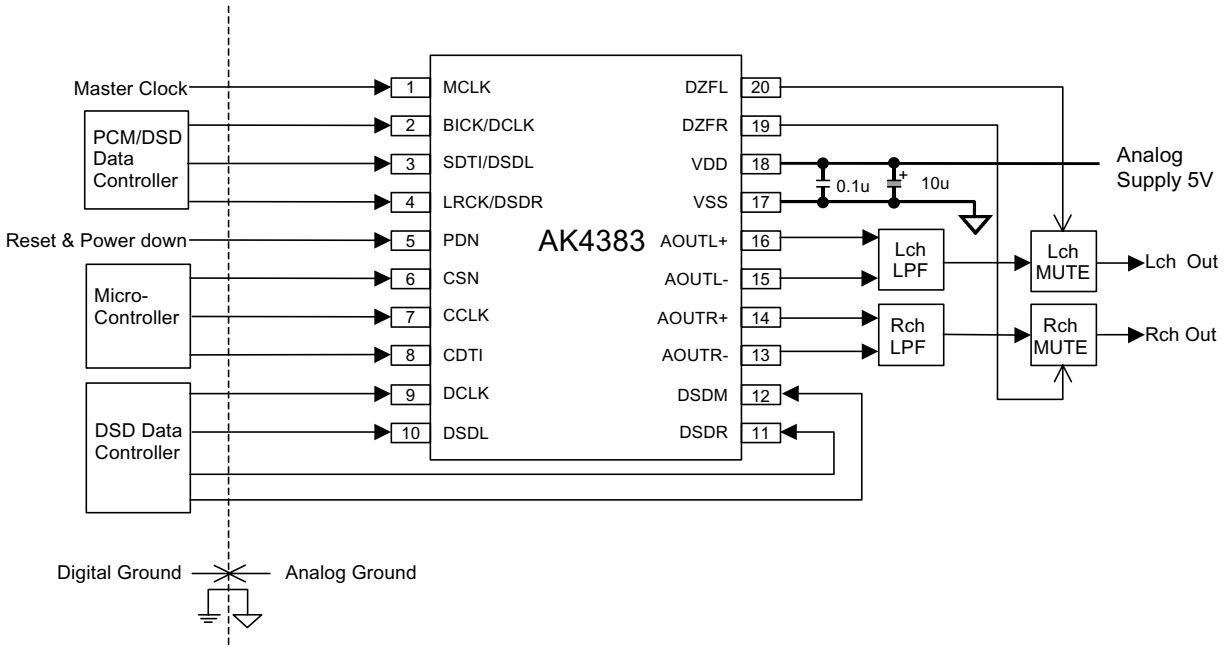


Figure 12. Typical Connection Diagram

Notes:

- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down pins should not be left floating.

1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor, especially 0.1μF ceramic capacitor for high frequency should be placed as near to VDD as possible. The differential Voltage between VDD and VSS pins set the analog output range.

2. Analog Outputs

The analog outputs are full-differential outputs and 0.5 x VDD Vpp (typ) centered around the internal common voltage (about AVDD/2). The differential outputs are summed externally, V_{AOUT}=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 5.0Vpp (typ @VDD=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFF (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H (@24bit).

The internal switched-capacitor filter and external low pass filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. DC offset on AOUT+/- is eliminated without AC coupling since the analog outputs are differential.

3. External Analog Filter

It is recommended by SACD format book (Scarlet Book) that the filter response at SACD playback is an analog low pass filter with a cut-off frequency of maximum 50kHz and a slop of minimum 30dB/Oct. The AK4383 can achieve this filter response by combination of the internal filter (Table 12) and an external filter (Figure 11).

Frequency	Gain
20kHz	-0.4dB
50kHz	-2.8dB
100kHz	-15.5dB

Table 12. Internal Filter Response at DSD mode

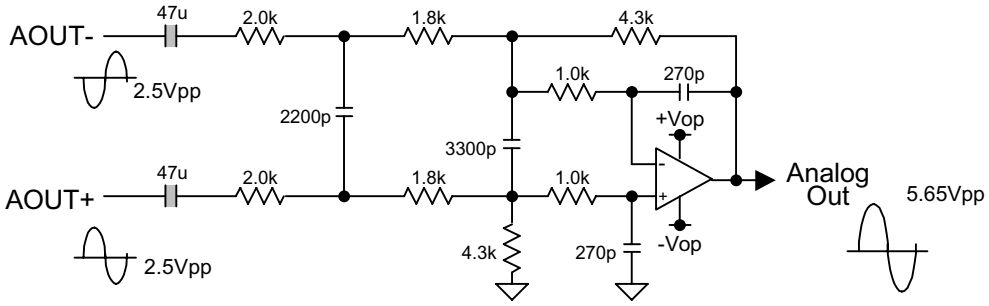


Figure 13. External 3rd order LPF Circuit Example

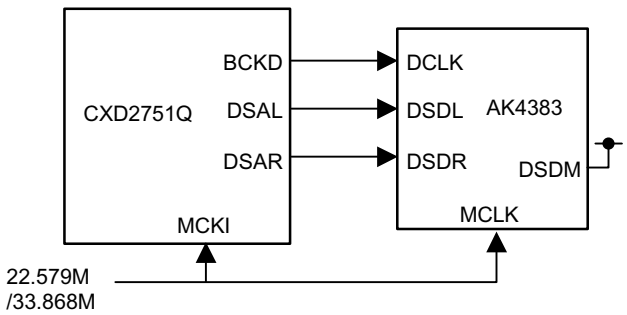
Frequency	Gain
20kHz	-0.05dBr
50kHz	-0.51dBr
100kHz	-16.8dBr

DC gain = 1.07dB

Table 13. 3rd order LPF (Figure 13) Response

■ Application Example

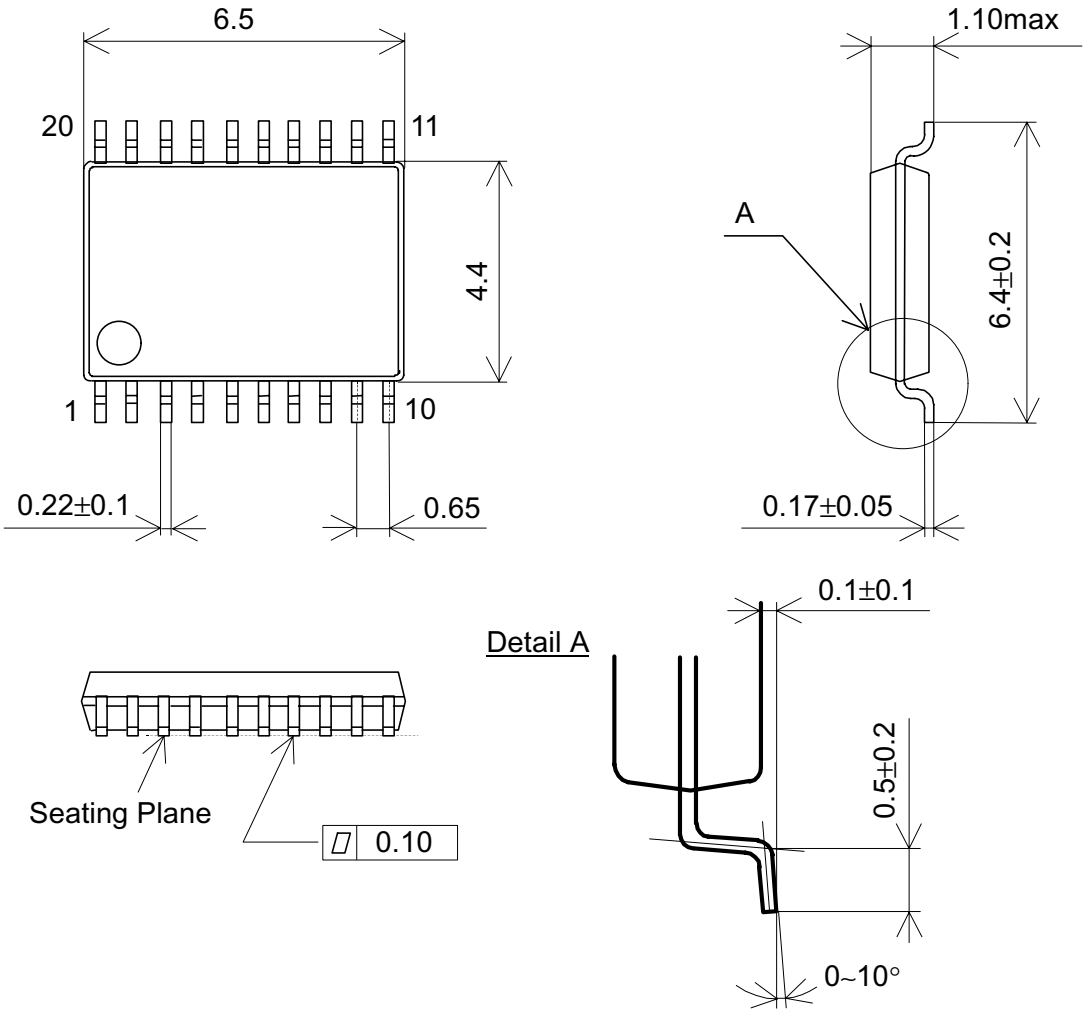
1) Connection with DSD Decoder, CXD2751Q



Phase Modulation Mode

PACKAGE

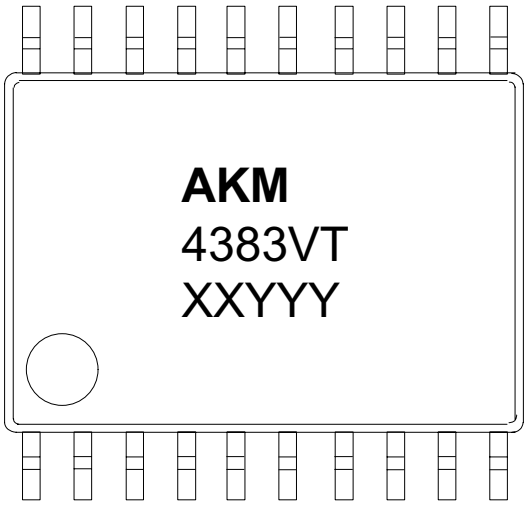
20pin TSSOP (Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Asahi Kasei Logo
2) Marketing Code : 4383VT
3) Date Code : XXYYY (5 digits)
   XX: lot#
   YYY: Date Code
4) Pin #1 indication

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.