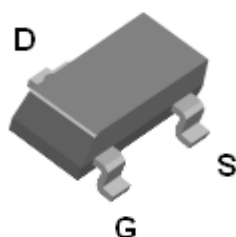


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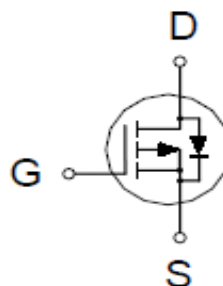
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-20V	150mΩ @ $V_{GS} = -4.5V$	-3A



SOT-23



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	-3	A
	$T_A = 70\text{ }^{\circ}\text{C}$		-1.9	
Pulsed Drain Current ¹		I_{DM}	-12	
Avalanche Current		I_{AS}	-12	
Avalanche Energy	$L = 0.1\text{ mH}$	E_{AS}	7	mJ
Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	1.2	W
	$T_A = 70\text{ }^{\circ}\text{C}$		0.7	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		110	$^{\circ}\text{C} / \text{W}$

¹Pulse width limited by maximum junction temperature.

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P-Channel Logic Level Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

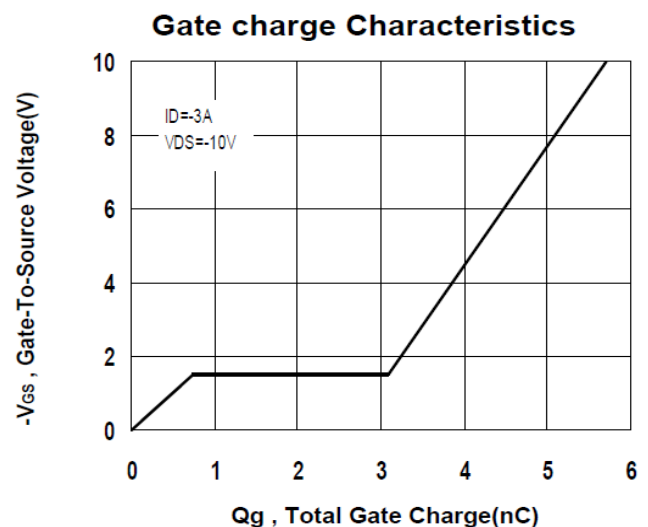
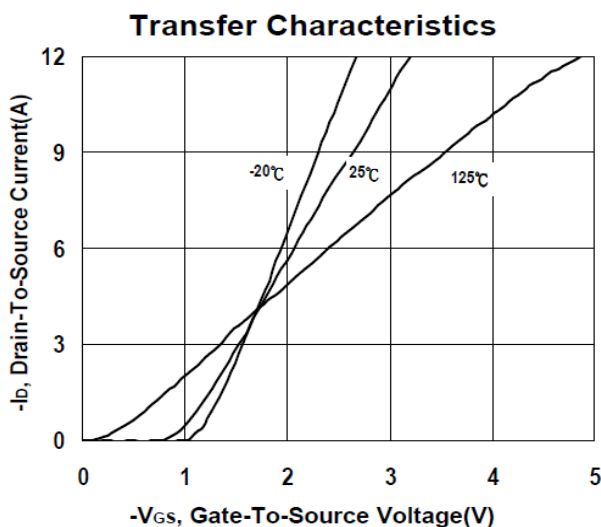
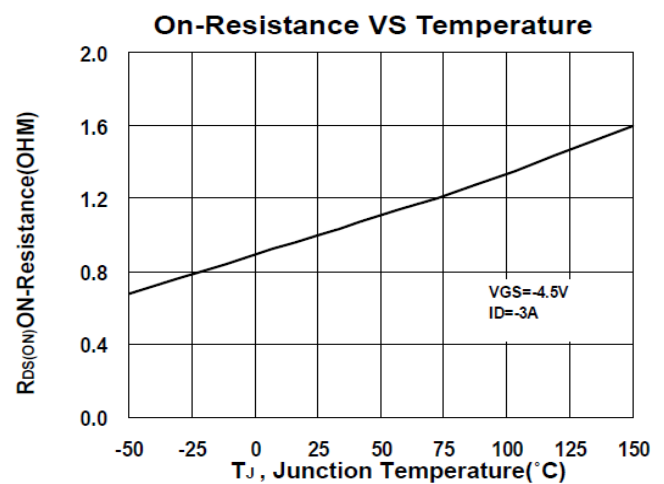
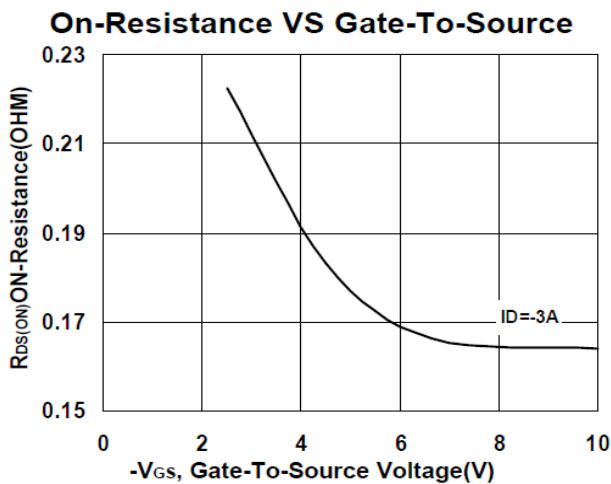
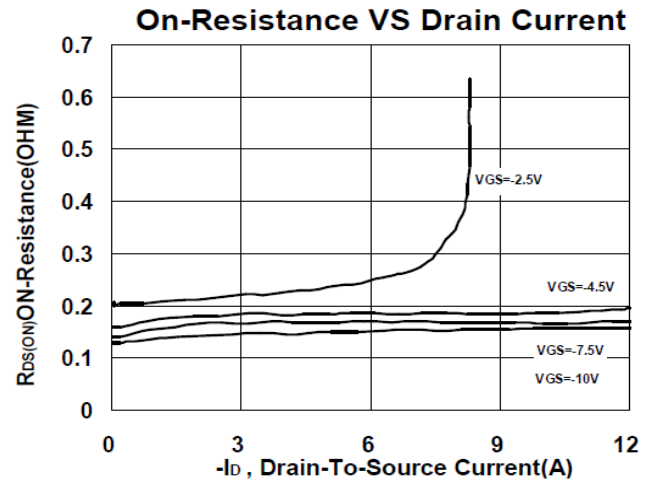
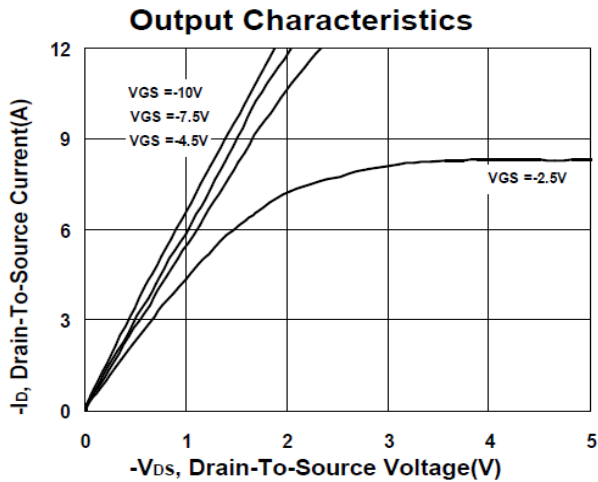
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.5	-0.9	-1.2	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
		V _{DS} = -16V, V _{GS} = 0V , T _J = 55 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-6			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -2.5V, I _D = -1A		118	250	mΩ
		V _{GS} = -4.5V, I _D = -3A		87	150	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -3A		16		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		415		pF
Output Capacitance	C _{oss}			119		
Reverse Transfer Capacitance	C _{rss}			85		
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		6.3		Ω
Total Gate Charge ²	Q _g	V _{DS} = 0.5V _{(BR)DSS} , V _{GS} = -4.5V, I _D = -3A		5.8		nC
Gate-Source Charge ²	Q _{gs}			1		
Gate-Drain Charge ²	Q _{gd}			2.4		
Turn-On Delay Time ²	t _{d(on)}	V _{DD} = -10V I _D ≅ -3A, V _{GS} = -4.5V, R _G = 6Ω		13		nS
Rise Time ²	t _r			36		
Turn-Off Delay Time ²	t _{d(off)}			42		
Fall Time ²	t _f			34		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICE (T _J = 25 °C)						
Continuous Current	I _S				3	A
Forward Voltage ¹	V _{SD}	I _F = -1A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = -1A,dI _F /dt = 100 A/μs		21		nS
Reverse Recovery Charge	Q _{rr}			7		nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

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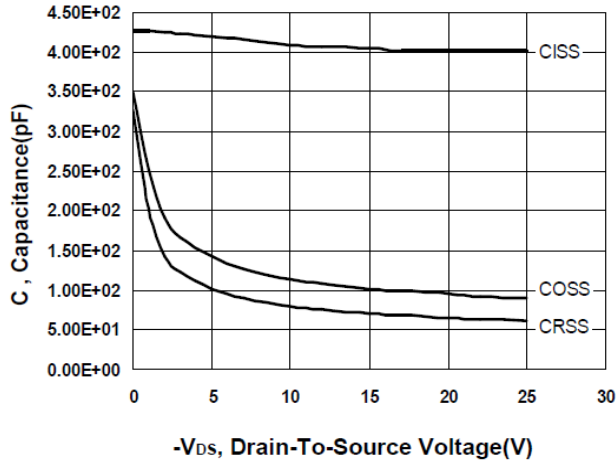
P-Channel Logic Level Enhancement Mode MOSFET



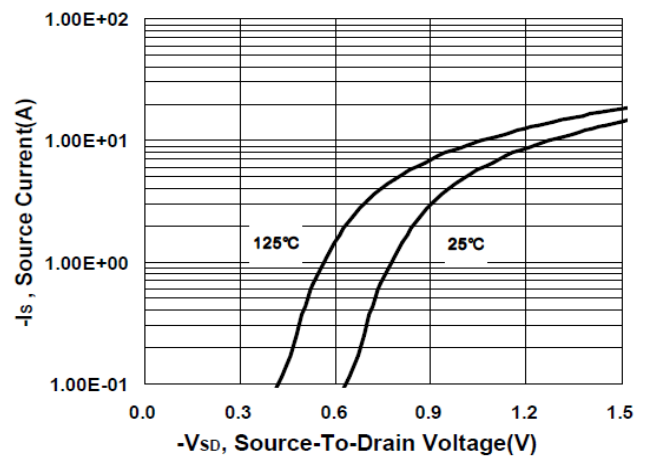
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P-Channel Logic Level Enhancement Mode MOSFET

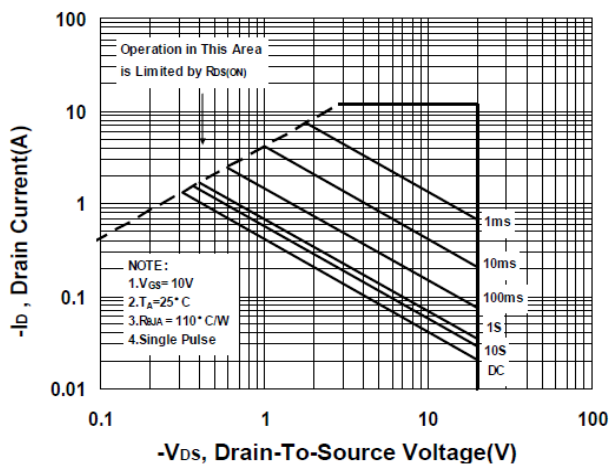
Capacitance Characteristic



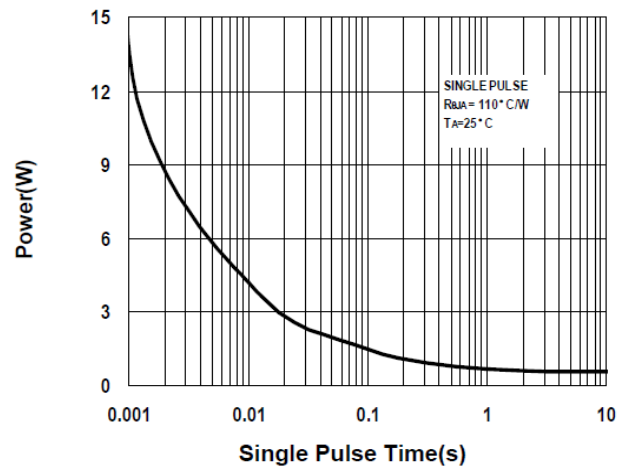
Body Diode Forward Voltage



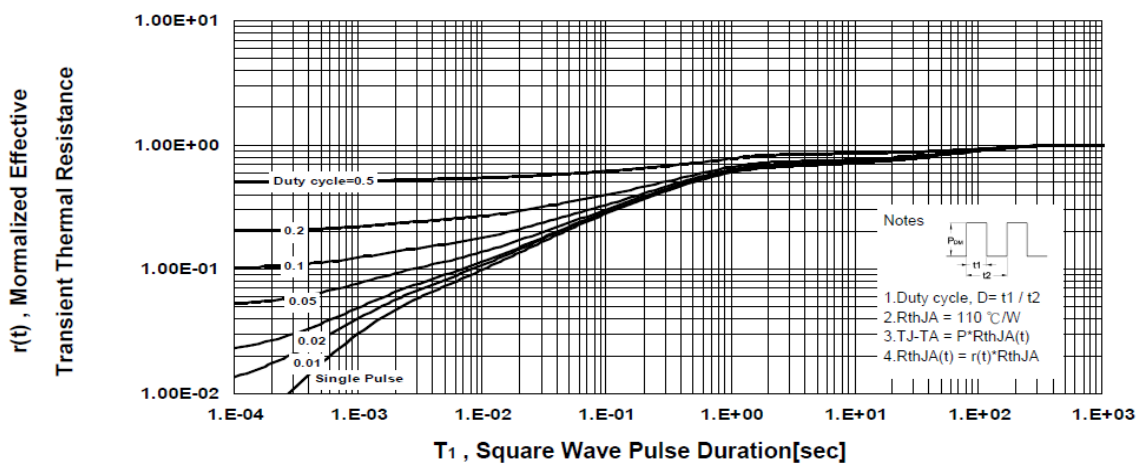
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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P-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

SOT-23 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A		1.05		H	0.1		0.2
B	2.4		3	I	0.3		0.6
C	1.4		1.73				
D	2.7		3.1				
E	1		1.31				
F	0		0.15				
G	0.3		0.5				

