ESD7205, SZESD7205

Product Preview

ESD Protection Diodes

Low Capacitance ESD Protection Diodes for High Speed Data Line

The ESD7205 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The small form factor, flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as Ethernet and LVDS present in automotive camera modules.

Features

- Low Capacitance (0.4 pF Typical, I/O to GND)
- Diode capacitance matching
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4 (ESD)
- Low ESD Clamping Voltage (12 V Typical, +16 A TLP, I/O to GND)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- 10/100/1000 Automotive Ethernet
- LVDS
- Automotive USB 2.0
- High Speed Differential Pairs

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact IEC 61000−4−2 Air ISO 10605 330 pF / 2 kΩ Contact ISO 10605 330 pF / 330 Ω Contact	ESD	±25 ±25 ±30 ±20	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

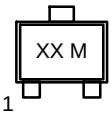
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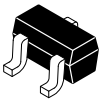
MARKING DIAGRAMS



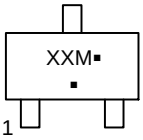
SOT−723
CASE 631AA



XX = Specific Device Code
M = Date Code

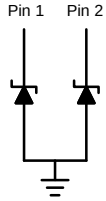


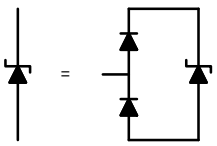
SC−70
CASE 419



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION AND SCHEMATIC





ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

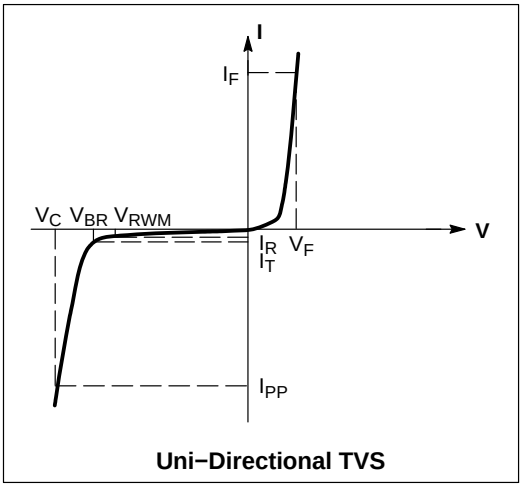
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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.2	6.0	8.0	V
Reverse Leakage Current	I_R	V_{RWM} = 5.0 V, I/O Pin to GND			1	μA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 3 and 4			
Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		10 12.5 −4.0 −8.0		V
Junction Capacitance Match	ΔC_J	V_R = 0 V, f = 1 MHz between I/O1 to GND and I/O 2 to GND		5	10	%
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins		0.2	0.35	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.4	0.55	pF
3dB Bandwidth	f_{BW}	R_L = 50 Ω		5		GHz

1. For test procedure see Figures 5 and 6 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

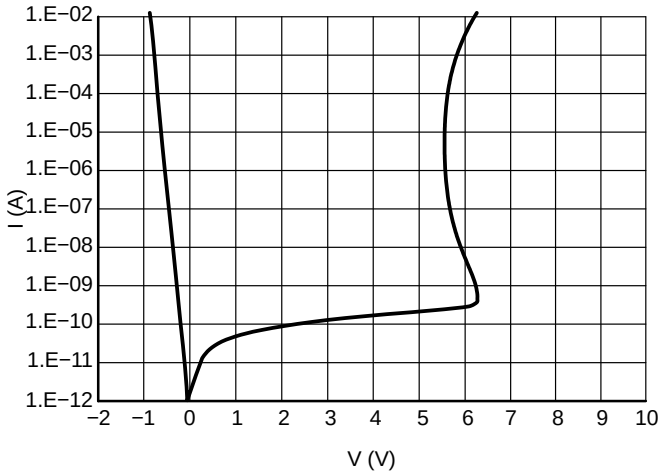


Figure 1. IV Characteristics

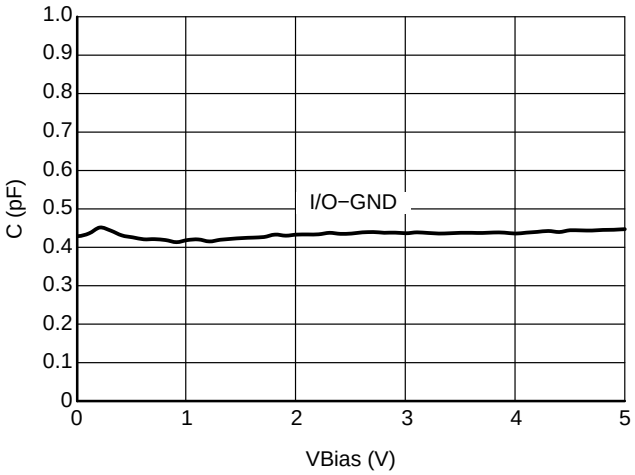


Figure 2. CV Characteristics

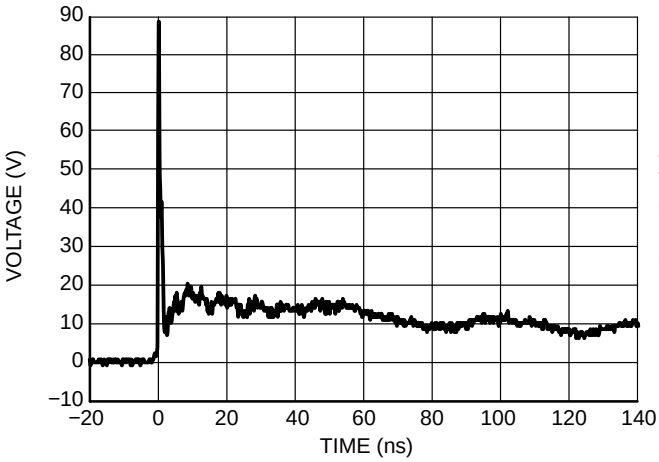


Figure 3. IEC61000−4−2 +8 kV Contact ESD Clamping Voltage

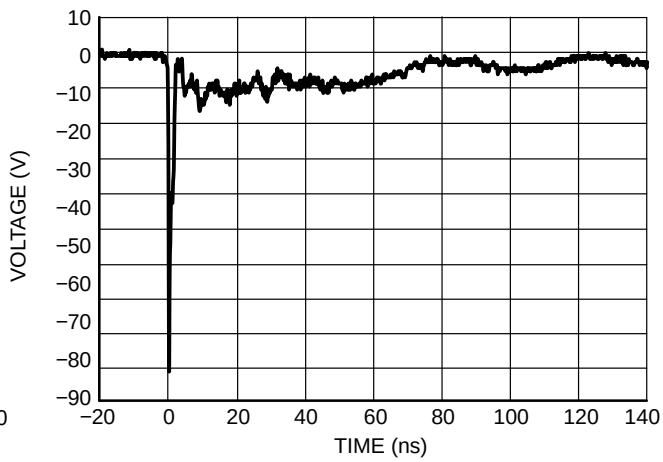


Figure 4. IEC61000−4−2 −8 kV Contact ESD Clamping Voltage

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

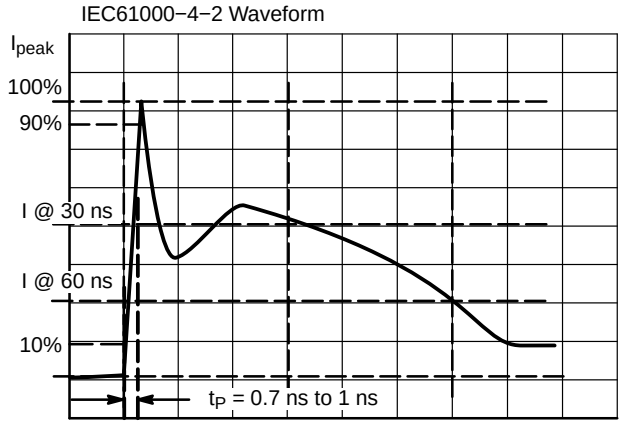


Figure 5. IEC61000−4−2 Spec

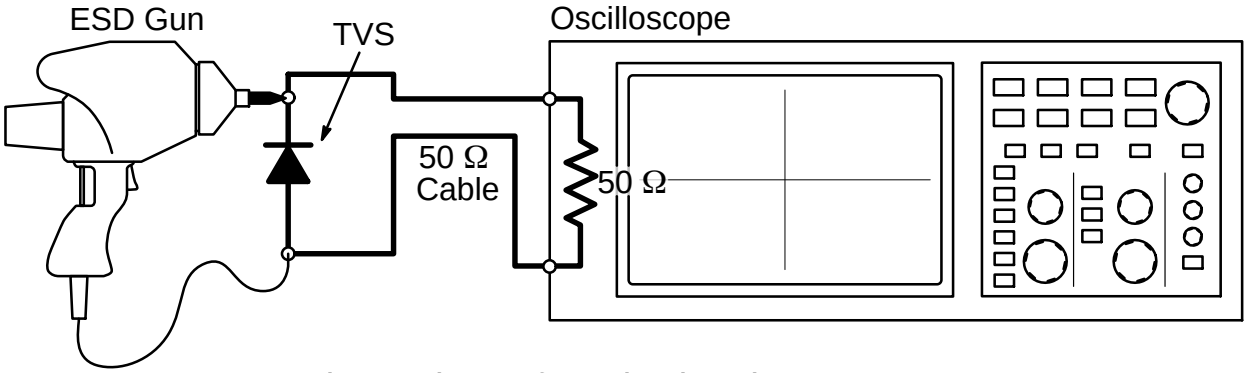


Figure 6. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

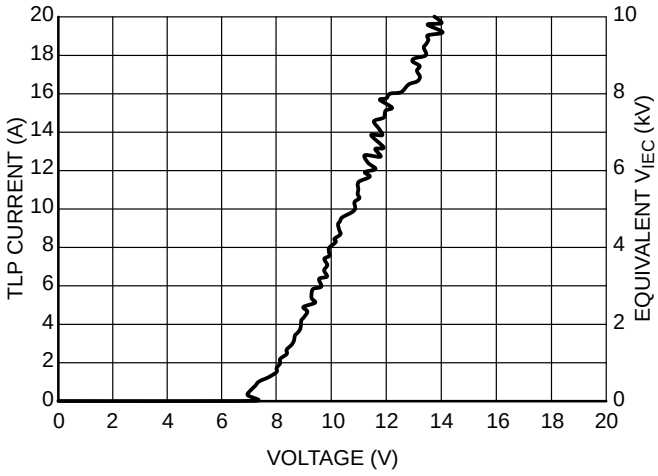


Figure 7. Positive TLP IV Curve

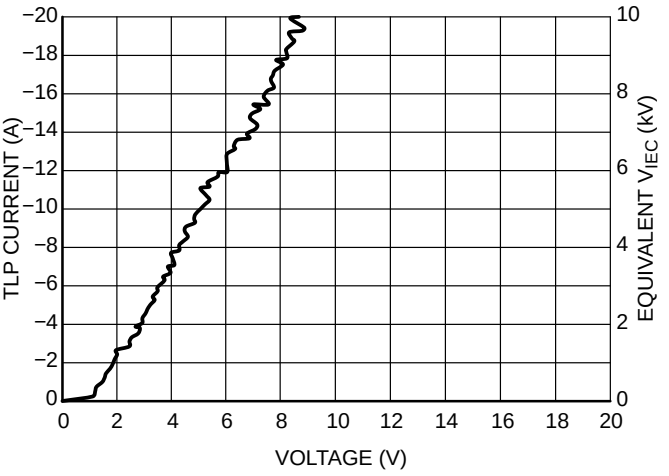


Figure 8. Negative TLP IV Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

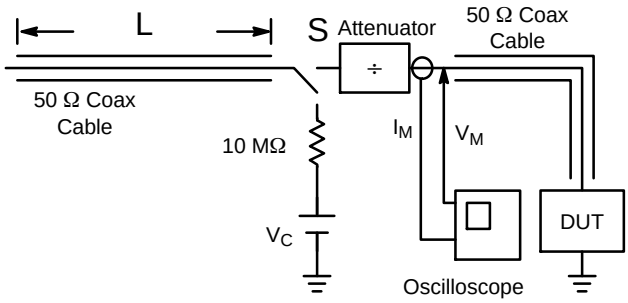


Figure 9. Simplified Schematic of a Typical TLP System

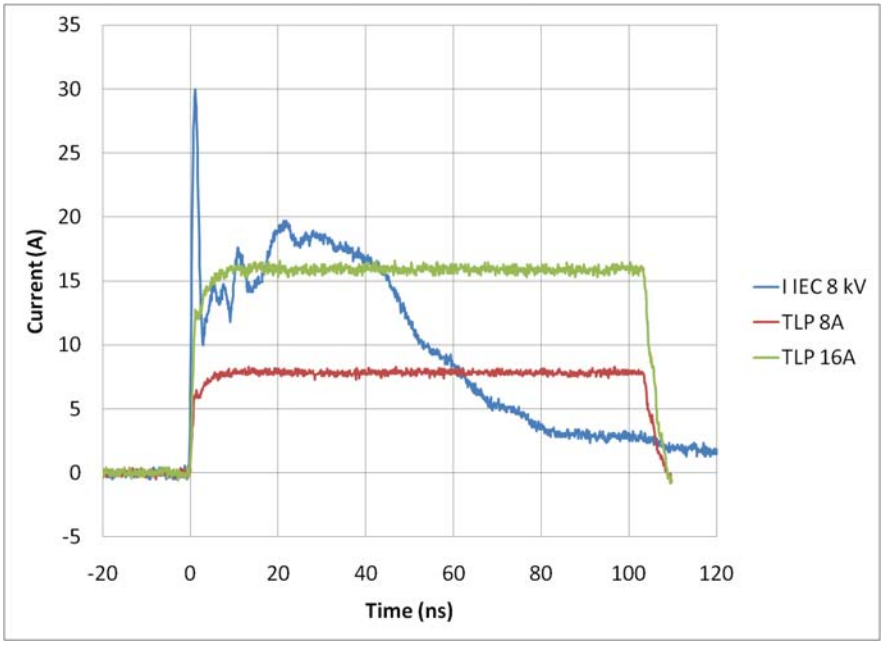


Figure 10. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

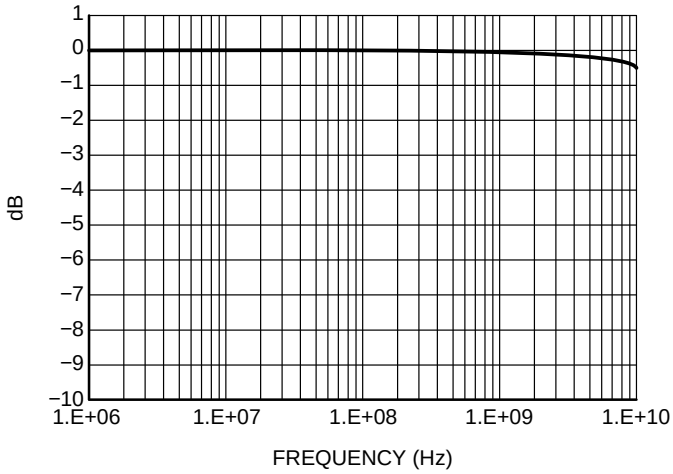


Figure 11. RF Insertion Loss

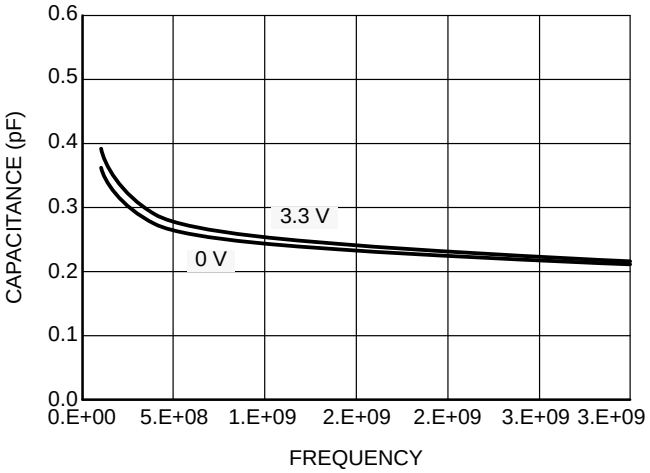


Figure 12. Capacitance over Frequency

ORDERING INFORMATION

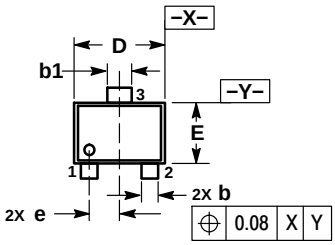
Device	Package	Shipping†
ESD7205M3T5G	SOT−723 (Pb−Free)	8000 / Tape & Reel
SZESD7205M3T5G*	SOT−723 (Pb−Free)	8000 / Tape & Reel
ESD7205WTT1G	SOT−323 (Pb−Free)	3000 / Tape & Reel
SZESD7205WTT1G*	SOT−323 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

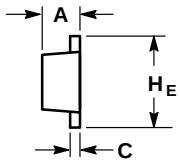
*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

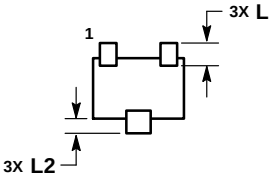
SOT−723
CASE 631AA
ISSUE D



TOP VIEW



SIDE VIEW

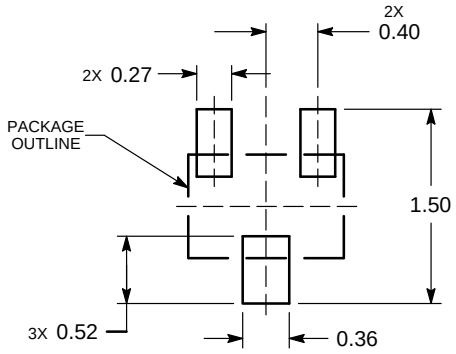


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
C	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H E	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25

RECOMMENDED SOLDERING FOOTPRINT*

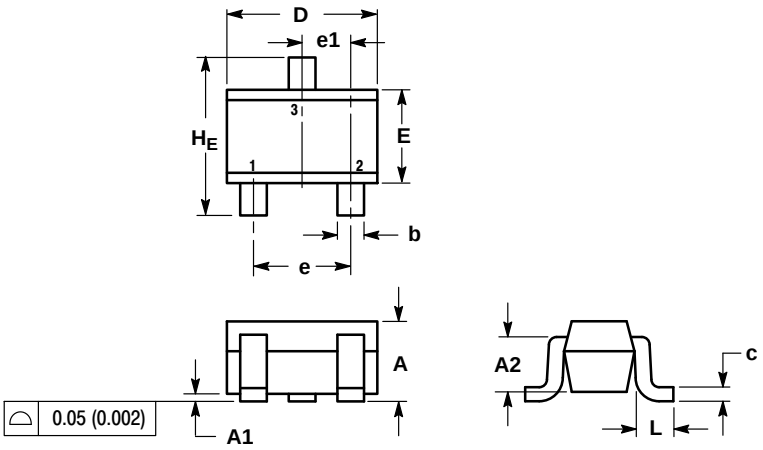


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

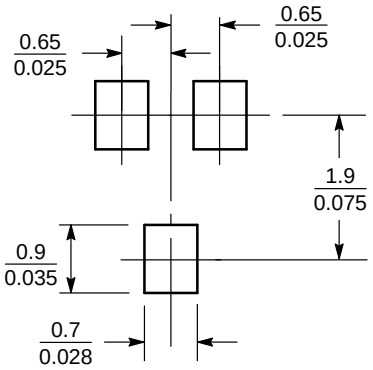
SC−70 (SOT−323)
CASE 419−04
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.70 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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