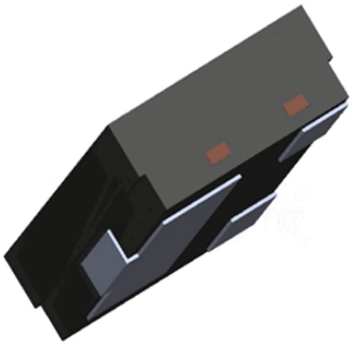
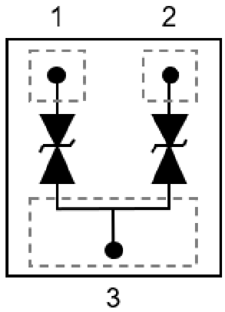
ESDCAN03-2BM3Y

Datasheet

Automotive dual-line TVS in DFN for CAN bus



QFN-3L 1.1 x 1.0 x 0.55



Product status link
ESDCAN03-2BM3Y

Product summary	
Order code	ESDCAN03-2BM3Y

Features

- AEC-Q101 qualified
- Dual-line ESD and EOS protection
- Triggering voltage, V_{TRIG} min = 28 V
- QFN-3L 1.1 x 1.0 x 0.55 package also called DFN1110
- Bidirectional device
- Max pulse power up to 3.3 A (8/20 µs)
- Low clamping factor V_{CL} / V_{BR}
- Low leakage current
- ECOPACK2 ROHS compliant component

Complies with the following standards

- UL94, V0
- J-STD-020 MSL level 1
- IPC7531 footprint and JEDEC registered package
- ISO 16750-2 (Jump start and reversed battery tests)
- ISO 10605 / IEC 61000-4-2- C = 150 pF, R = 330 Ω, exceeds level 4:
  – ±15 kV (contact discharge)
- ISO 10605 - C = 330 pF, R = 2 kΩ:
  – ±30 kV (contact discharge)
- ISO 10605 - C = 330 pF, R = 330 Ω:
  – ±12 kV (contact discharge)
- ISO 7637-3:
  – Pulse 3a: -150 V
  – Pulse 3b: +150 V
  – Pulse 2a: +/- 85 V

Applications

Automotive controller area network where an electrostatic discharge or another transient surge may damage the CAN transceiver or an integrated circuit (IC) featuring a CAN PHY. This product is compliant with most of automotive interfaces.

Description

This device is a dual-line transient voltage suppressor (TVS) specifically designed to protect the CAN H and CAN L pins of an automotive CAN transceiver against electrostatic discharge (ESD) and ISO 7637-3.

The ESDCAN03-2BM3Y complies with all the physical layer constraints (jump start, reverse polarity, …) without compromising the low clamping voltage for an efficient CAN bus protection.

The low line capacitance of each ESD diode makes this CAN protection compatible not only with CAN-FD but also with high speed and high data rate buses like FlexRay, USB and more.

1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 / ISO 10605 - C = 150 pF, R = 330 Ω: Contact discharge	±15	kV
		ISO 10605 - C = 330 pF, R = 330 Ω: Contact discharge	±12	
		ISO 10605 - C = 330 pF, R = 2 kΩ: Contact discharge	±30	
I_{PP}	Peak pulse current (8/20 µs)		3.3	A
T_j	Operating junction temperature range		-55 to +175	°C
T_{stg}	Storage temperature range		-55 to +175	°C

Figure 1. Electrical characteristics (definitions)

Symbol		Parameter
V_{Trig}	=	Trigger voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
I_{PP}	=	Peak pulse current
R_D	=	Dynamic resistance
V_H	=	Holding voltage
C_{LINE}	=	Input capacitance per line

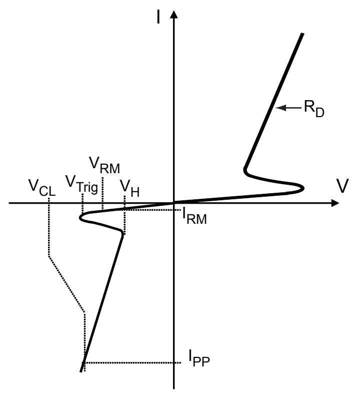


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{Trig}	Trigger voltage, higher voltage than V_{TRIG} guarantees the protection turn-on		28			V
V_H	Holding voltage, lower voltage than V_H guarantees the protection turn-off		24			V
I_{RM}	Leakage current	V_{RM} = 24 V			50	nA
V_{CL}	Clamping voltage	ISO7637-3 pulse 3a at -150 V min.		-36		V
		ISO7637-3 pulse 3b at +150 V max.		36		
		8/20 µs waveform, I_{PP} = 3 A		32	36.5	
C_{LINE}	Line capacitance	V_{LINE} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		3.3	3.6	pF
ΔC_{LINE}	Line capacitance variation between IO1 and IO2 versus GND	V_{LINE} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		0.01		pF

1.1 Characteristics (curves)

Figure 2. Maximum peak current versus initial junction temperature (8/20 µs exponential waveform)

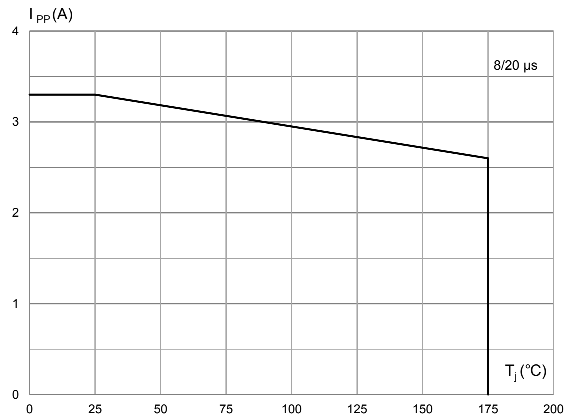


Figure 3. Maximum peak pulse current versus exponential pulse duration

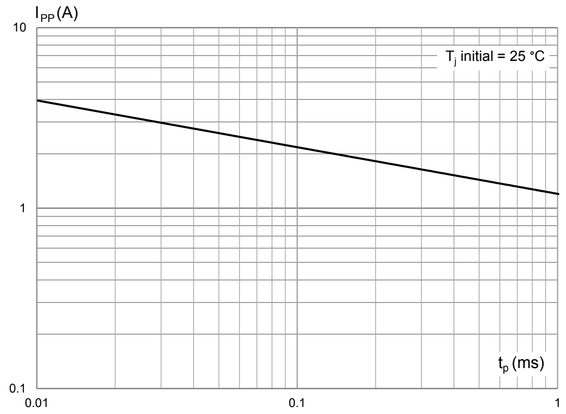


Figure 4. Peak pulse current versus clamping voltage (8/20 µs exponential waveform)

Figure 5. Junction capacitance versus reverse applied voltage

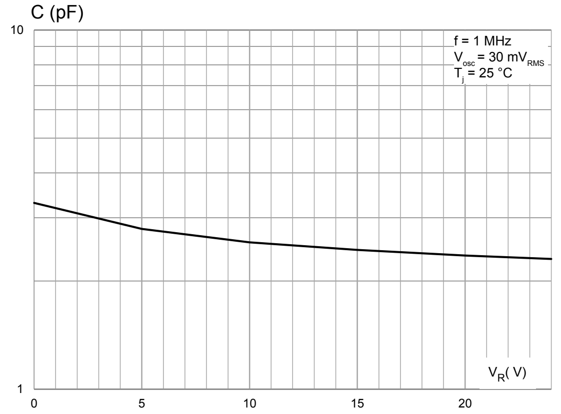


Figure 6. Leakage current versus junction temperature

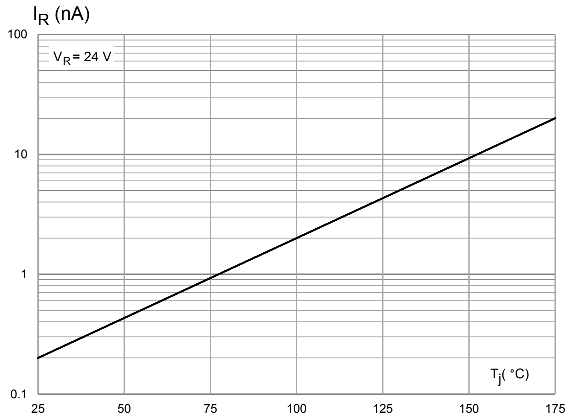


Figure 7. TLP

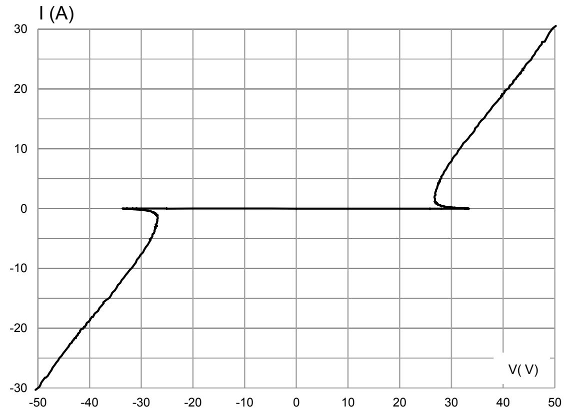


Figure 8. **Response to ISO 10605 -C = 150 pF, R = 330 Ω (-8 kV contact)**

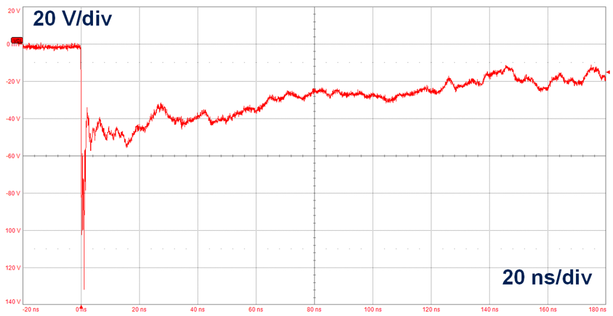


Figure 9. **Response to ISO 10605 - C = 150 pF, R = 330 Ω (+8 kV contact)**

Figure 10. **Response to ISO 7637-3 Pulse 3a: -150 V**

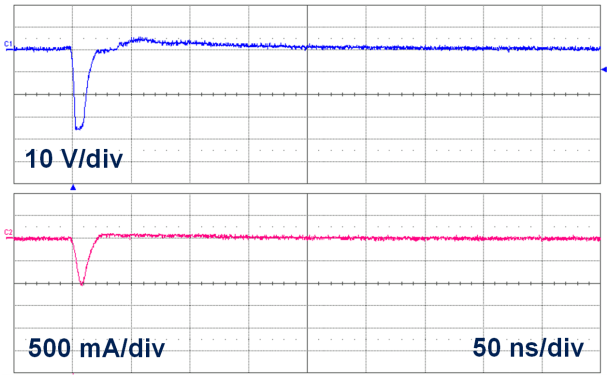


Figure 11. **Response to ISO 7637-3 Pulse 3b : +150 V**

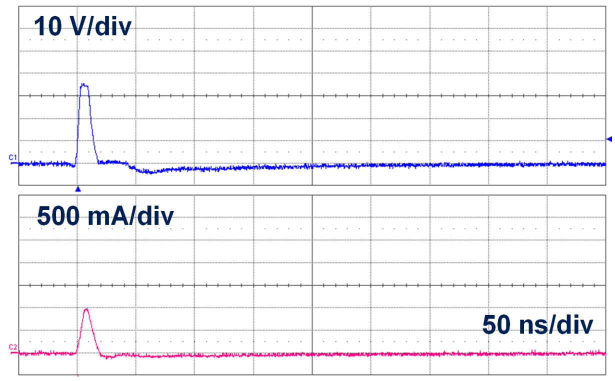


Figure 12. **Response to ISO 7637-3 pulse 2a: -85 V**

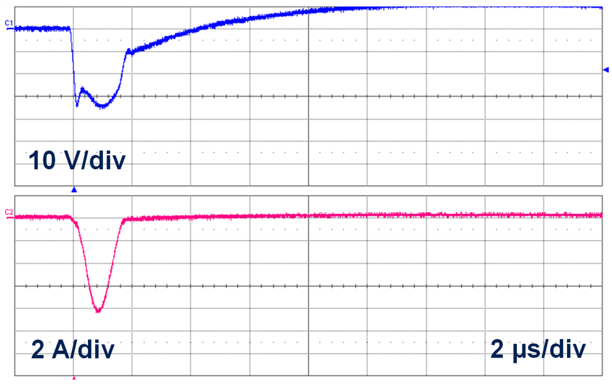
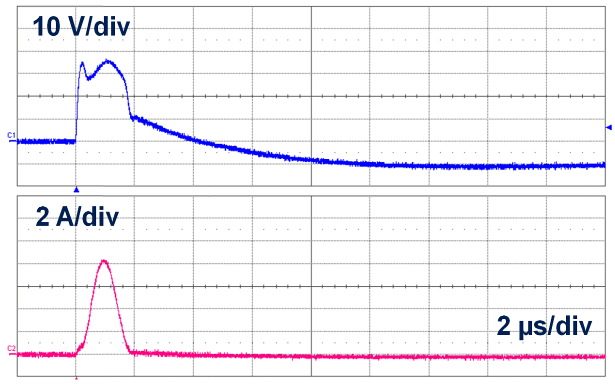
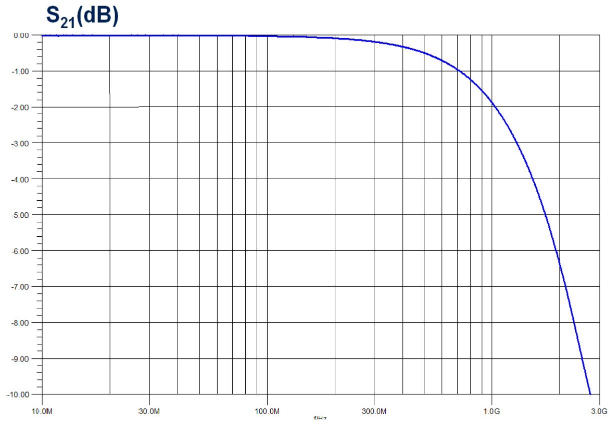


Figure 13. **Response to ISO 7637-3 pulse 2a: +85 V**



Note: DCC (direct capacitive coupling) for Figure 10, Figure 11, Figure 12 and Figure 13.

Figure 14. S21 measurements results

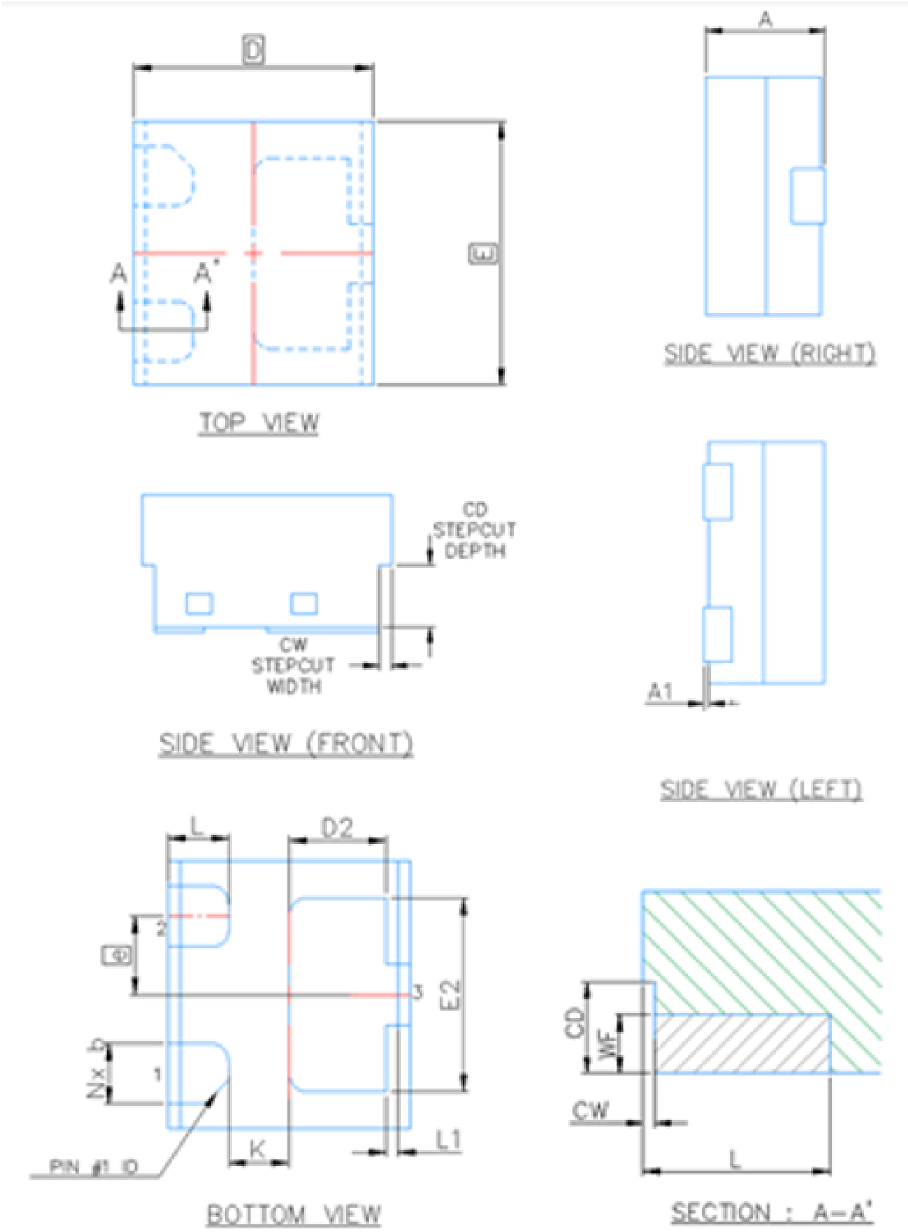


2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 QFN-3L 1.1 x 1.0 x 0.55 package information

Figure 15. QFN-3L 1.1 x 1.0 x 0.55 package outline



Note: The marking codes can be rotated to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

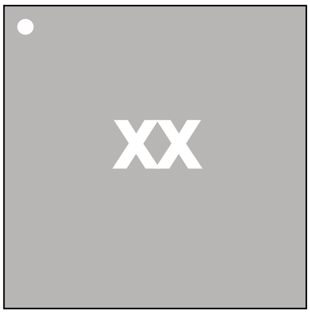
Table 3. **QFN-3L 1.1 x 1.0 x 0.55 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches[(1)]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.0201	0.0217	0.0236
A1	0.00	0.02	0.05	0.000	0.0008	0.0020
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
D	0.95	1.00	1.05	0.0374	0.0394	0.0413
D2	0.25	0.40	0.50	0.0098	0.0157	0.0197
e		0.33			0.0130	
E	1.05	1.10	1.15	0.0413	0.0433	0.0453
E2	0.65	0.80	0.90	0.0256	0.0315	0.0354
K	0.20			0.0079		
L	0.15	0.25	0.35	0.0059	0.0098	0.0138
L1	0.00	0.05	0.10	0.000	0.0020	0.0039
N	3			3		
CD	0.23			0.0091		
CW	0.02	0.05	0.08	0.0008	0.0020	0.0031
WF	0.14	0.15		0.0055	0.0059	

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

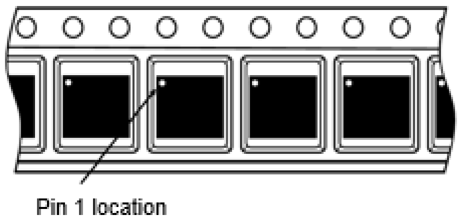
2.2 Packing information

Figure 16. Marking



The marking can be rotated to differentiate assembly location

Figure 17. Package orientation in reel



Taped according to EIA-481.
Pocket dimensions are not on scale.
Pocket shape may vary depending on package.

Figure 18. Tape and reel orientation

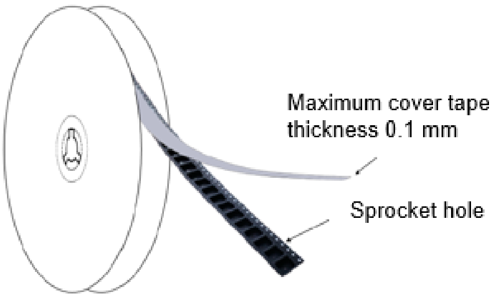


Figure 19. 7" reel dimension values

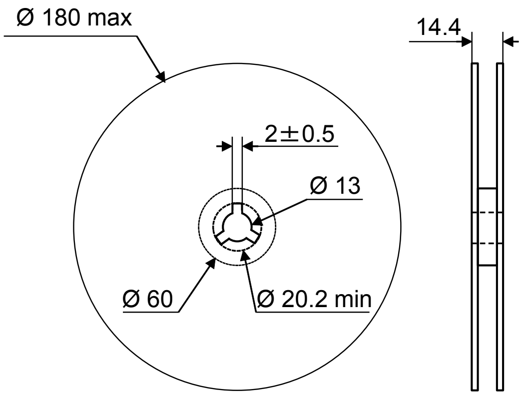


Figure 20. Inner box dimension values

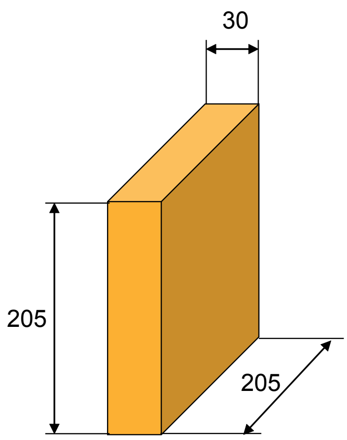


Figure 21. Tape outline

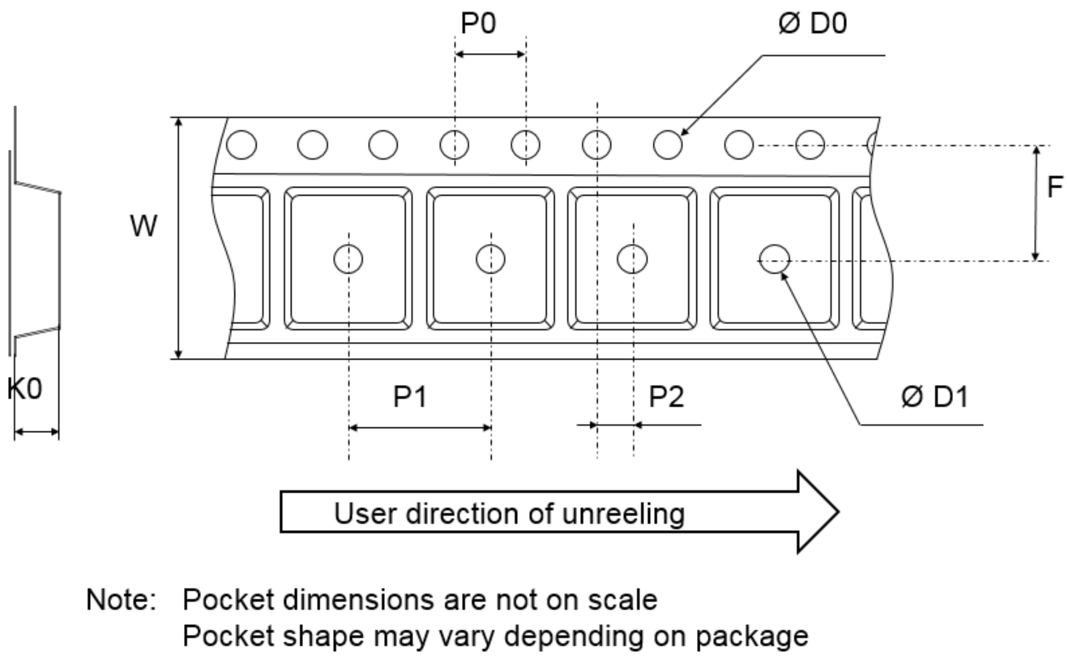


Table 4. Tape dimension values

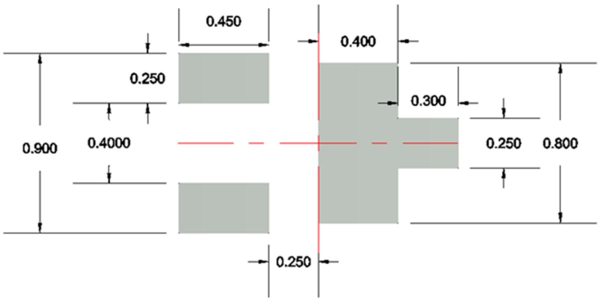
Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.50	1.55	1.60
D1	0.55	0.60	0.65
F	3.45	3.50	3.55
K0	0.67	0.70	0.73
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.10

3 Recommendation on PCB assembly

3.1 Footprint

SMD footprint design is recommended.

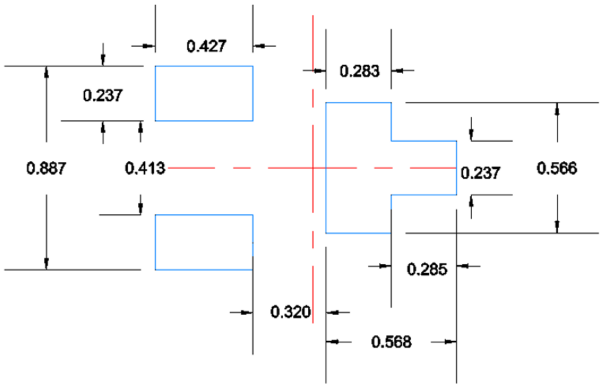
Figure 22. **Recommended footprint in mm**



3.2 Stencil opening design

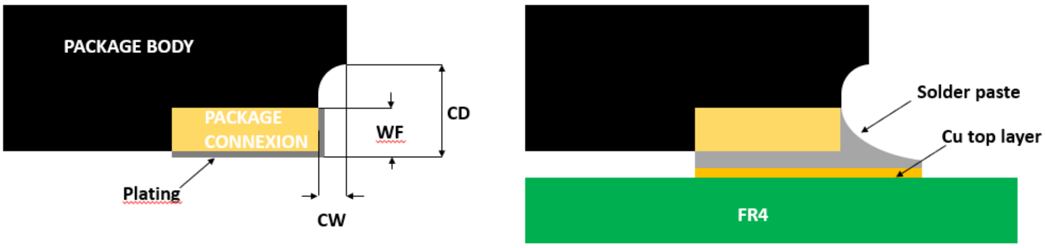
1. Reference design
   a. Stencil opening thickness: 100 µm / 4 mils
   b. I/O (pin 1 and pin 2) pads stencil aperture ratio: 90%
   c. GND (pin 3) pad stencil aperture ratio: 50%

Figure 23. **Recommended stencil window position in mm**



3.3 Wettable flank profile

Figure 24. **Wettable flank profile**



3.4 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size is 20-38 µm.

3.5 Placement

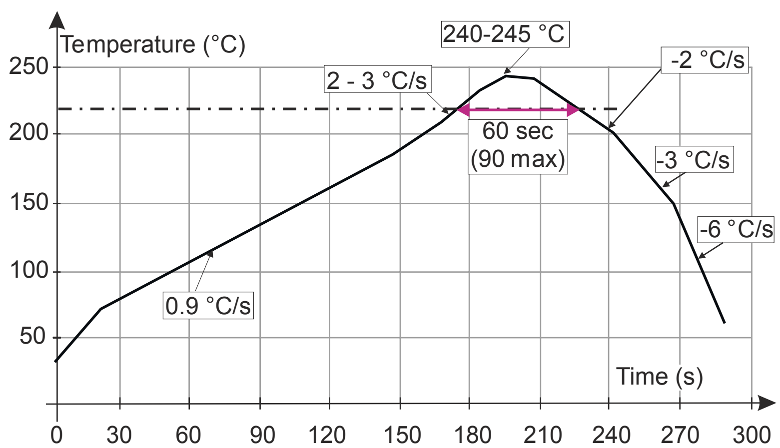
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.6 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.7 Reflow profile

Figure 25. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Table 5. Ordering information

Order code	Marking (1)	Package	Weight	Base qty.	Delivery mode
ESDCAN03-2BM3Y	YA	QFN-3L 1.1 x 1.0 x 0.55	1.68 mg	5000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 6. Document revision history

Date	Revision	Changes
05-Nov-2020	1	First issue.