

InGaAs linear image sensor G9211 to G9214/G9205 to G9208 series

Near infrared image sensors (0.9 to 1.67 μm / 2.55 μm)



G9211 to G9214/G9205 to G9208 series InGaAs linear image sensors are specifically designed for near infrared multichannel spectrophotometry. These linear image sensors consist of an InGaAs photodiode array, a charge amplifier array, an offset compensation circuit, a shift register and a timing generator formed on a CMOS chip. The charge amplifier array is made up of CMOS transistors connected to each pixel of the InGaAs photodiode array. Signals from each pixel are read out in charge integration mode to achieve high sensitivity and stable operation in the near infrared spectral range. The package is hermetically sealed for high reliability.

Signal processing circuits on the CMOS chip allow selecting a feedback capacitance (C_f) of 10 pF or 0.5 pF by using an external voltage input. The image sensor operates over a wide dynamic range when $C_f=10$ pF and delivers high gain when $C_f=0.5$ pF.

Features

- Wide dynamic range
- Low noise and low dark current
- Selectable gain
- Anti-saturation circuit
- CDS circuit *1
- Offset compensation circuit
- Simple operation (by built-in timing generator) *2
- High resolution: 25 μm pitch (512 ch)
- Low cross-talk
- 256 ch: 1 video line
512 ch: 2 video lines

Applications

- Near infrared multichannel spectrophotometry
- Radiation thermometry
- Non-destructive inspection

Related products

- InGaAs multichannel detector head C8061-01, C8062-01
- Multichannel detector head controller C7557

Selection guide

Type No.	Cooling	Number of pixels	Pixel pitch (μm)	Pixel size [μm (H) $\times$ μm (V)]	Spectral response range (μm)	Defective pixel
G9211-256S	One-stage TE-cooled	256	50	50 $\times$ 250	0.9 to 1.70	1 % Max. *3
G9212-512S		512	25	25 $\times$ 250		
G9213-256S		256	50	50 $\times$ 500		
G9214-512S		512	25	25 $\times$ 500		
G9205-256W	Two-stage TE-cooled	256	50	50 $\times$ 250	0.9 to 1.85	5 % Max.
G9206-256W					0.9 to 2.05	
G9207-256W					0.9 to 2.25	
G9208-256W					0.9 to 2.55	

*1: CDS (Correlated Double Sampling) circuit

A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.

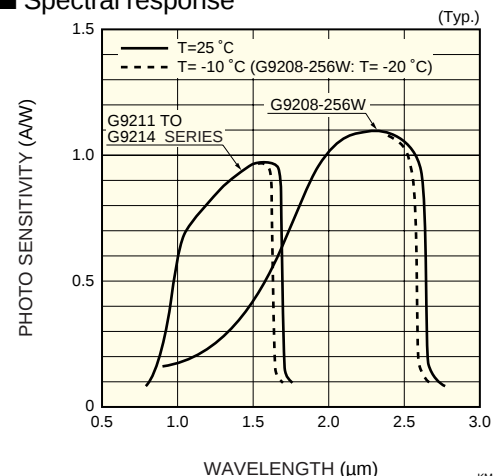
*2: Timing generator

Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (Programmable Logic Devices) are used to input the required timing signals. However, G9211 to G9214/G9205 to G9208 series image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

*3: Percentage of defective pixels

If your application requires sensors with no defective pixels, please select G9201 series.

Spectral response



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Absolute maximum ratings

Parameter	Symbol	Value	Unit
Clock pulse voltage	V_{ϕ}	5.5	V
Operating temperature *1	T_{opr}	-40 to +70	°C
Storage temperature *1	T_{stg}	-40 to +85	°C

*1: Non condensation

Electrical characteristics ($T_a=25^{\circ}\text{C}$, $V_{\phi}=5\text{ V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vdd	4.5	5.0	5.5	V
	Vref	-	1.26	-	
Ground	Vss	-	0	-	V
Element bias	INP	3.5	4.5	4.6	V
Clock frequency	f	0.1	-	4	MHz
Clock pulse voltage	V_{ϕ}	$V_{\phi} - 0.5$	V_{ϕ}	$V_{\phi} + 0.5$	V
		0	0	0.4	V
Clock pulse rise/fall times	$t_{r\phi}$	0	20	100	ns
	$t_{f\phi}$				
Clock pulse width	tpw_{ϕ}	200	-	-	ns
Reset pulse voltage	V (RES)	$V_{\phi} - 0.5$	V_{ϕ}	$V_{\phi} + 0.5$	V
		0	0	0.4	V
Reset pulse rise/fall times	$t_{r(RES)}$	0	20	100	ns
	$t_{f(RES)}$				
Reset pulse width	$tpw(RES)$	6000	-	-	ns
Video output voltage	V_H	-	4.1	-	V
	V_L	-	1.26	-	
Data rate	fV	-	f/8	-	Hz

Electrical and optical characteristics (G9211 to G9214 series: $T=25^{\circ}\text{C}$, G9205 to G9208 series: $T=-20^{\circ}\text{C}$)

Parameter	Symbol	G9211 to G9214 series			G9205 to G9208 series				Unit
		Min.	Typ.	Max.		Min.	Typ.	Max.	
Peak sensitivity wavelength	λ_p	-	1.55	-	G9205	-	1.75	-	μm
					G9206	-	1.95	-	
					G9207	-	2.05	-	
					G9208	-	2.3	-	
Saturation charge *2	Qsat	-	30	-		-	30	-	pC
RMS noise voltage (Readout noise)	N	-	180	300		-	180	300	μV_{rms}
Photo response non-uniformity	PRNU	-	-	± 5 *3		-	-	± 10 *4	%

*2: $V_{\phi}=5\text{ V}$, $C_f=10\text{ pF}$

*3: 50 % of saturation, integration time: 10 ms, after dark output subtraction, excluding first and last pixels.

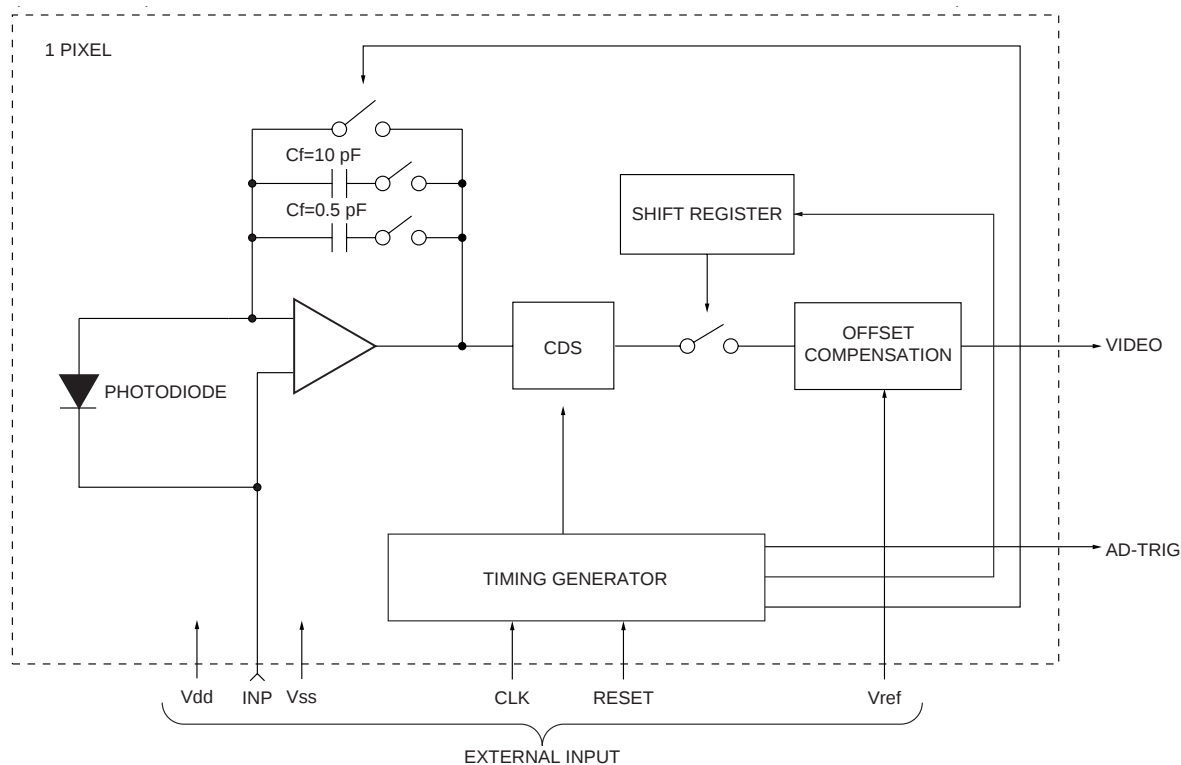
*4: 50 % of saturation, integration time: 3 ms, after dark output subtraction, excluding first and last pixels.

Dark current characteristics ($T=25^{\circ}\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
G9211-256S	I_D	-	2	10	pA
G9212-512S		-	1	5	
G9213-256S		-	4	20	
G9214-512S		-	1	5	
G9205-256W *5		-	15	60	
G9206-256W *5		-	30	120	
G9207-256W *5		-	200	800	
G9208-256W *5		-	500	2000	

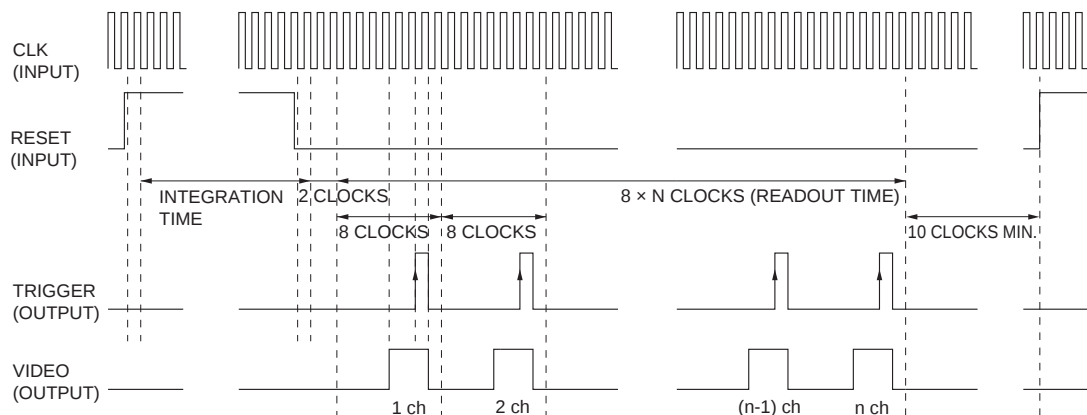
*5: $T_D=-20^{\circ}\text{C}$

■ Equivalent circuit



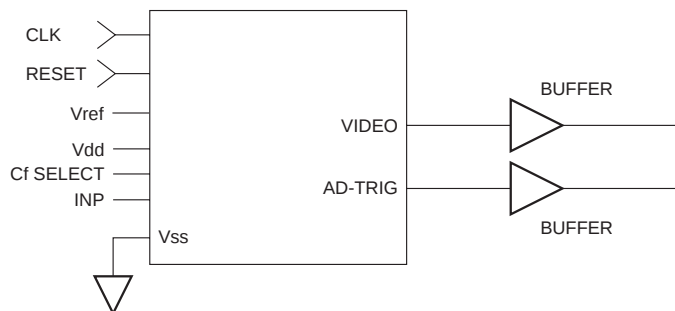
■ Timing chart

KMIRC0010EB



■ Basic circuit connection

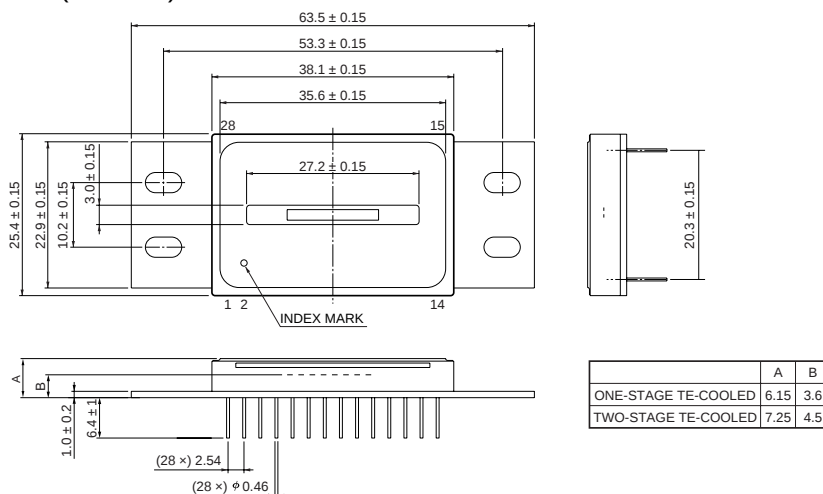
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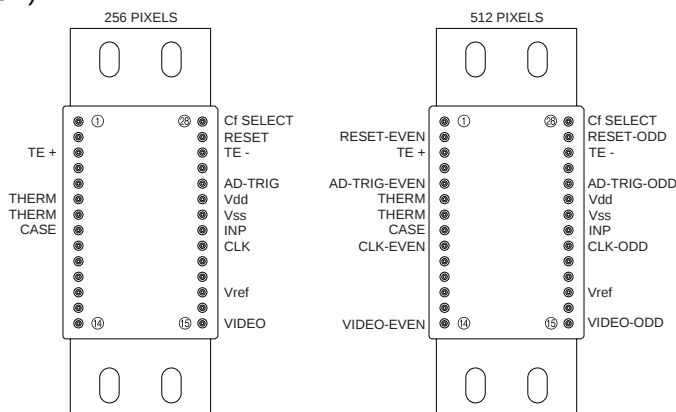
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Dimensional outline (unit: mm)



KMIRA0011EA

Pin connection (top view)



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Terminal name	Input/Output	Function and recommended connection
CLK	Input (CMOS logic compatible)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic compatible)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. The width of the reset pulse is integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit on the CMOS chip.
Vss	-	Ground for the signal processing circuit on the CMOS chip.
INP	Input	Reset voltage for the charge amplifier array on the CMOS chip.
Cf SELECT	Input	Voltage that determines the feedback capacitance (Cf) on the CMOS chip. Cf=10 pF at 0 V, and Cf=0.5 pF at 5 V.
CASE	-	This terminal is electrically connected to the package.
THERM	-	Thermistor for monitoring temperature inside the package.
TE+, TE-	-	Power supply terminal for the thermoelectric cooler that cools the photodiode array. No connection for room temperature operation type.
AD-TRIG	Output	Digital signal for AD conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit at the CMOS chip

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