



## SN74LVC1G3157-Q1 Single-Pole Double-Throw Analog Switch

### 1 Features

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 1.65-V to 5.5-V  $V_{CC}$  Operation
- Useful for Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity
- High Speed, Typically 0.5 ns ( $V_{CC} = 3$  V,  $C_L = 50$  pF)
- Low ON-State Resistance, Typically  $\approx 6$   $\Omega$  ( $V_{CC} = 4.5$  V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

### 2 Applications

Advanced Driver Assistance Systems (ADAS)

### 3 Description

The SN74LVC1G3157-Q1 device is a single-pole double-throw (SPDT) analog switch designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to  $V_{CC}$  (peak) to be transmitted in either direction.

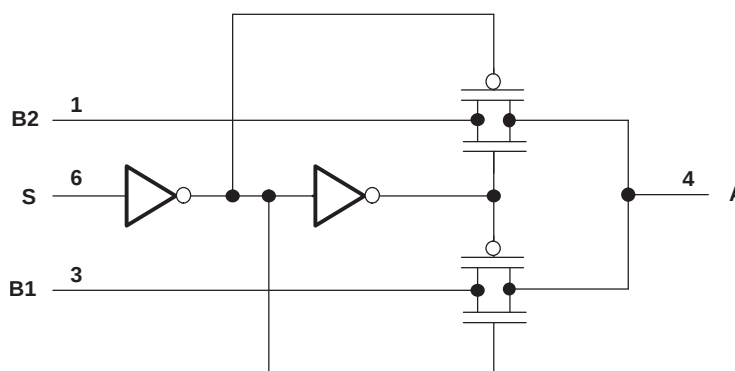
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

#### Device Information<sup>(1)</sup>

| PART NUMBER      | PACKAGE    | BODY SIZE (NOM)   |
|------------------|------------|-------------------|
| SN74LVC1G3157-Q1 | SOT-23 (6) | 2.90 mm × 1.60 mm |
|                  | SC70 (6)   | 2.00 mm × 1.25 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



## Table of Contents

|                                                  |           |                                                                  |           |
|--------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                          | <b>1</b>  | 8.2 Functional Block Diagram .....                               | 14        |
| <b>2 Applications</b> .....                      | <b>1</b>  | 8.3 Feature Description.....                                     | 14        |
| <b>3 Description</b> .....                       | <b>1</b>  | 8.4 Device Functional Modes.....                                 | 14        |
| <b>4 Revision History</b> .....                  | <b>2</b>  | <b>9 Application and Implementation</b> .....                    | <b>15</b> |
| <b>5 Pin Configuration and Functions</b> .....   | <b>3</b>  | 9.1 Application Information.....                                 | 15        |
| <b>6 Specifications</b> .....                    | <b>4</b>  | 9.2 Typical Application .....                                    | 15        |
| 6.1 Absolute Maximum Ratings .....               | 4         | <b>10 Power Supply Recommendations</b> .....                     | <b>17</b> |
| 6.2 ESD Ratings.....                             | 4         | <b>11 Layout</b> .....                                           | <b>17</b> |
| 6.3 Recommended Operating Conditions.....        | 5         | 11.1 Layout Guidelines .....                                     | 17        |
| 6.4 Thermal Information .....                    | 5         | 11.2 Layout Example .....                                        | 17        |
| 6.5 Electrical Characteristics.....              | 6         | <b>12 Device and Documentation Support</b> .....                 | <b>18</b> |
| 6.6 Switching Characteristics .....              | 7         | 12.1 Documentation Support .....                                 | 18        |
| 6.7 Analog Switch Characteristics .....          | 7         | 12.2 Trademarks .....                                            | 18        |
| 6.8 Typical Characteristics.....                 | 8         | 12.3 Electrostatic Discharge Caution.....                        | 18        |
| <b>7 Parameter Measurement Information</b> ..... | <b>8</b>  | 12.4 Glossary .....                                              | 18        |
| <b>8 Detailed Description</b> .....              | <b>14</b> | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>18</b> |
| 8.1 Overview .....                               | 14        |                                                                  |           |

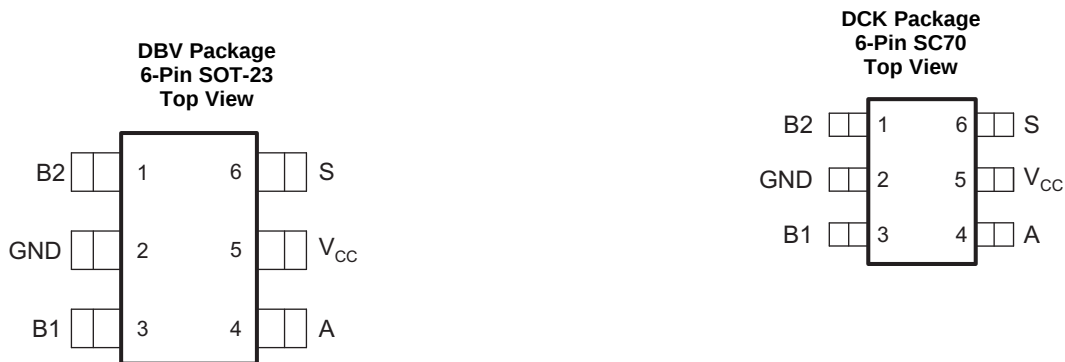
## 4 Revision History

### Changes from Revision E (April 2008) to Revision F

Page

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

## 5 Pin Configuration and Functions



See mechanical drawings for dimensions.

### Pin Functions

| PIN |      | I/O | DESCRIPTION     |
|-----|------|-----|-----------------|
| NO. | NAME |     |                 |
| 1   | B2   | I/O | Second terminal |
| 2   | GND  | —   | Ground          |
| 3   | B1   | I/O | First terminal  |
| 4   | A    | I/O | Common terminal |
| 5   | VCC  | I   | Power supply    |
| 6   | S    | I   | Select          |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                   |                                                        | MIN  | MAX                   | UNIT |
|------------------|---------------------------------------------------|--------------------------------------------------------|------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>                     |                                                        | –0.5 | 6.5                   | V    |
| V <sub>IN</sub>  | Control input voltage <sup>(2)(3)</sup>           |                                                        | –0.5 | 6.5                   | V    |
| V <sub>I/O</sub> | Switch I/O voltage <sup>(2)(3)(4)(5)</sup>        |                                                        | –0.5 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Control input clamp current                       | V <sub>IN</sub> < 0                                    | –50  |                       | mA   |
| I <sub>I/O</sub> | I/O port diode current                            | V <sub>I/O</sub> < 0                                   | –50  |                       | mA   |
| I <sub>I/O</sub> | ON-state switch current                           | V <sub>I/O</sub> = 0 to V <sub>CC</sub> <sup>(6)</sup> |      | ±128                  | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                                                        |      | ±100                  | mA   |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(7)</sup>          | DBV package                                            |      | 165                   | °C/W |
|                  |                                                   | DCK package                                            |      | 258                   |      |
| T <sub>stg</sub> | Storage temperature                               |                                                        | –65  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) V<sub>I</sub>, V<sub>O</sub>, V<sub>A</sub>, and V<sub>BN</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (6) I<sub>I</sub>, I<sub>O</sub>, I<sub>A</sub>, and I<sub>BN</sub> are used to denote specific conditions for I<sub>I/O</sub>.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

### 6.2 ESD Ratings

|                    |                         |                                                          | VALUE | UNIT |
|--------------------|-------------------------|----------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), performed per JEDEC (JESD22)     | ±2000 | V    |
|                    |                         | Charged device model (CDM), performed per JEDEC (JESD22) | ±1000 |      |
|                    |                         |                                                          | ±1000 |      |

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                         |                                    | MIN                    | NOM | MAX             | UNIT |
|------------------|-----------------------------------------|------------------------------------|------------------------|-----|-----------------|------|
| V <sub>CC</sub>  |                                         |                                    | 1.65                   |     | 5.5             | V    |
| V <sub>I/O</sub> |                                         |                                    | 0                      |     | V <sub>CC</sub> | V    |
| V <sub>IN</sub>  |                                         |                                    | 0                      |     | 5.5             | V    |
| V <sub>IH</sub>  | High-level input voltage, control input | V <sub>CC</sub> = 1.65 V to 1.95 V | V <sub>CC</sub> × 0.75 |     |                 | V    |
|                  |                                         | V <sub>CC</sub> = 2.3 V to 5.5 V   | V <sub>CC</sub> × 0.7  |     |                 |      |
| V <sub>IL</sub>  | Low-level input voltage, control input  | V <sub>CC</sub> = 1.65 V to 1.95 V | V <sub>CC</sub> × 0.25 |     |                 | V    |
|                  |                                         | V <sub>CC</sub> = 2.3 V to 5.5 V   | V <sub>CC</sub> × 0.3  |     |                 |      |
| Δt/Δv            | Input transition rise/fall time         | V <sub>CC</sub> = 1.65 V to 1.95 V | 20                     |     |                 | ns/V |
|                  |                                         | V <sub>CC</sub> = 2.3 V to 2.7 V   | 20                     |     |                 |      |
|                  |                                         | V <sub>CC</sub> = 3 V to 3.6 V     | 10                     |     |                 |      |
|                  |                                         | V <sub>CC</sub> = 4.5 V to 5.5 V   | 10                     |     |                 |      |
| T <sub>A</sub>   |                                         |                                    | −40                    |     | 125             | °C   |

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVC1G3157-Q1 |            | UNIT |
|-------------------------------|----------------------------------------------|------------------|------------|------|
|                               |                                              | DBV (SOT-23)     | DCK (SC70) |      |
|                               |                                              | 6 PINS           | 6 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 201.8            | 233.8      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 103.7            | 107.9      |      |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 51.8             | 52.7       |      |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 12               | 4.9        |      |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 51.4             | 52.4       |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |                                                                         | TEST CONDITIONS                                                               |                                                   | V <sub>CC</sub> | MIN | TYP <sup>(1)</sup> | MAX                     | UNIT |
|---------------------------------|-------------------------------------------------------------------------|-------------------------------------------------------------------------------|---------------------------------------------------|-----------------|-----|--------------------|-------------------------|------|
| r <sub>on</sub>                 | ON-state switch resistance <sup>(2)</sup>                               | See Figure 2 and Figure 1                                                     | V <sub>I</sub> = 0 V, I <sub>O</sub> = 4 mA       | 1.65 V          |     | 11                 | 20                      | Ω    |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 1.65 V, I <sub>O</sub> = –4 mA   |                 |     | 15                 | 50                      |      |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 0 V, I <sub>O</sub> = 8 mA       | 2.3 V           |     | 8                  | 12                      |      |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 2.3 V, I <sub>O</sub> = –8 mA    |                 |     | 11                 | 30                      |      |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 0 V, I <sub>O</sub> = 24 mA      | 3 V             |     | 7                  | 9.5                     |      |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 3 V, I <sub>O</sub> = –24 mA     |                 |     | 9                  | 20                      |      |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 0 V, I <sub>O</sub> = 30 mA      | 4.5 V           |     | 6                  | 7.5                     |      |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 2.4 V, I <sub>O</sub> = –30 mA   |                 |     | 7                  | 12                      |      |
|                                 |                                                                         |                                                                               | V <sub>I</sub> = 4.5 V, I <sub>O</sub> = –30 mA   |                 |     | 7                  | 15                      |      |
| r <sub>range</sub>              | ON-state switch resistance over signal range <sup>(2)(3)</sup>          | 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub> (see Figure 2 and Figure 1)             | I <sub>A</sub> = –4 mA                            | 1.65 V          |     |                    | 140                     | Ω    |
|                                 |                                                                         |                                                                               | I <sub>A</sub> = –8 mA                            | 2.3 V           |     |                    | 45                      |      |
|                                 |                                                                         |                                                                               | I <sub>A</sub> = –24 mA                           | 3 V             |     |                    | 18                      |      |
|                                 |                                                                         |                                                                               | I <sub>A</sub> = –30 mA                           | 4.5 V           |     |                    | 10                      |      |
| Δr <sub>on</sub>                | Difference in on-state resistance between switches <sup>(2)(4)(5)</sup> | See Figure 2                                                                  | V <sub>Bn</sub> = 1.15 V, I <sub>A</sub> = –4 mA  | 1.65 V          |     | 0.5                |                         | Ω    |
|                                 |                                                                         |                                                                               | V <sub>Bn</sub> = 1.6 V, I <sub>A</sub> = –8 mA   | 2.3 V           |     | 0.1                |                         |      |
|                                 |                                                                         |                                                                               | V <sub>Bn</sub> = 2.1 V, I <sub>A</sub> = –24 mA  | 3 V             |     | 0.1                |                         |      |
|                                 |                                                                         |                                                                               | V <sub>Bn</sub> = 3.15 V, I <sub>A</sub> = –30 mA | 4.5 V           |     | 0.1                |                         |      |
| r <sub>on(flat)</sub>           | ON-state resistance flatness <sup>(2)(4)(6)</sup>                       | 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>                                         | I <sub>A</sub> = –4 mA                            | 1.65 V          |     |                    | 110                     | Ω    |
|                                 |                                                                         |                                                                               | I <sub>A</sub> = –8 mA                            | 2.3 V           |     |                    | 26                      |      |
|                                 |                                                                         |                                                                               | I <sub>A</sub> = –24 mA                           | 3 V             |     |                    | 9                       |      |
|                                 |                                                                         |                                                                               | I <sub>A</sub> = –30 mA                           | 4.5 V           |     |                    | 4                       |      |
| I <sub>off</sub> <sup>(7)</sup> | OFF-state switch leakage current                                        | 0 ≤ V <sub>I</sub> , V <sub>O</sub> ≤ V <sub>CC</sub> (see Figure 3)          |                                                   | 1.65 V to 5.5 V |     | ±1                 | ±1 <sup>(1)</sup>       | μA   |
| I <sub>S(on)</sub>              | ON-state switch leakage current                                         | V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = Open (see Figure 4) |                                                   | 5.5 V           |     | ±1                 | ±0.1 <sup>(1)</sup>     | μA   |
| I <sub>IN</sub>                 | Control input current                                                   | 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                         |                                                   | 0 V to 5.5 V    |     | ±1                 | ±0.05 ±1 <sup>(1)</sup> | μA   |
| I <sub>CC</sub>                 | Supply current                                                          | V <sub>IN</sub> = V <sub>CC</sub> or GND                                      |                                                   | 5.5 V           |     | 1                  | 10                      | μA   |
| ΔI <sub>CC</sub>                | Supply-current change                                                   | V <sub>IN</sub> = V <sub>CC</sub> – 0.6 V                                     |                                                   | 5.5 V           |     |                    | 500                     | μA   |
| C <sub>in</sub>                 | Control input capacitance                                               | S                                                                             |                                                   | 5 V             |     | 2.7                |                         | pF   |
| C <sub>io(off)</sub>            | Switch I/O capacitance                                                  | Bn                                                                            |                                                   | 5 V             |     | 5.2                |                         | pF   |
| C <sub>io(on)</sub>             | Switch I/O capacitance                                                  | Bn                                                                            |                                                   | 5 V             |     | 17.3               |                         | pF   |
|                                 |                                                                         | A                                                                             |                                                   |                 |     | 17.3               |                         |      |

(1) T<sub>A</sub> = 25°C

(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.

(3) Specified by design

(4) Δr<sub>on</sub> = r<sub>on(max)</sub> – r<sub>on(min)</sub> measured at identical V<sub>CC</sub>, temperature, and voltage levels

(5) This parameter is characterized, but not tested in production.

(6) Flatness is defined as the difference between the maximum and minimum values of ON-state resistance over the specified range of conditions.

(7) I<sub>off</sub> is the same as I<sub>S(off)</sub> (OFF-state switch leakage current).

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 5](#) and [Figure 11](#))

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     | UNIT |
|-----------------|-----------------|----------------|-------------------------------------------|-----|------------------------------------------|-----|------------------------------------------|-----|----------------------------------------|-----|------|
|                 |                 |                | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $t_{pd}^{(1)}$  | A or Bn         | Bn or A        |                                           | 2   |                                          | 1.2 |                                          | 0.8 |                                        | 0.3 | ns   |
| $t_{en}^{(2)}$  | S               | Bn             | 7                                         | 24  | 3.5                                      | 14  | 2.5                                      | 7.6 | 1.7                                    | 5.7 | ns   |
| $t_{dis}^{(3)}$ |                 |                | 3                                         | 13  | 2                                        | 7.5 | 1.5                                      | 5.3 | 0.8                                    | 3.8 |      |
| $t_{B-M}^{(4)}$ |                 |                | 0.5                                       |     | 0.5                                      |     | 0.5                                      |     | 0.5                                    |     |      |

- (1)  $t_{pd}$  is the slower of  $t_{PLH}$  or  $t_{PHL}$ . Propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
- (2)  $t_{en}$  is the slower of  $t_{PZL}$  or  $t_{PZH}$ .
- (3)  $t_{dis}$  is the slower of  $t_{PLZ}$  or  $t_{PHZ}$ .
- (4) Specified by design

## 6.7 Analog Switch Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER                                              | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                                                                                                                                    | $V_{CC}$ | TYP    | UNIT |
|--------------------------------------------------------|-----------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------|------|
| Frequency response<br>(switch on) <sup>(1)</sup>       | A or Bn         | Bn or A        | $R_L = 50\ \Omega$ ,<br>$f_{in} = \text{sine wave}$<br>(see <a href="#">Figure 6</a> )                                                             | 1.65 V   | 300    | MHz  |
|                                                        |                 |                |                                                                                                                                                    | 2.3 V    | 300    |      |
|                                                        |                 |                |                                                                                                                                                    | 3 V      | 300    |      |
|                                                        |                 |                |                                                                                                                                                    | 4.5 V    | 300    |      |
| Crosstalk<br>(between switches) <sup>(2)</sup>         | B1 or B2        | B2 or B1       | $R_L = 50\ \Omega$ ,<br>$f_{in} = 10\text{ MHz}$ (sine wave)<br>(see <a href="#">Figure 7</a> )                                                    | 1.65 V   | –54    | dB   |
|                                                        |                 |                |                                                                                                                                                    | 2.3 V    | –54    |      |
|                                                        |                 |                |                                                                                                                                                    | 3 V      | –54    |      |
|                                                        |                 |                |                                                                                                                                                    | 4.5 V    | –54    |      |
| Feedthrough attenuation<br>(switch off) <sup>(2)</sup> | A or Bn         | Bn or A        | $C_L = 5\text{ pF}$ , $R_L = 50\ \Omega$ ,<br>$f_{in} = 10\text{ MHz}$ (sine wave)<br>(see <a href="#">Figure 8</a> )                              | 1.65 V   | –57    | dB   |
|                                                        |                 |                |                                                                                                                                                    | 2.3 V    | –57    |      |
|                                                        |                 |                |                                                                                                                                                    | 3 V      | –57    |      |
|                                                        |                 |                |                                                                                                                                                    | 4.5 V    | –57    |      |
| Charge injection <sup>(3)</sup>                        | S               | A              | $C_L = 0.1\text{ nF}$ , $R_L = 1\text{ M}\Omega$<br>(see <a href="#">Figure 9</a> )                                                                | 3.3 V    | 3      | pC   |
|                                                        |                 |                |                                                                                                                                                    | 5 V      | 7      |      |
| Total harmonic distortion                              | A or Bn         | Bn or A        | $V_I = 0.5\text{ V}_{p-p}$ , $R_L = 600\ \Omega$ ,<br>$f_{in} = 600\text{ Hz to }20\text{ kHz}$<br>(sine wave)<br>(see <a href="#">Figure 10</a> ) | 1.65%    | 0.1%   | V    |
|                                                        |                 |                |                                                                                                                                                    | 2.3%     | 0.025% |      |
|                                                        |                 |                |                                                                                                                                                    | 3%       | 0.015% |      |
|                                                        |                 |                |                                                                                                                                                    | 4.5%     | 0.01%  |      |

- (1) Adjust  $f_{in}$  voltage to obtain 0 dBm at output. Increase  $f_{in}$  frequency until dB meter reads –3 dB.
- (2) Adjust  $f_{in}$  voltage to obtain 0 dBm at input.
- (3) Specified by design

## 6.8 Typical Characteristics

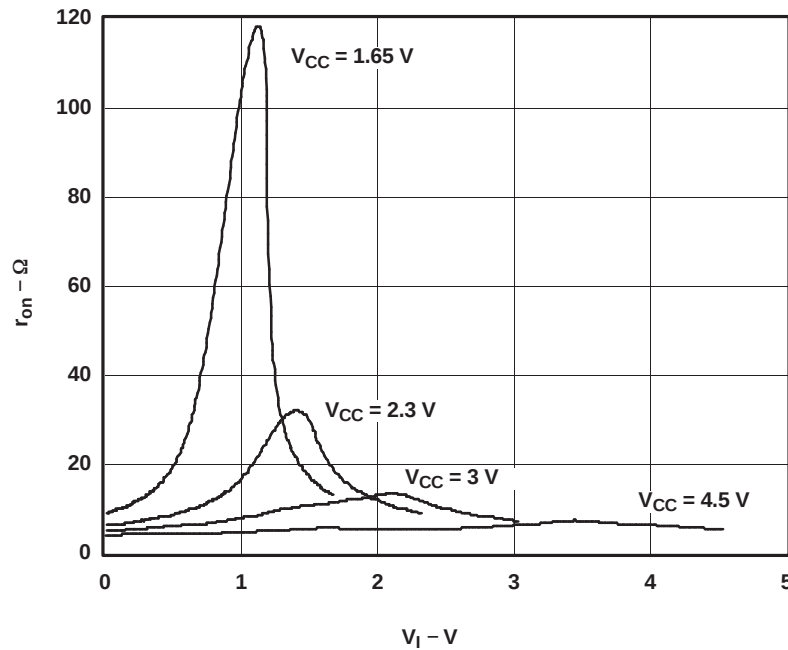


Figure 1. Typical  $R_{on}$  as a Function of Input Voltage ( $V_I$ ) for  $V_I = 0$  To  $V_{CC}$

## 7 Parameter Measurement Information

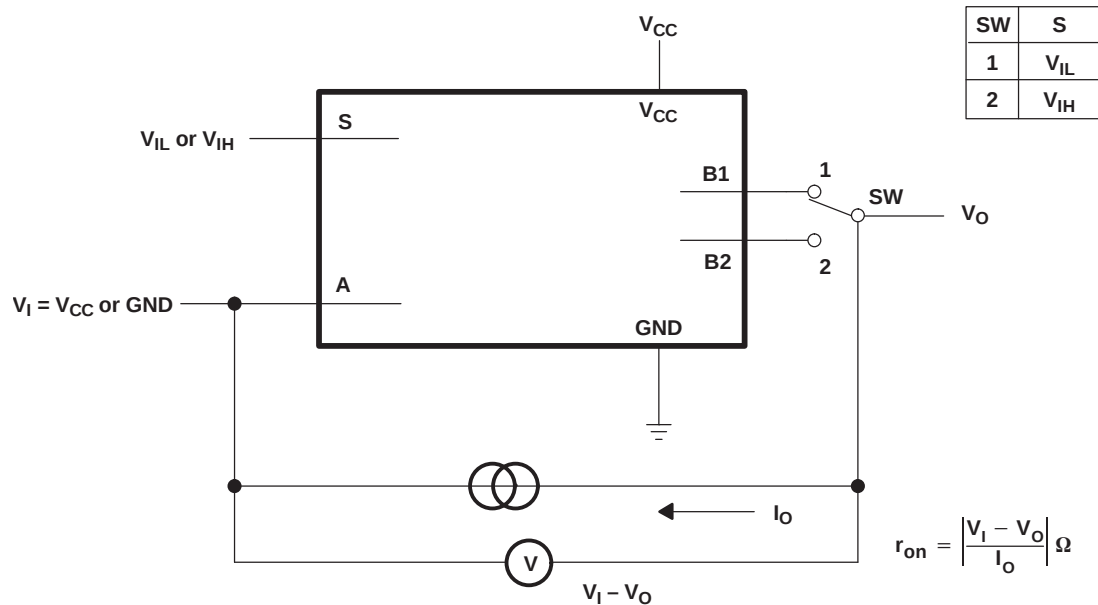
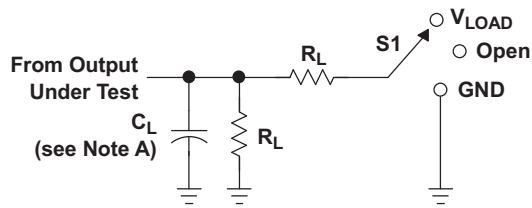


Figure 2. ON-State Resistance Test Circuit

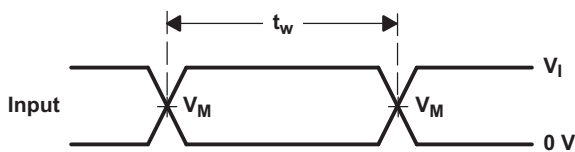
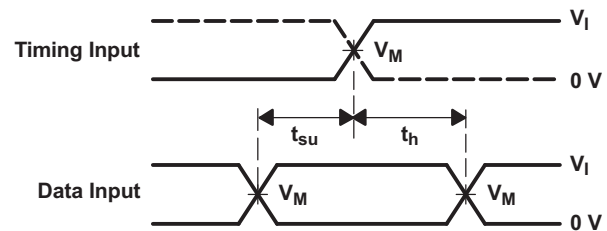
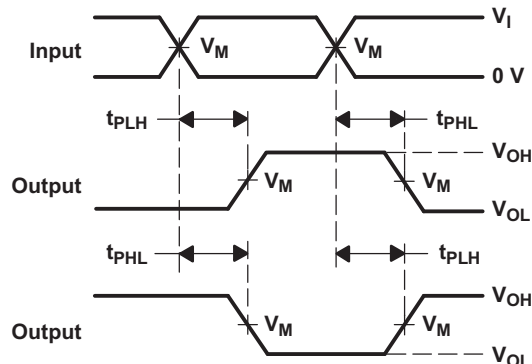
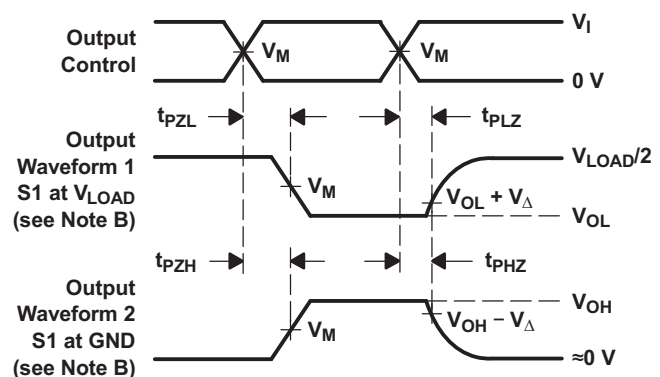


## Parameter Measurement Information (continued)


**LOAD CIRCUIT**

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

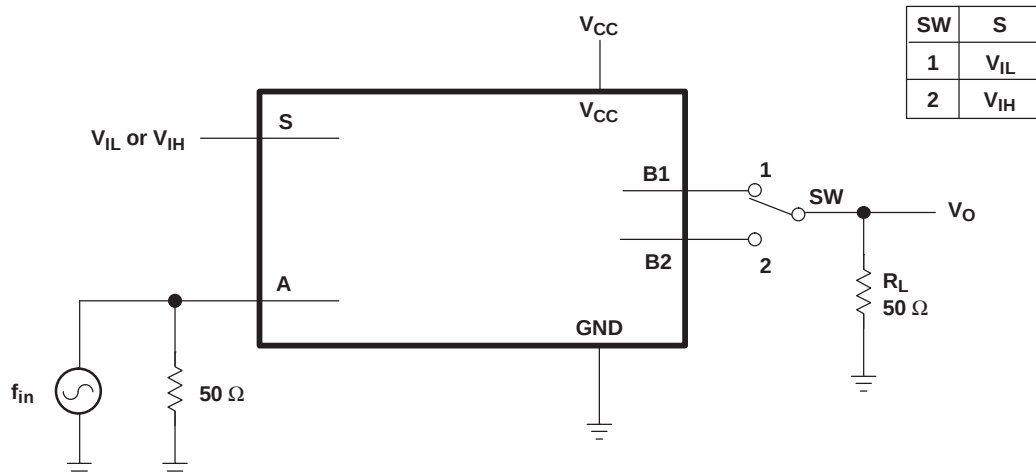
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |


**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

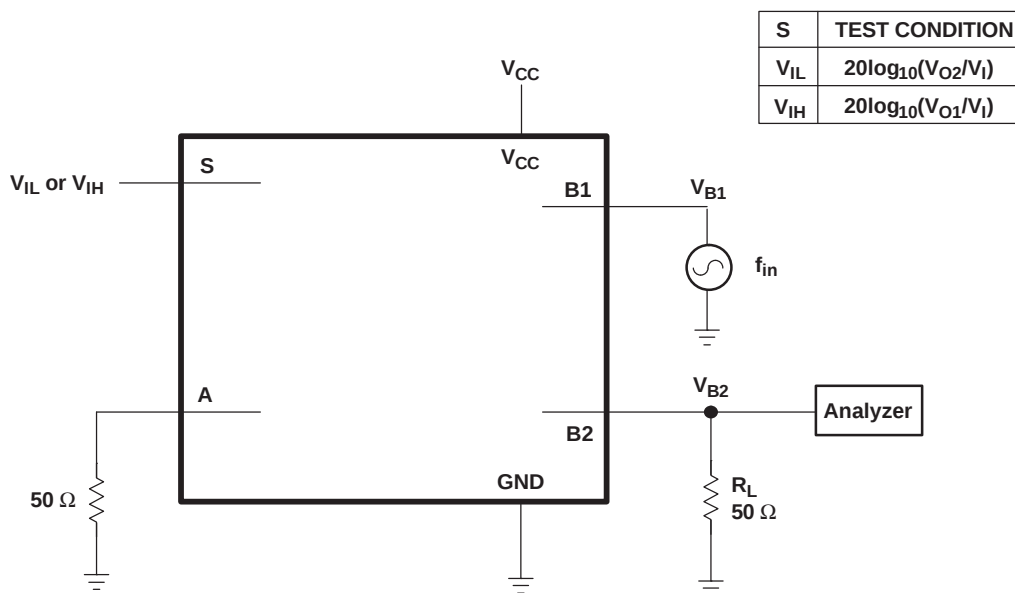
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 5. Load Circuit and Voltage Waveforms**

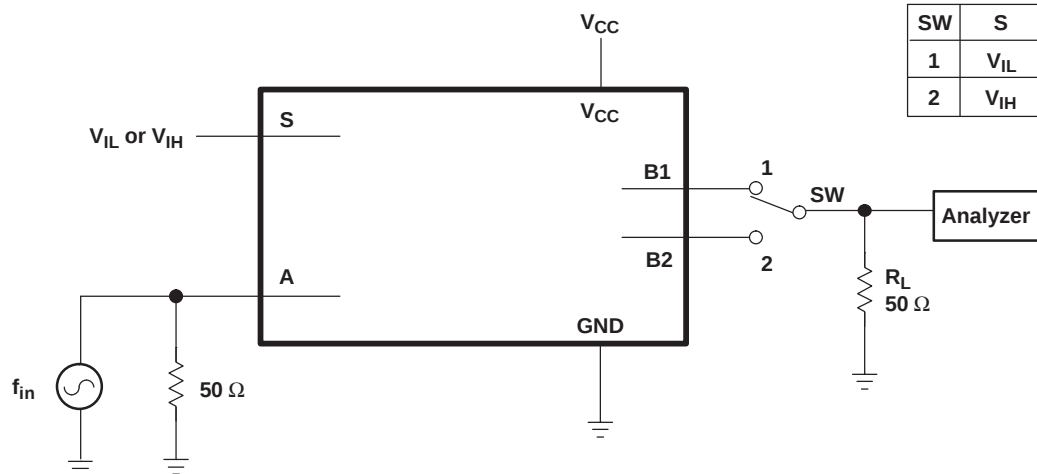
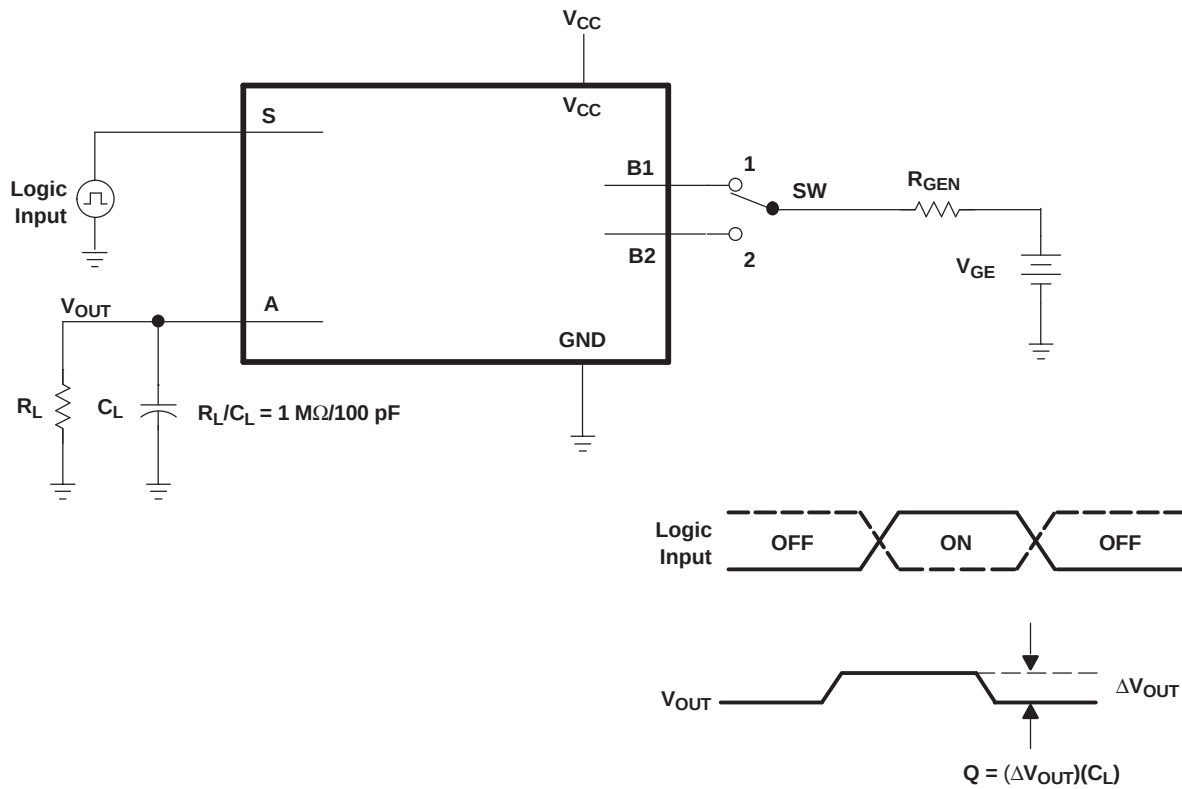
## Parameter Measurement Information (continued)



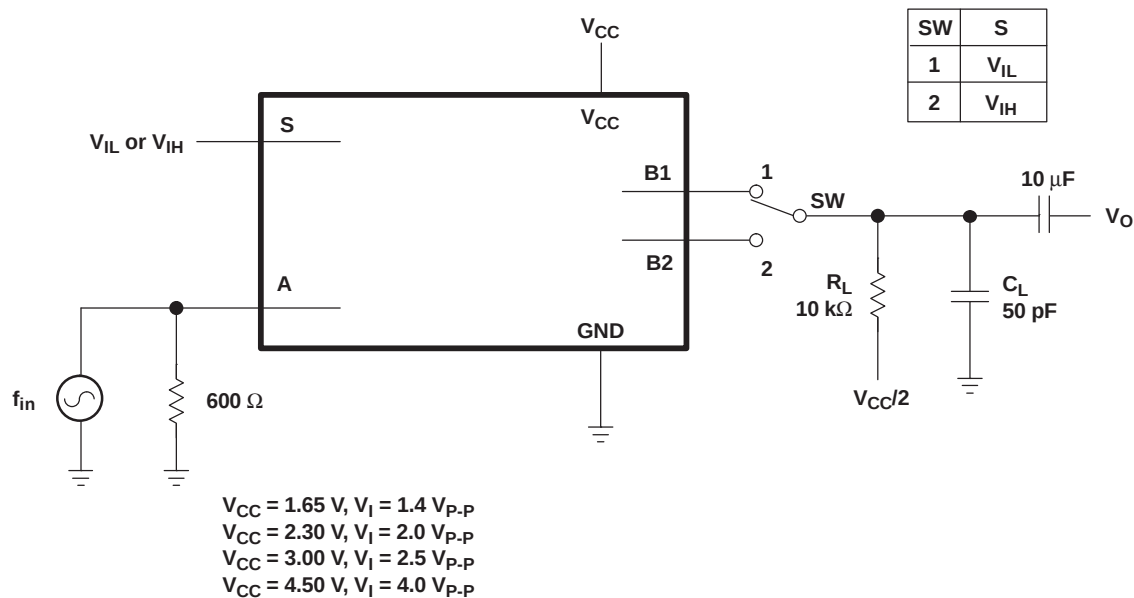
**Figure 6. Frequency Response (Switch On)**



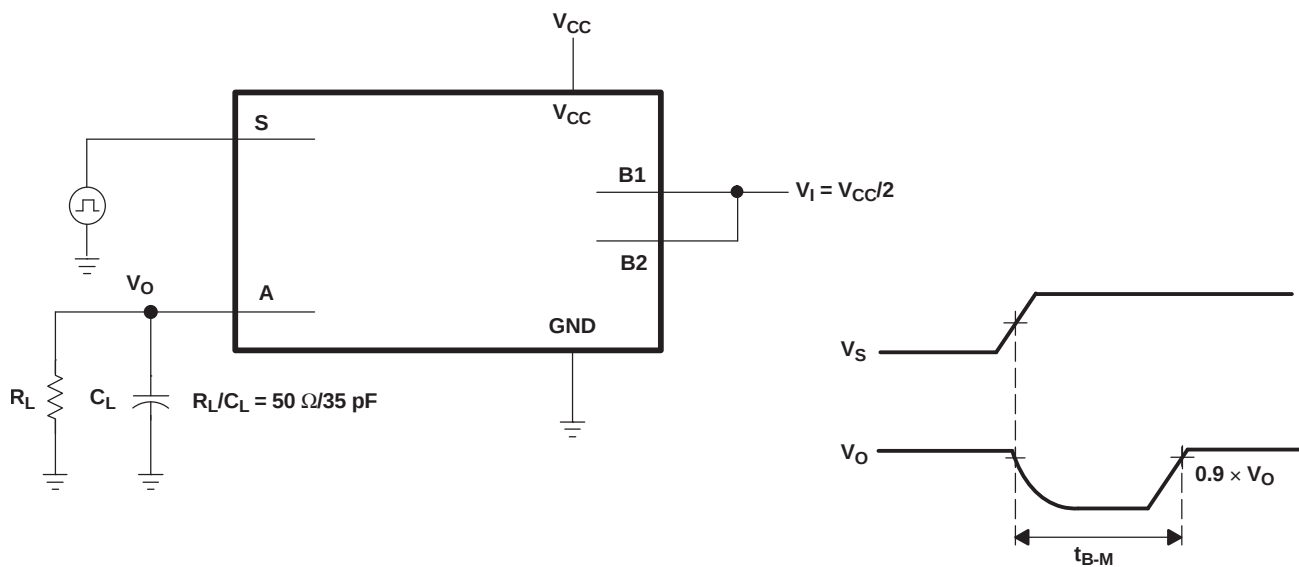
**Figure 7. Crosstalk (Between Switches)**

**Parameter Measurement Information (continued)**

**Figure 8. Feedthrough**

**Figure 9. Charge-Injection Test**

**Parameter Measurement Information (continued)**



**Figure 10. Total Harmonic Distortion**



**Figure 11. Break-Before-Make Internal Timing**

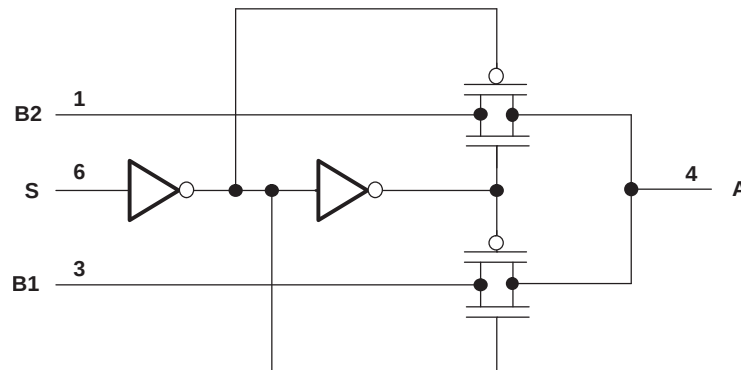
## 8 Detailed Description

### 8.1 Overview

The SN74LVC1G3157-Q1 device is a single-pole double-throw (SPDT) analog switch designed for 1.65-V to 5.5-V

$V_{CC}$  operation. The SN74LVC1G3157-Q1 device can handle analog and digital signals. The device permits signals with amplitudes of up to  $V_{CC}$  (peak) to be transmitted in either direction.

### 8.2 Functional Block Diagram



**Figure 12. Logic Diagram (Positive Logic)**

### 8.3 Feature Description

These devices are qualified for automotive applications. The 1.65-V to 5.5-V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

### 8.4 Device Functional Modes

Table 1 lists the ON channel when one of the control inputs is selected.

**Table 1. Function Table**

| CONTROL INPUTS | ON CHANNEL |
|----------------|------------|
| L              | B1         |
| H              | B2         |

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LVC1G3157-Q1 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing and so on. For details on the applications, you can also view [SCYB014](#).

### 9.2 Typical Application

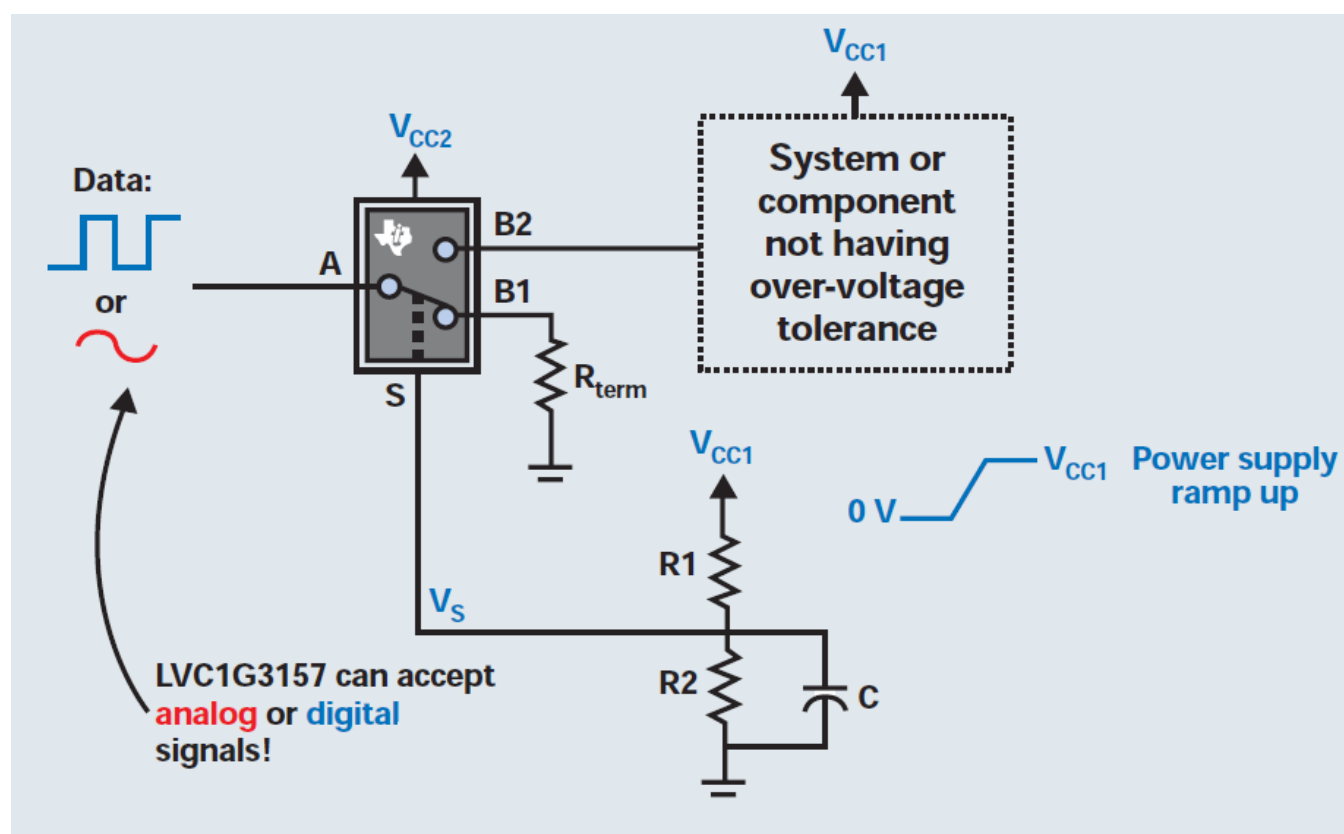


Figure 13. Typical Application Schematic

#### 9.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until VCC has ramped to a level in [Recommended Operating Conditions](#) before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2 and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use Equation 1 to calculate the time required from a transition from ground (0 V) to half the supply voltage (VCC1/2).

$$\text{Set} \left( \frac{R2}{R1 + R2} \times V_{CC1} > V_{IH} \right) \text{ of the select pin} \quad (1)$$

Choose Rs and C to achieve the desired delay.

When Vs goes high, the signal will be passed.

### 9.2.3 Application Curve

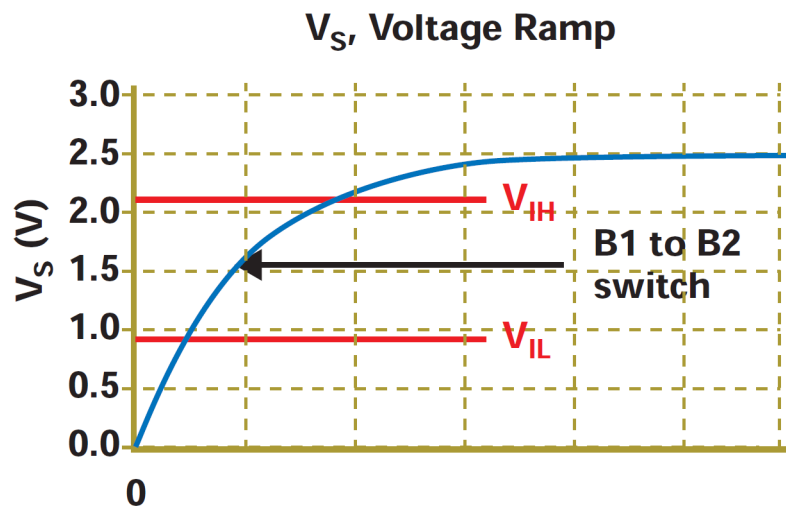


Figure 14. V<sub>S</sub> Voltage Ramp

## 10 Power Supply Recommendations

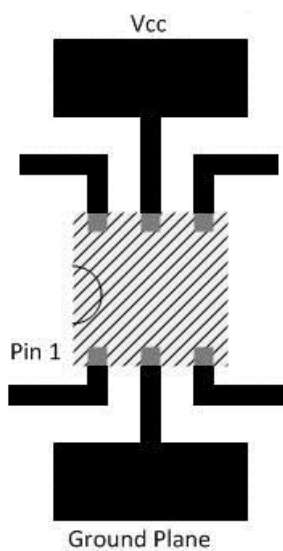
Most systems have a common 3.3-V or 5-V rail that can supply the  $V_{CC}$  pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

## 11 Layout

### 11.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either  $50\ \Omega$  or  $75\ \Omega$ , as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

### 11.2 Layout Example



**Figure 15. Recommended Layout Example**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- *SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches*, [SCYB014](#)

### 12.2 Trademarks

All trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 1P1G3157QDBVRQ1  | ACTIVE        | SOT-23       | DBV                | 6    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | CC5O                    | <a href="#">Samples</a> |
| 1P1G3157QDCKRQ1  | ACTIVE        | SC70         | DCK                | 6    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | C5O                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G3157-Q1 :**

- Catalog: [SN74LVC1G3157](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 1P1G3157QDBVRQ1 | SOT-23       | DBV             | 6    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| 1P1G3157QDCKRQ1 | SC70         | DCV             | 6    | 3000 | 179.0              | 8.4                | 2.2     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS

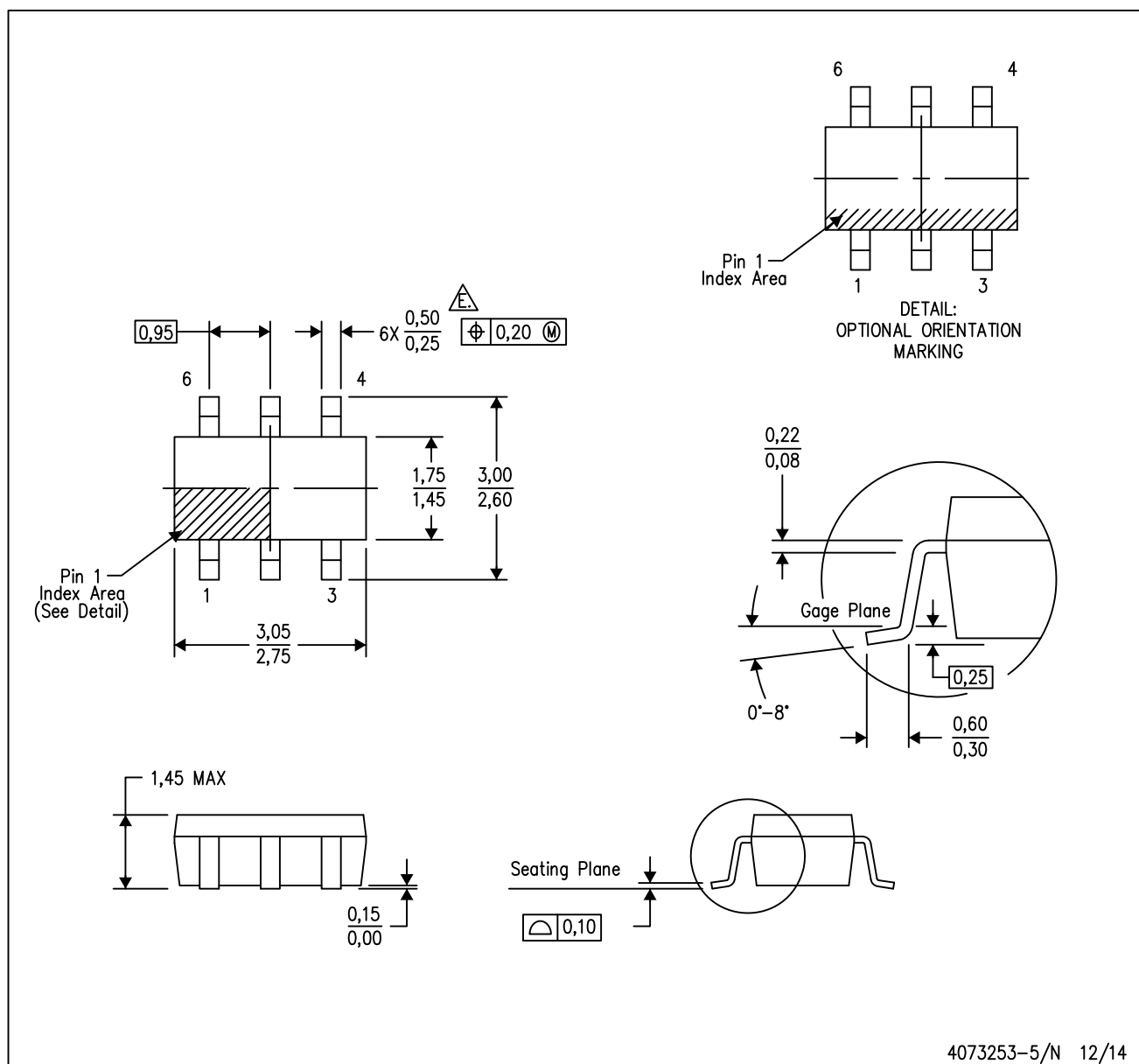


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 1P1G3157QDBVRQ1 | SOT-23       | DBV             | 6    | 3000 | 203.0       | 203.0      | 35.0        |
| 1P1G3157QDCKRQ1 | SC70         | DCK             | 6    | 3000 | 203.0       | 203.0      | 35.0        |

DBV (R-PDSO-G6)

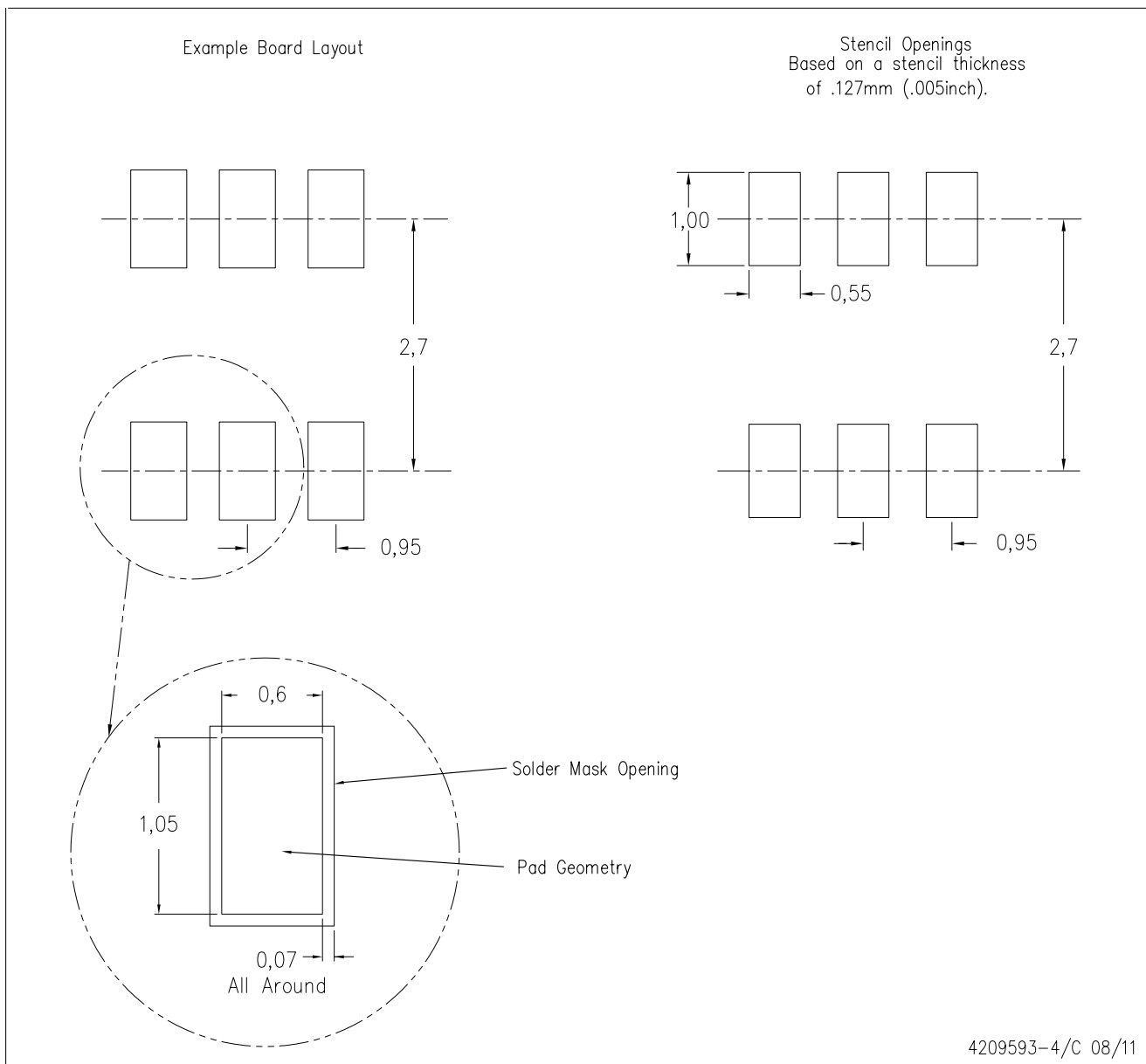
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

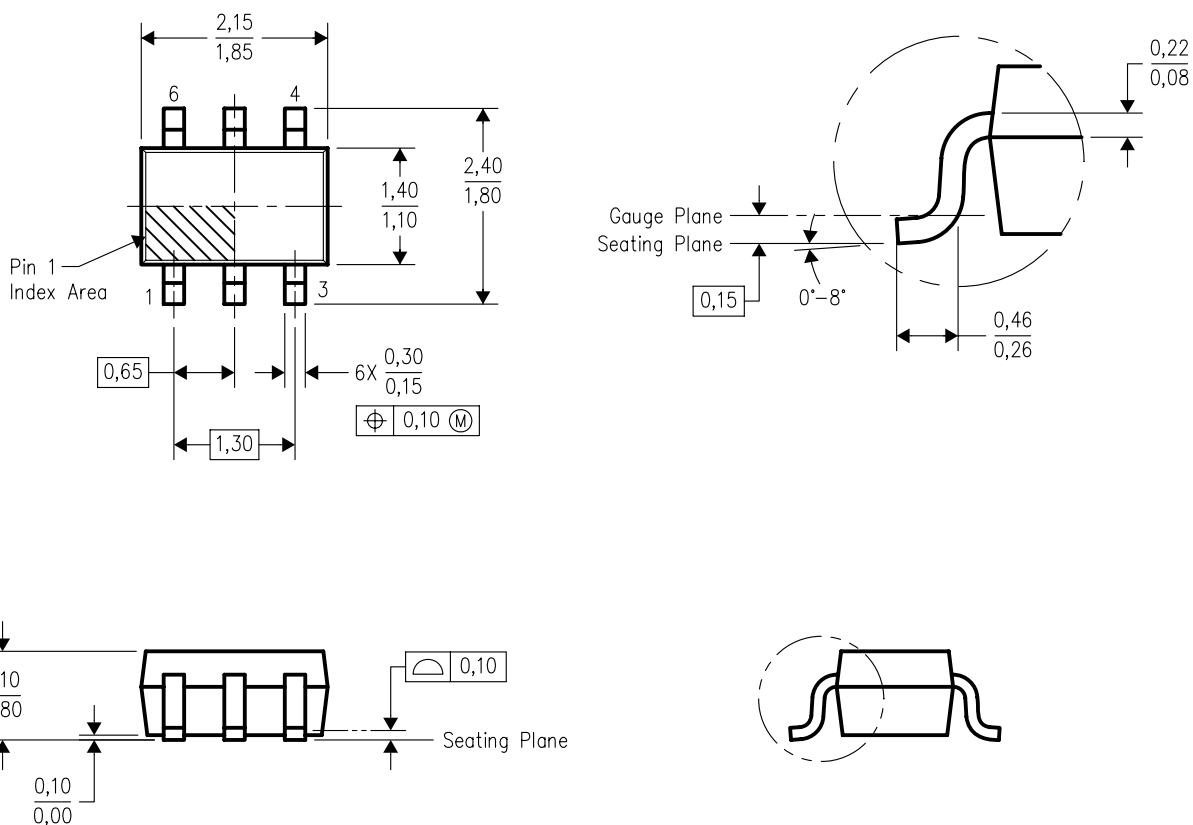
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE

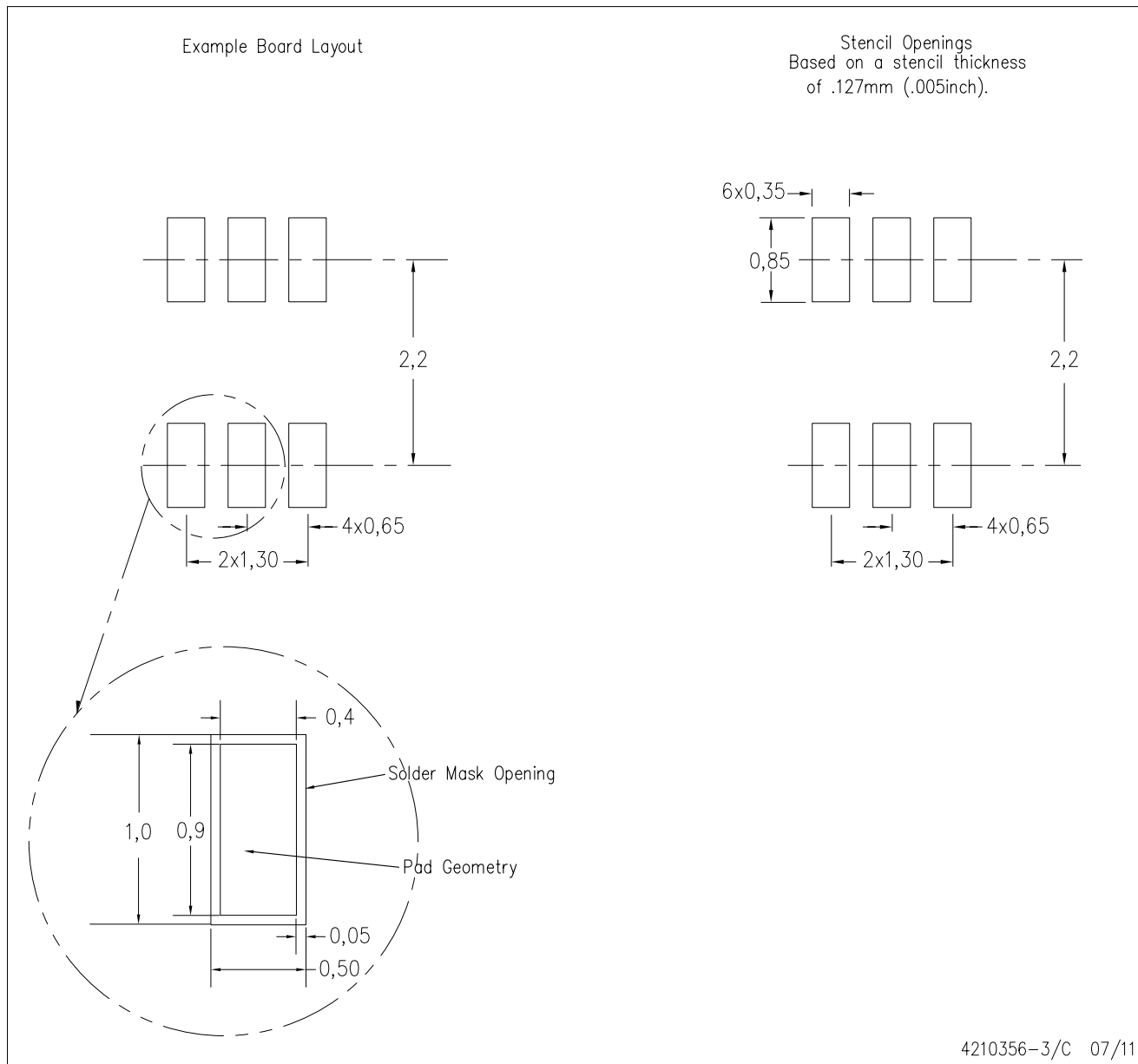


4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.