TLE7259G

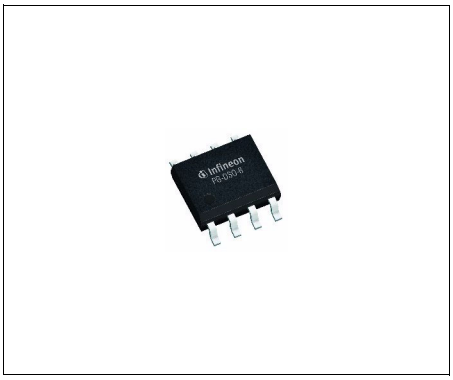
LIN Transceiver

Automotive Power

Never stop thinking

AEC Qualified

1 Overview



P-DSO-8

Features

- Transmission rate up to 20 kBaud
- Compliant to LIN specification 1.2, 1.3, 2.0 and 2.1
- Support of K-line function (ISO 9141)
- Very high ESD Robustness
- Very low Electromagnetic Emission (EME)
- Very High Electromagnetic Immunity (EMI)
- Very low current consumption in sleep mode
- Very low leakage current on the BUS output
- Control output for voltage regulator
- Wake up source recognition (local/remote)
- For 3.3 V and 5 V micro controller I/O
- Suitable for 12V and 24V board-net
- Bus short to V_{BAT} protection
- Bus short to GND handling
- Over temperature protection
- AEC Qualified

Description

The TLE7259G is a transceiver for the Local Interconnect Network (LIN) with integrated wake-up and protection features. It is designed for in-vehicle networks using data transmission rates from 2.4 kBaud to 20 kBaud. The TLE7259G functions as a bus driver between the protocol controller and the physical bus inside the LIN network. Compliant to all LIN standards and with a wide operational supply range the TLE7259G can be used in all automotive applications.

Different operation modes and the INH output allow the TLE7259G to control external components, like voltage regulators. In Sleep-mode the TLE7259G draws less than 8 µA of quiescent while still being able to wake up off of LIN bus traffic and a local wake-up input. The very low leakage current on the BUS pin makes the TLE7259G especially suitable for “Mixed Power Supply“ applications and supports the low quiescent current requirements of the LIN network.

Based on the Infineon Smart Power Technology SPT®, the TLE7259G provides excellent ESD Robustness together with a very high electromagnetic immunity (EMI). The TLE7259G reaches a very low level of electromagnetic emission (EME) within a broad frequency range and independent form the battery voltage.

The Infineon Smart Power Technology SPT® allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit. The TLE7259G and the Infineon SPT® technology are AEC qualified and tailored to withstand the harsh condition of the Automotive Environment.

Type	Package	Marking
TLE7259G	P-DSO-8	7259G

2 Block Diagram

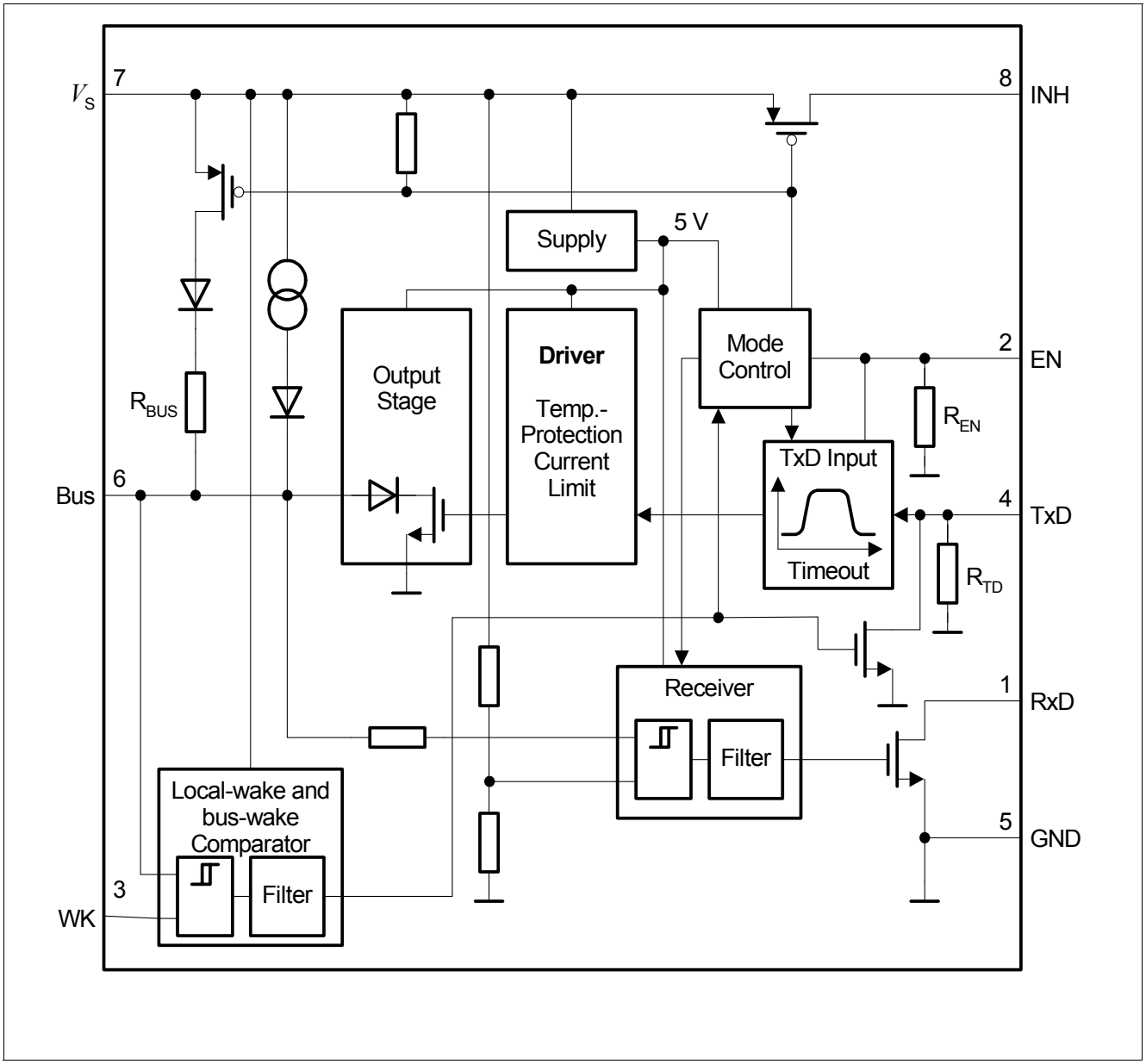


Figure 1 Functional Block Diagram

3 Pin Configuration

3.1 Pin Assignment

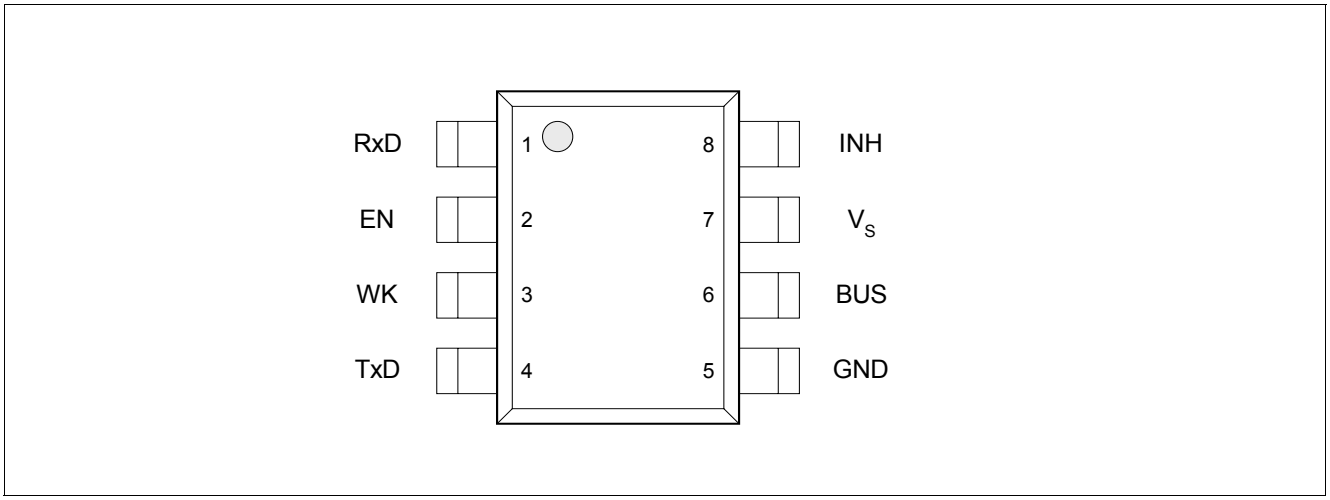


Figure 2 **Pin Configuration** (top view)

3.2 Pin Definitions and Functions

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	RxD	**Receive data output;** External Pull Up necessary LOW in dominant state, active LOW after a wake-up event at Bus or WK pin
2	EN	**Enable input;** integrated pull-down, device in normal operation mode when HIGH
3	WK	**Wake input;** active LOW, negative edge triggered, internal pull-up
4	TxD	**Transmit data input;** integrated pull-down, LOW in dominant state; active LOW after wake-up via WK pin
5	GND	**Ground**
6	Bus	**Bus output/input;** LIN bus line input/output LOW in dominant state Internal pull-up
7	V_S	**Battery supply input**
8	INH	**Inhibit output;** battery supply related output HIGH (V_S) in Normal and Stand-By operation mode can be used to control an external voltage regulator can be used to control external bus termination resistor when the device will be used as Master node

4 Functional Description

The LIN Bus is a single wire, bi-directional bus, used for in-vehicle networks. The LIN Transceiver TLE7259G is the interface between the micro controller and the physical LIN Bus (see **Figure 11** and **Figure 12**). The logical values of the micro controller are driven to the LIN bus via the TxD input of the TLE7259G. The transmit data stream on the TxD input is converted to a LIN bus signal with optimized slew rate to minimize the EME level on the LIN bus. The RxD output reads back the information from the LIN bus to the micro controller, regardless of the logical value of the TxD input. The receiver has an integrated filter network to suppress noise on the LIN Bus and to increase the EMI level of the transceiver. Two logical states are possible on the LIN bus according to the LIN Specification 2.1. The dominate state (voltage near ground) on the LIN bus represents a “logic 0“ on the TxD input of the TLE7259G; the recessive state (voltage near supply voltage V_S) represents a “logic 1” on the TxD input (see timing diagram **Figure 9**).

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE7259G for master node applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply V_S or the INH pin of the TLE7259G (see **Figure 11** and **Figure 12**).

4.1 Operating Modes

The TLE7259G has 3 different operation modes. After a power-up event the TLE7259G starts from the Stand-By mode. By setting the EN pin to “logic 1“ the micro controller can change the mode into Normal-Operation mode.

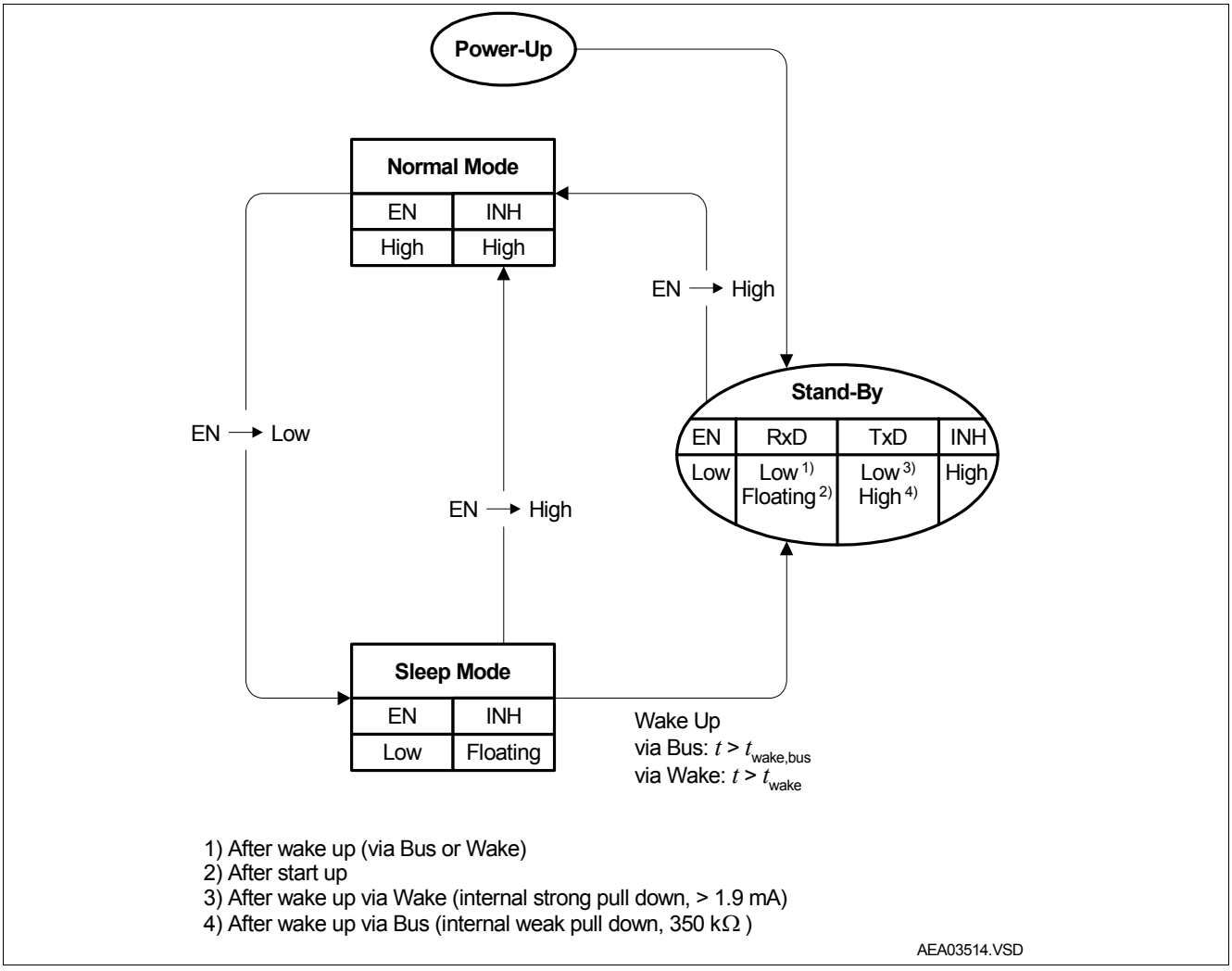


Figure 3 Operation Mode State Diagram

Table 2 Operating modes

Mode	EN	INH	TxD	RxD	LIN Bus Termination	Comments
Sleep	Low	Floating	Low	High[1)]	High Impedance	No wake-up request detected
Stand-By	Low	High	Low[2)] High[3)]	Low High [1)]	30 kΩ (typical)	RxD “Low” after local or bus wake-up RxD “High“ after power-up TxD strong pull down after local wake-up (WK pin)[2)] TxD weak pull down after bus wake-up or power-up[3)]
Normal	High	High	Low High	Low High	30 kΩ (typical)	RxD reflects the signal on the LIN bus TxD driven by the micro controller

1) Pull-up resistor to micro controller power supply (V_{IO}) required (see **Figure 11** and **Figure 12**).

2) TxD indicates logical “Low“ in case the micro controller output is set to “High“ and the micro controller output current is limited to less than 1.9 mA.

3) TxD indicates logical “High“ in case the micro controller output is set to “High“.

4.2 Normal Operation Mode

The TLE7259G enters the normal mode after the micro controller sets EN = high (see **Figure 3**). In Normal operation mode the LIN bus receiver and the LIN bus transmitter are active. Data from the micro controller is transmitted to the LIN bus via the TxD pin, the receiver detects the data stream on the LIN bus and outputs it to the RxD pin.

4.3 Stand-By Mode

The Stand-By mode is entered automatically after:

- A power-up event on the supply V_S.
- A wake-up event on the LIN bus.
- A local wake-up event on the pin WK.
- A power on reset caused by power supply V_S dropping below $V_{S,UV,PON}$ ($V_S < V_{S,UV,PON}$).

In Stand-By mode no communication on the LIN Bus is possible. The output stage is disabled and the LIN Bus termination remains activated. The RxD and TxD pins are indicating the wake-up source. The RxD pin remains “Low“ after a local and bus wake-up event. A power-up event is indicated by a logical “High“ on RxD pin. The signal on the TxD pin indicates the wake-up source, a weak pull-down signals a bus wake-up event and a strong pull-down signals a local wake-up event caused by the WK pin (see **Table 2**). In order to detect a wake-up event via the TxD pin, the external micro controller needs outputs needs to provide a logical “high” signal. The wake-up flags indicating the wake-up source on the pins TxD and RxD are reset by changing the operation mode to Normal operation.

The signal on the EN pin remains “Low“ due to an internal pull-down resistor. Setting the EN pin to “High“, by the micro controller the device returns to Normal operation mode. Entering the Stand-By mode switches the INH output to V_S. Depending on the operation mode of the TLE7259G external circuitry, like a voltage regulator, can be controlled by the INH output.

4.4 Sleep Mode

In order to reduce the current consumption the TLE7259G offers a Sleep mode. In Sleep mode the quiescent current on V_S and the leakage current on the pin Bus, are cut back to a minimum.

Switching the TLE7259G from Normal operation mode to Sleep mode, the EN pin needs to be set to “Low”. A logical “High” on the EN pin sets the device direct back to Normal operation mode (see **Figure 3**).

While the TLE7259G is in Sleep mode the following functions are available:

- The output stage is disabled and the internal bus termination is switched off (High Impedance on the Bus pin). An internal current source on the Bus pin ensures that the level on the Bus pin remains dominate and protects the LIN network against accidental bus wake-up events.
- The receiver is turned off
- RxD and TxD pins are disabled. The logical state on the TxD pin is low, due to the internal pull-down resistor. The RxD pin is “High” driven by the external pull-up resistor
- The INH output is switched off and floating.
- The BUS wake-up comparator is active and turns the TLE7259G to Stand-By mode in case of a bus wake-up.
- The WK pin is active and turns the TLE7259G to Stand-By mode in case of a local wake-up.
- The EN pin remains active, switching EN pin to “High“ changes the operation mode to Normal operation.

4.5 Wake-up Events

There are 3 different ways to wake-up the TLE7259G from Sleep mode.

- Bus or also called remote wake-up via a dominate signal on the LIN bus.
- Local wake-up via a minimum dominant time (t_{WK}) on the WK pin.
- Mode change from Sleep mode to Normal operation mode, by setting EN pin to logical “High”.

4.6 Bus Wake-up

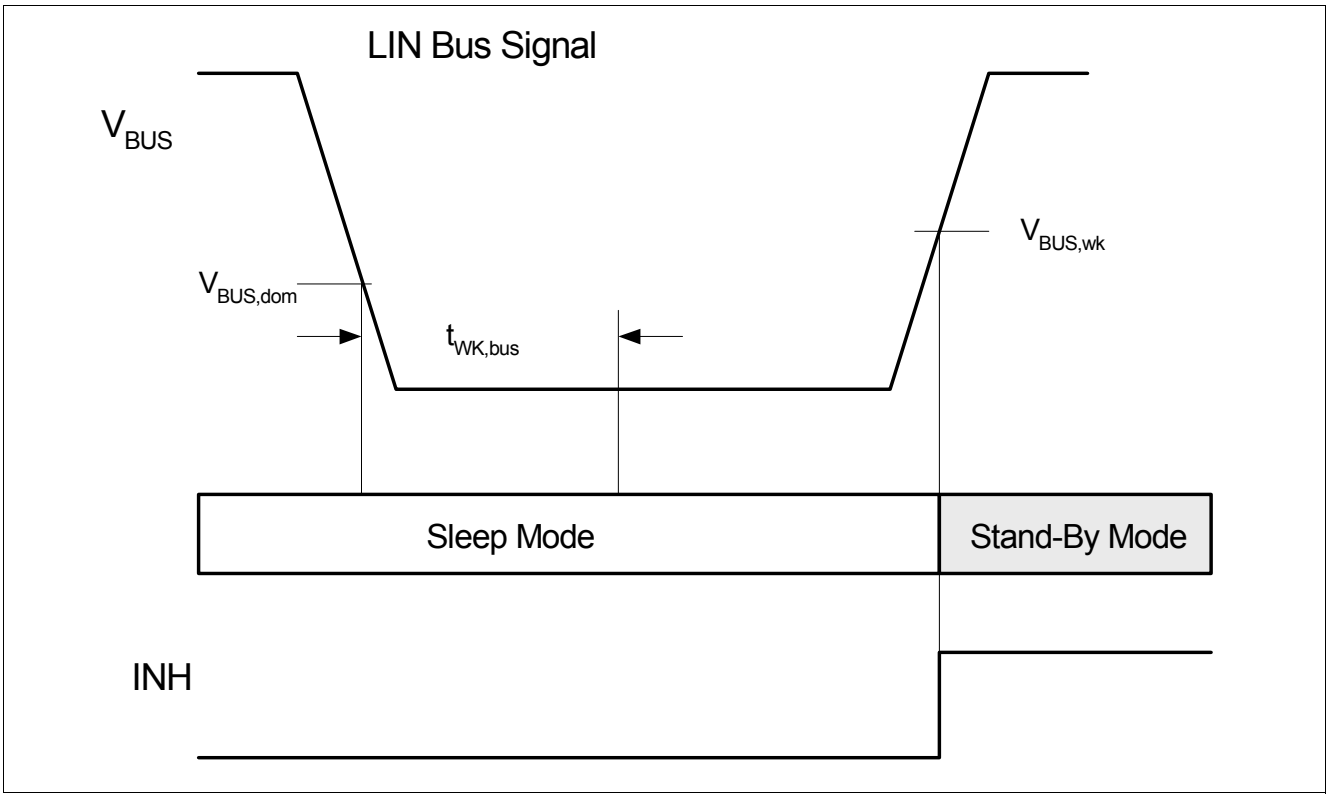


Figure 4 Bus wake-up behavior

The bus wake-up, often called remote wake-up, changes the operation mode from Sleep mode to Stand-By mode. A falling edge on the LIN bus, followed by a dominate bus signal t > $t_{WK,bus}$ results in a bus wake-up. The mode change to Stand-By mode becomes active with the following rising edge on the LIN bus. The TLE7259G remains in Sleep mode until it detects a change from dominate to recessive on the LIN bus (see **Figure 4**).

In Stand-By mode the TxD pin indicates the source of the wake-up event. A weak pull-down on the pin TxD indicates a bus wake-up event (see **Figure 3**). The RxD pin signals if a wake-up event occurred or the power-up event. A logical “Low” on the RxD pin reports a local or bus wake-up event, a logical “High“ signal on RxD indicates a power-up event.

4.7 Local Wake-up

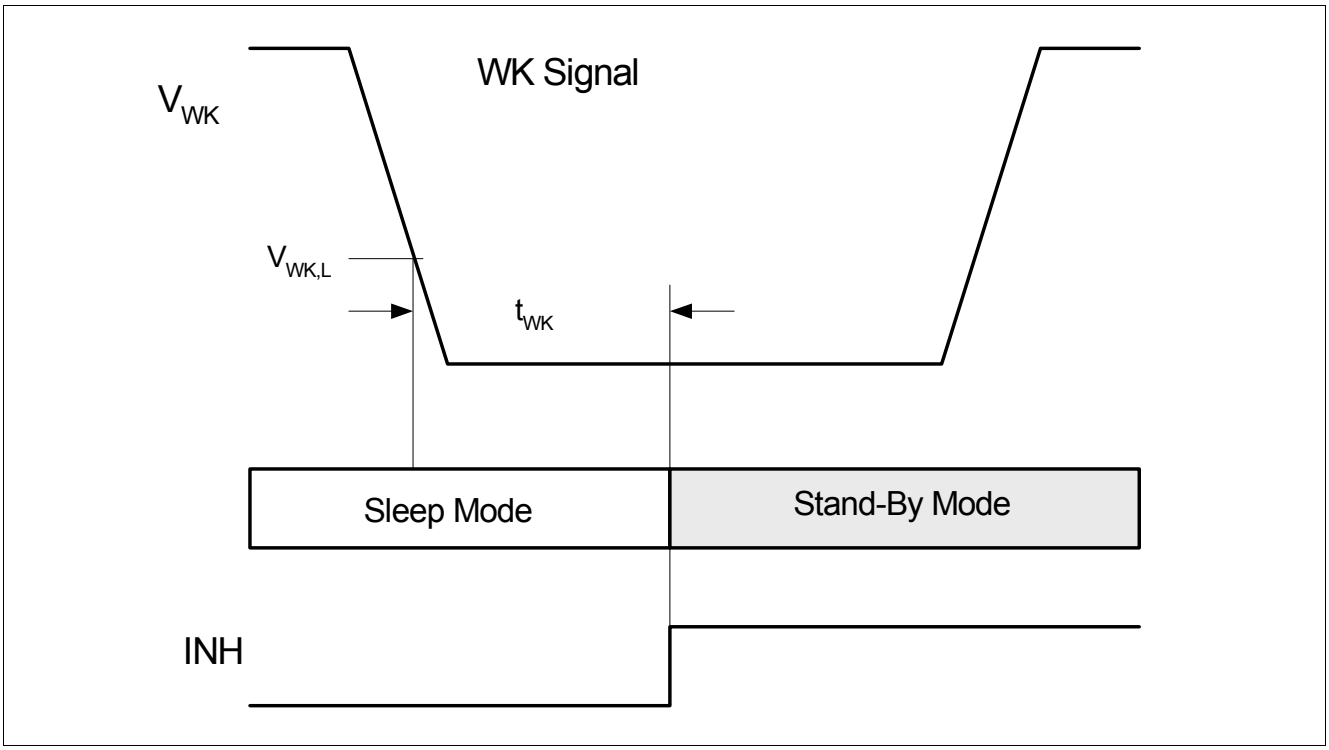


Figure 5 Local wake-up behavior

Beside the remote wake-up, a wake-up of the TLE7259G via the WK pin is possible. This wake-up event is called local wake up. A falling edge on the WK pin followed by a logical “Low“ for t > t_{WK} results in a local wake up (see **Figure 5**) and change the operation mode to Stand-By Mode.

In Stand-By mode the TxD pin indicates the source of the wake-up event. A strong pull down on the pin TxD indicates a local wake-up event via the pin WK (see **Figure 3**). The RxD pin signals if a wake-up event occurred or the power-up event. A logical “Low” on the RxD pin reports a local or bus wake-up event, a logical “High“ signal on RxD indicates a power-up event.

4.8 Mode Transition via EN pin

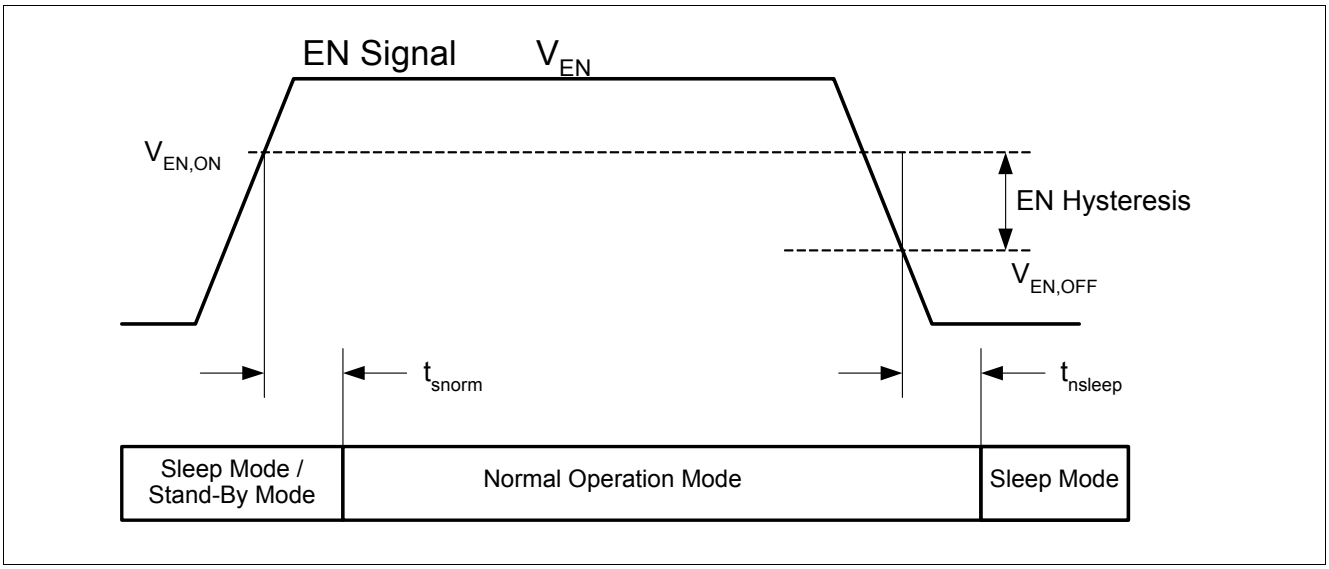


Figure 6 Mode transition via EN pin

It is also possible to change from Sleep mode to Normal operation mode by setting the EN pin to logical “Low“.This feature is useful if the external micro controller is continuously powered and not connected to the INH pin. The EN pin has an integrate pull-down resistor to ensure the device remains in Sleep or Stand-By mode even if the voltage on the EN pin is floating. The EN pin has an integrated hysteresis (see **Figure 6**).

A transition from logical “High“ to logical “Low“ on the EN pin changes the operation mode from Normal operation mode to Sleep mode. If the TLE7259G is already in Sleep mode, changing the EN from “Low“ to “High” results into a mode change from Sleep mode to Normal operation mode. If the device is in Stand-By mode a change from “Low“ to “High” on the EN pin changes the mode to Normal operation mode (see **Figure 3**).

4.9 Power-On Reset

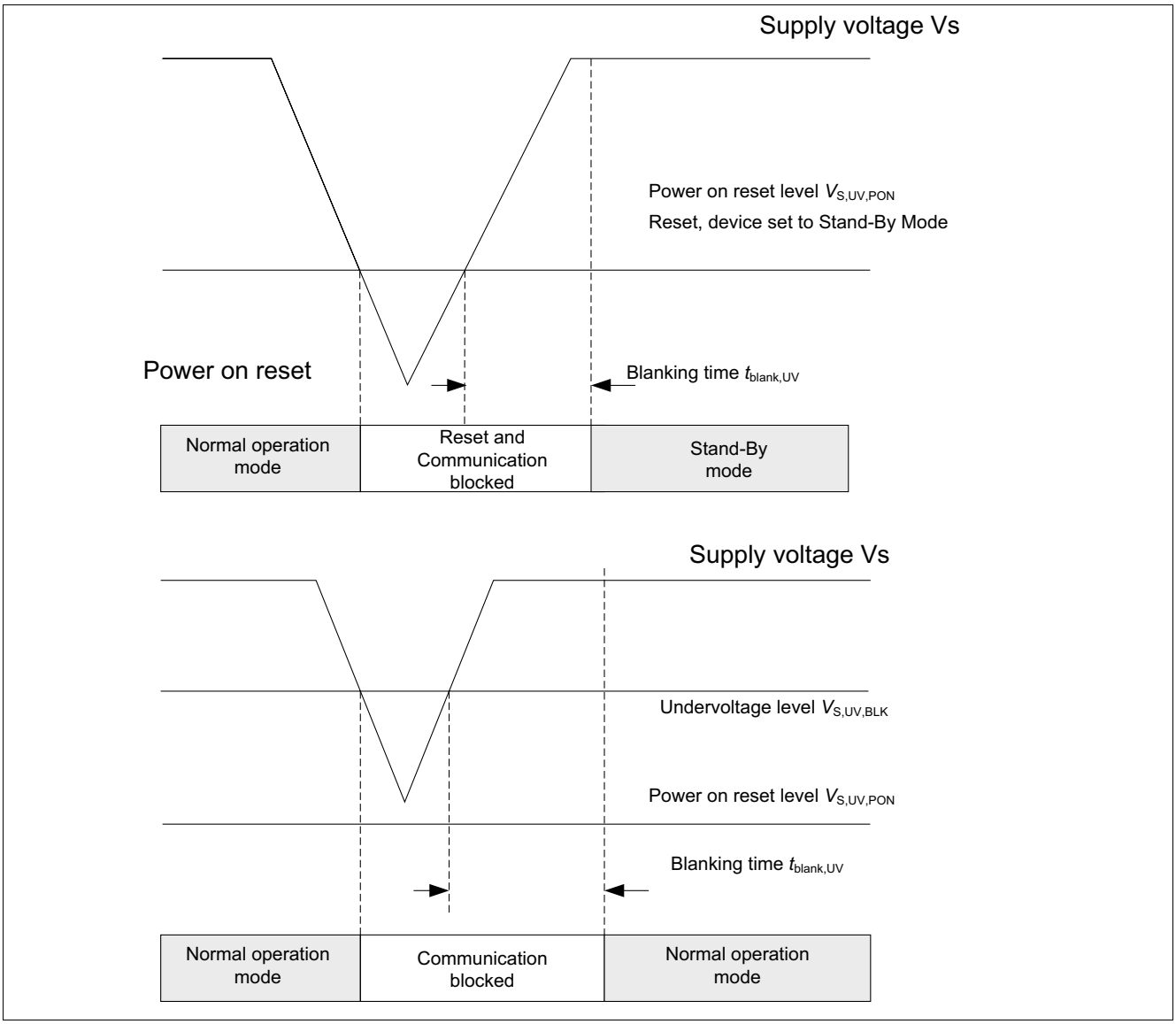


Figure 7 Power-on reset and Undervoltage situation

A drooping power supply V_S on a local ECU can effect the communication of the whole LIN network. To avoid any blocking of the LIN network by a local ECU the TLE7259G has an integrated power-on reset and undervoltage detection. In case the supply voltage is dropping below the power on reset level $V_S < V_{S,UV,PON}$, the TLE7259G changes the operation mode to Stand-By mode. In Stand-By mode the output stage of the TLE7259G is disabled and no communication to the LIN bus is possible. The internal bus termination remains active as well as the INH pin (see **Figure 7**).

In Stand-By mode the RxD pin signals the low power supply condition with a logical “High“ Signal. A logical “High“ on the EN pin changes the operation mode back to Normal operation mode.

In case the supply voltage V_S is dropping below the specified operation range (see **Table 5**), the TLE7259G disables the output and receiver stages. The feature secures the communication on the LIN bus, even if the local ECU power supply of the TLE7259G drops below the specified operating range. If the power supply reaches a higher level as the undervoltage level $V_S > V_{S,UV,PON}$ the TLE7259G continues with normal operation. A mode change only apply if the power supply V_S drops below the power on reset level ($V_S < V_{S,UV,PON}$).

4.10 TxD time out function

If the TxD signal is dominant for a time $t > t_{timeout}$ the TxD time-out function deactivates the transmission of the LIN signal to the bus. This is realized to prevent the bus from being permanently blocked by a permanent “Low” signal on the TxD pin due to an error.

The transmission is released again, after a rising edge at TxD has been detected.

4.11 Over temperature protection

The TLE7259G has an integrated over temperature sensor, to protect the device against thermal overstress. In case of an over temperature event, the temperature sensor will disable the output stage. An over temperature event will not cause any mode change nor will it be signaled by either the RxD pin or the TxD pin. When the junction temperature falls below the thermal shut down level $T_J < T_{jSD}$, the output stage is re-enabled and data communication can start again. A10°C hysteresis avoids toggling during the temperature shut down.

4.12 3.3 V and 5 V Logic Capability

The TLE7259G can be used for 3.3 V and 5 V micro controllers. The inputs (TxD, EN) take the reference voltage from the connected micro controller pins. The RxD output must have an external pull-up resistor to the micro controller supply, to define the output voltage level.

4.13 BUS Short to GND Feature

The TLE7259G has a feature implemented to protect the battery from running out of charge in the case the LIN bus is shorted to GND.

In this failure case a normal master termination, a 1 kΩ resistor and a diode connected between the Bus pin and the power supply V_S, would cause a constant current between V_S and GND, even in sleep mode. The resulting resistance between V_S and GND of this LIN bus short to GND is lower than 1 kΩ. To avoid this current during a generator off state, like in a parked car, the TLE7259G has a Bus Short to GND feature implemented. This feature is only applicable, if the master termination is connected to the INH pin, instead of the V_S power supply (see **Figure 11** and **Figure 12**). In Sleep mode the INH pin is switched of and no currently can flow between V_S and GND. The internal 30 kΩ bus termination is also switched off (see **Figure 1** and **Table 2**) to minimize the discharge current.

4.14 LIN Specifications 1.2, 1.3, 2.0 and 2.1

The device fulfills the Physical Layer Specification of LIN 1.2, 1.3, 2.0 and 2.1.

The differences between LIN specification 1.2 and 1.3 is mainly the physical layer specification. The reason was to improve the compatibility between the nodes.

The LIN specification 2.0 is a super set of the 1.3 version. The 2.0 version offers new features. However, it is possible to use the LIN 1.3 slave node in a 2.0 node cluster, as long as the new features are not used. Vice versa it is possible to use a LIN 2.0 node in the 1.3 cluster without using the new features.

In terms of the physical layer the LIN 2.1 Specification doesn’t include any changes and is fully compliant to the LIN Specification 2.0.

LIN 2.1 is the latest version of the LIN specification, released in December 2006.

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings Voltages, Currents and Temperatures[1)]

T_j = -40 °C to 150 °C; all voltages with respect to ground; positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
Voltages						
5.1.1	Battery supply voltage	V_S	-0.3	40	V	LIN Spec 2.1 Param. 10
5.1.2	Bus input voltage versus GND versus V_S	 $V_{BUS,G}$ $V_{BUS,Vs}$	 -40 -40	 40 40	 V V	t < 1 s
5.1.3	Wake input versus GND Wake input versus V_S	$V_{WK,G}$ $V_{WK,Vs}$	-40 -40	40 40	V V	–
5.1.4	Logic voltages at EN, TxD, RxD	V_{logic}	-0.3	5.5	V	–
5.1.5	Inhibit Voltage versus GND Versus V_S	 $V_{INH,G}$ $V_{INH, Vs}$	 -0.3 -40	 40 0,3	 V V	
Currents						
5.1.6	Output current at INH	I_{INH}	-150	80	mA	2)
Temperatures						
5.1.7	Junction temperature	T_j	-40	150	°C	–
5.1.8	Storage temperature	T_S	-55	150	°C	–

1) Not subject to production test specified by design

2) Output current is internally limited to -150 mA

Table 4 Absolute Maximum Ratings ESD Resistivity[1)]

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
5.1.9	Electrostatic discharge voltage at V_S,Bus, Wk versus GND	V_{ESD}	-6	6	kV	Human Body Model[2)] (100 pF via 1.5 kΩ)
5.1.10	Electrostatic discharge voltage execpt V_S versus Bus	V_{ESD}	-2	2	kV	Human Body Model[2)] (100 pF via 1.5 kΩ)
5.1.11	Electrostatic discharge voltage at Bus versus V_S	V_{ESD}	-1	1	kV	Human Body Model (100 pF via 1.5 kΩ)[2)]

1) Not subject to production test specified by design

2) ESD susceptibility HBM according to EIA / JESD 22-A 114B

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

5.2 Functional Range

Table 5 Operating Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
5.2.1	Supply Voltage range V_S	V_S	6	40	V	LIN Spec 2.1 Param. 10
Thermal parameters						
5.2.2	Junction temperature	T_j	-40	150	°C	1)

1) Not subject to production test, specified by design

5.3 Thermal Resistance

Table 6 Thermal Resistance[1)]

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
5.3.1	Junction to Ambient	R_{thJA}	–	185	K/W	2)

1) Not subject to production test, specified by design

2) JESD 51-2, 51-3, FR4 76,2 mm x 114,3 mm x 1,5 mm, 70µm, Cu, minimal footprint, T_A = 27°C

5.4 Electrical Characteristics

Table 7 Electrical Characteristics

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Current Consumption							
5.4.1	Current consumption at V_S in recessive state	$I_{S,rec}$	0.1	0.8	1.5	mA	recessive state, without R_L; $V_{TxD} = V_{CC}$
5.4.2	Current consumption at V_S in dominant state	$I_{S,dom}$	0.1	1.3	2.5	mA	dominant state, without R_L; V_{TxD} = 0 V
5.4.3	Current consumption in sleep mode	$I_{S,sleep}$	1	–	14	µA	sleep mode, $V_{WK} = V_S$; $V_{BUS} = V_S$
5.4.4	Current consumption in sleep mode	$I_{S,sleep,typ}$	1	–	8	µA	sleep mode, T_j=85°C $V_{WK} = V_S$; $V_{BUS} = V_S$
5.4.5	Current consumption in stand-by mode	$I_{S,stby}$	0.1	–	1.5	mA	stand-by mode, $V_{WK} = V_S$; $V_{BUS} = V_S$
5.4.6	Current consumption in sleep mode, bus shorted to ground	$I_{S,sleep,short}$	5	10	60	µA	sleep mode, $V_{WK} = V_S$; $V_{BUS} = 0V$

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Reset Levels							
5.4.7	Blocking Undervoltage Detection at V_S	$V_{S,UV,BLK}$	5	–	6		Communication blocked (see **Figure 7**)
5.4.8	Power on reset	$V_{S,UV,PON}$	–	2.4	4	V	Device reset to Stand-by-Mode (see **Figure 7**)
5.4.9	Blanking time power on reset detection	$t_{blank,UV}$	–	10	–	µs	1)
Thermal Shutdown (Junction Temperature)							
5.4.10	Thermal shutdown temp.	T_{jSD}	150	170	190	°C	1)
5.4.11	Thermal shutdown temp.	ΔT	–	10	–	K	1)
Receiver Output RxD							
5.4.12	HIGH level leakage current	$I_{RD,H}$	-5	0	5	µA	V_{RxD} = 5 V; V_{BUS} = V_S
5.4.13	LOW level output current	$I_{RD,L}$	1.3	–	10	mA	V_{RxD} = 0.9 V; V_{BUS} = 0 V
Transmission Input TxD							
5.4.14	HIGH level input voltage threshold	$V_{TD,H}$	–	–	0.7 × V_{EN}	V	recessive state 3.0 V < V_{EN} < 5.5 V
5.4.15	TxD input hysteresis	$V_{TD,hys}$	–	0.12 × V_{EN}	–	mV	3.0 V < V_{EN} < 5.5 V
5.4.16	LOW level input voltage threshold	$V_{TD,L}$	0.3 × V_{EN}	–	–	V	dominant state 3.0 V < V_{EN} < 5.5 V
5.4.17	TxD pull-down resistance	R_{TD}	100	350	800	kΩ	V_{TxD} = 5 V
5.4.18	TxD low level leakage current Wake = V_S	I_{TD}	-1	–	10	µA	V_{EN} = 0 V; V_{TxD} = 0 V V_{BUS} = V_S
5.4.19	TxD dominant current Wake = 0 V; V_S = 12 V; standby mode	$I_{TD,L}$	1.5	3	6	mA	V_{TxD} = 0.9 V V_{BUS} = V_S
Enable Input EN							
5.4.20	HIGH level input voltage threshold	$V_{EN,on}$	0.95	–	2	V	normal mode see **Figure 6**
5.4.21	LOW level input voltage threshold	$V_{EN,off}$	0.8	–	1.85	V	low power mode see **Figure 6**
5.4.22	EN input hysteresis	$V_{EN,hys}$	150	300	450	mV	–
5.4.23	EN pull-down resistance	R_{EN}	15	30	60	kΩ	–
5.4.24	Enable inhibit high current	$I_{EN,\ hc}$	50	–	400	µA	V_{EN} = 5 V, 3 V

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Inhibit Output INH							
5.4.25	Inhibit R_{on} resistance	$R_{INH,on}$	22	36	50	Ω	I_{INH} = -15 mA
5.4.26	Maximum INH output current	I_{INH}	-150	–	-40	mA	V_{INH} = 0 V
5.4.27	Leakage current	$I_{INH,lk}$	-5.0	–	5.0	µA	sleep mode; V_{INH} = 0 V
Wake Input WK							
5.4.28	High level input voltage	$V_{WK,H}$	V_S - 1	–	V_S + 3	V	–
5.4.29	Low level input voltage	$V_{WK,L}$	-0.3	–	V_S -3.3 V	V	–
5.4.30	Pull-up current	$I_{WK,PU}$	-60	-30	-3	µA	–
5.4.31	High level leakage current	$I_{WK,L}$	-5	–	5	µA	V_S = 0 V; V_{WK} = 40 V
5.4.32	Dominant time for wake-up	t_{WK}	30	–	150	µs	–
Bus Receiver							
5.4.33	Receiver threshold voltage, recessive to dominant edge	$V_{th,rd}$	0.4 x V_S	0.48 × V_S	–	V	–
5.4.34	Receiver dominant state	V_{BUSdom}	0	–	0.4 x V_S	V	LIN Spec 2.1 Param. 17
5.4.35	Receiver threshold voltage, dominant to recessive edge	$V_{th,dr}$	–	0.52 × V_S	0.6 x V_S	V	$V_{BUS,rec}$ < V_{BUS} < 27 V
5.4.36	Receiver recessive state	V_{BUSrec}	0.6 x V_S	–	V_S	V	LIN Spec 2.1 Param. 18
5.4.37	Receiver center voltage	V_{BUS_CNT}	0.475× V_S	0.5 × V_S	0.525× V_S	V	LIN Spec 2.1 Param. 19
5.4.38	Receiver hysteresis	V_{HYS}	0.02 × V_S	0.04 × V_S	0.1 × V_S	V	LIN Spec 2.1 Param. 20 [2]
5.4.39	Wake-up threshold voltage	$V_{BUS,wk}$	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–
5.4.40	Dominant time for bus wake-up	$t_{WK,bus}$	30	–	150	µs	–

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Bus Transmitter							
5.4.41	Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level
5.4.42	Bus dominant output voltage maximum load	$V_{BUS,do}$	 0.6 0.8	 – – –	 1.2 0.2 x V_S 2.0	V	V_{TxD} = 0 V; R_L = 500 Ω; 6.0 V ≤ V_S ≤ 7.3 V 7.3 V < V_S ≤ 10 V 10 V < V_S ≤ 18 V
5.4.43	Bus dominant output voltage minimum load	$V_{BUS,do}$	 0.6 0.8	 – –	 1.2 2.0	V	V_{TxD} = 0 V; R_L = 1000 Ω; V_S = 7.3 V; V_S = 18 V;
5.4.44	Bus short circuit current	I_{BUS_LIM}	40	100	150	mA	V_{BUS} = 13.5 V; LIN Spec 2.1 Param. 12
5.4.45	Leakage current	$I_{BUS_NO_GND}$	-500	-70	0	µA	V_S = 0 V; V_{BUS} = -12V; LIN Spec 2.1 Param. 15
5.4.46	Leakage current	$I_{BUS_NO_BAT}$	–	5	8	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.1 Param. 16
5.4.47	Leakage current	$I_{BUS_PAS_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.1 Param. 13
5.4.48	Leakage current	$I_{BUS_PAS_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.1 Param. 14
5.4.49	Bus pull-up resistance	R_{SLAVE}	20	30	47	kΩ	Normal mode LIN Spec 2.1 Param. 26
5.4.50	LIN output current	I_{BUS}	-60	-30	-5	µA	Sleep mode V_S = 12V; EN = 0V

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Dynamic Transceiver Characteristics							
5.4.51	Slew rate falling edge	t_{fslope}	-3	–	-1	V/µs	[3] 60% > V_{bus} > 40%; 1 µs < (τ = $R_L \times C_{BUS}$) < 5 µs; V_S = 13.5 V; normal mode;
5.4.52	Slew rate rising edge	t_{rslope}	1	–	3	V/µs	[3] 40% < V_{bus} < 60%; 1 µs < (τ = $R_L \times C_{BUS}$) < 5 µs; V_S = 13.5 V; normal mode;
5.4.53	Slope symmetry	$t_{slopesym}$	-5	–	5	µs	t_{fslope} - t_{rslope}; V_S = 13.5 V;
5.4.54	Propagation delay TxD LOW to bus	$t_{d(L),T}$	0.1	1	4	µs	V_{EN} = 5 V;
5.4.55	Propagation delay TxD HIGH to bus	$t_{d(H),T}$	0.1	1	4	µs	V_{EN} = 5 V;
5.4.56	Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF; R_{RxD} = 2.4 kΩ;
5.4.57	Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF; R_{RxD} = 2.4 kΩ;
5.4.58	Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$;
5.4.59	Transmitter delay symmetry	$t_{sym,T}$	-2	–	2	µs	$t_{sym,T}$ = $t_{d(L),T}$ - $t_{d(H),T}$
5.4.60	Delay time for change sleep/stand by mode - normal mode	t_{snorm}	0.1	–	10	µs	–
5.4.61	Delay time for change normal mode - sleep mode	t_{nsleep}	0.1	–	10	µs	–
5.4.62	TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V
5.4.63	TxD dominant time out recovery time	t_{torec}	1	5	10	µs	[1]

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
5.4.64	Duty cycle D1 (for worst case at 20 kBit/s)	t_{duty1}	0.396	–	–		duty cycle 1 [3] TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) =0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$/2 t_{bit}; LIN Spec 2.1 Param. 27
5.4.65	Duty cycle D2 (for worst case at 20 kBit/s)	t_{duty2}	–	–	0.581		duty cycle 2 [3] TH_{Rec}(max) = 0.422 × V_S; TH_{Dom}(max) = 0.284 × V_S V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$/2 t_{bit}; LIN Spec 2.1 Param. 28

1) Not subject to production test, specified by design

2) V_{HYS} = V_{BUSrec} - V_{BUSdom}

3) Bus load concerning LIN Spec 2.1
Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
Load 3 = 10 nF / 500Ω = C_{BUS} / R_{BUS}

6 Diagrams

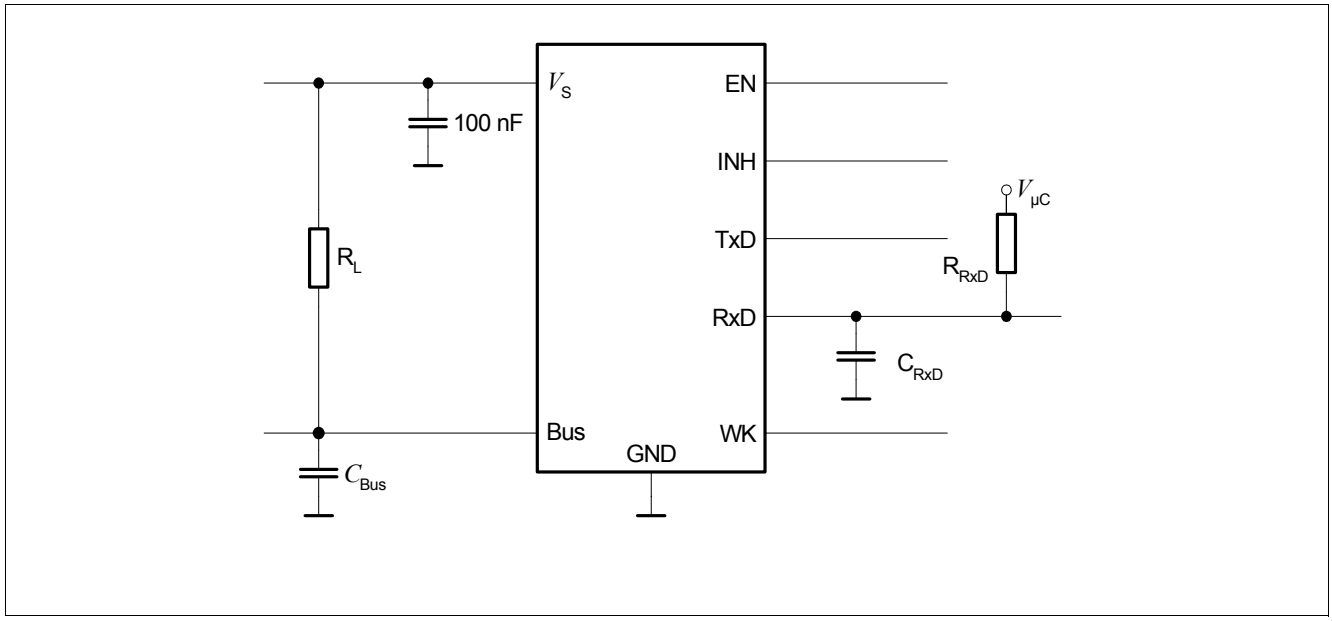


Figure 8 Test Circuits

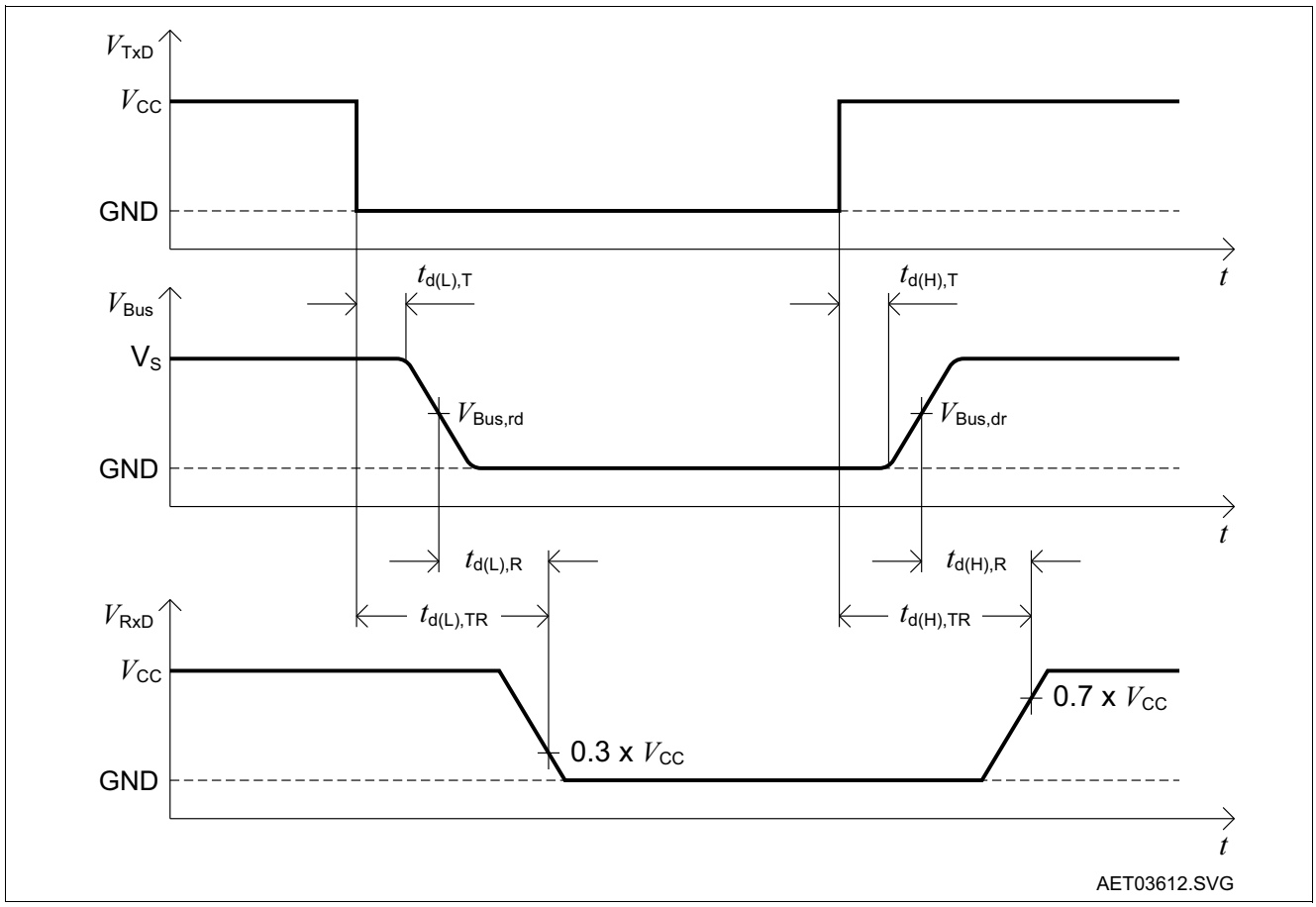


Figure 9 Timing Diagrams for Dynamic Characteristics according to LIN 1.3

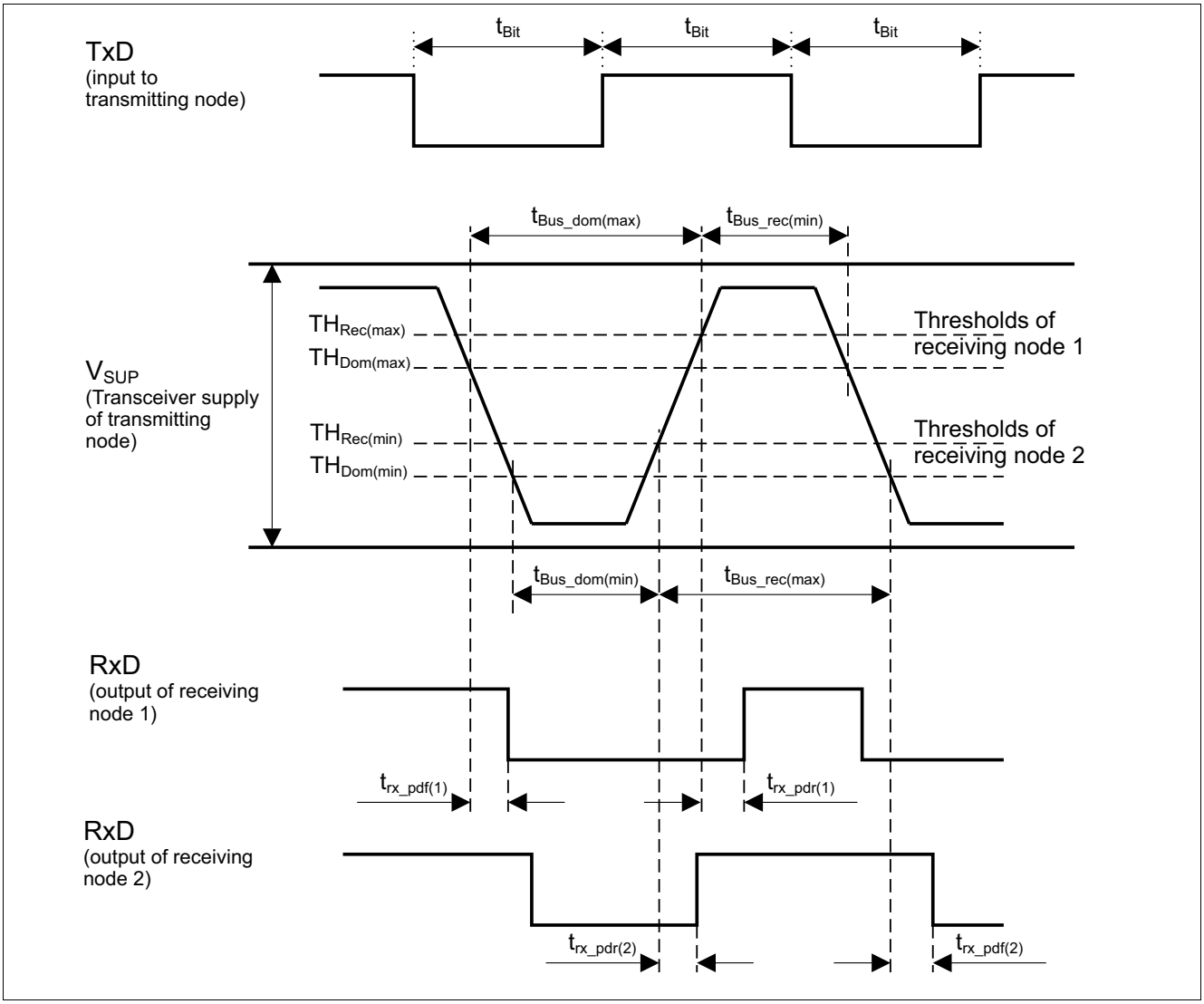


Figure 10 Timing Diagrams for Duty cycle measurements according to LIN 2.1

7 Application Information

7.1 ESD Robustness according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a seperate test report.

Table 8 ESD “Gun test”

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin V_S, Bus, Wk versus GND	≥ +8	kV	1)Positive pulse
Electrostatic discharge voltage at pin V_S, Bus, Wk versus GND	≤ -8	kV	1)Negative pulse

1) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3. (IEC 61000-4-2) -Tested by external testhouse (IBEE Zwickau, EMC Testreport Nr. 16-05-06).

7.2 Master Termination

To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is mandatory. It is recommended to place this resistor at the master node. To avoid reverse currents from the bus line into the battery supply line it is recommended to place a diode in series with the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF in the master node (see **Figure 11** and **Figure 12**, application circuit).

7.3 External Capacitors

A capacitor of 22 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

The 100 nF capacitors close to the V_S pins of the TLE7259G and the voltage regulator help to improve the EMC behavior of the system.

7.4 Application Example

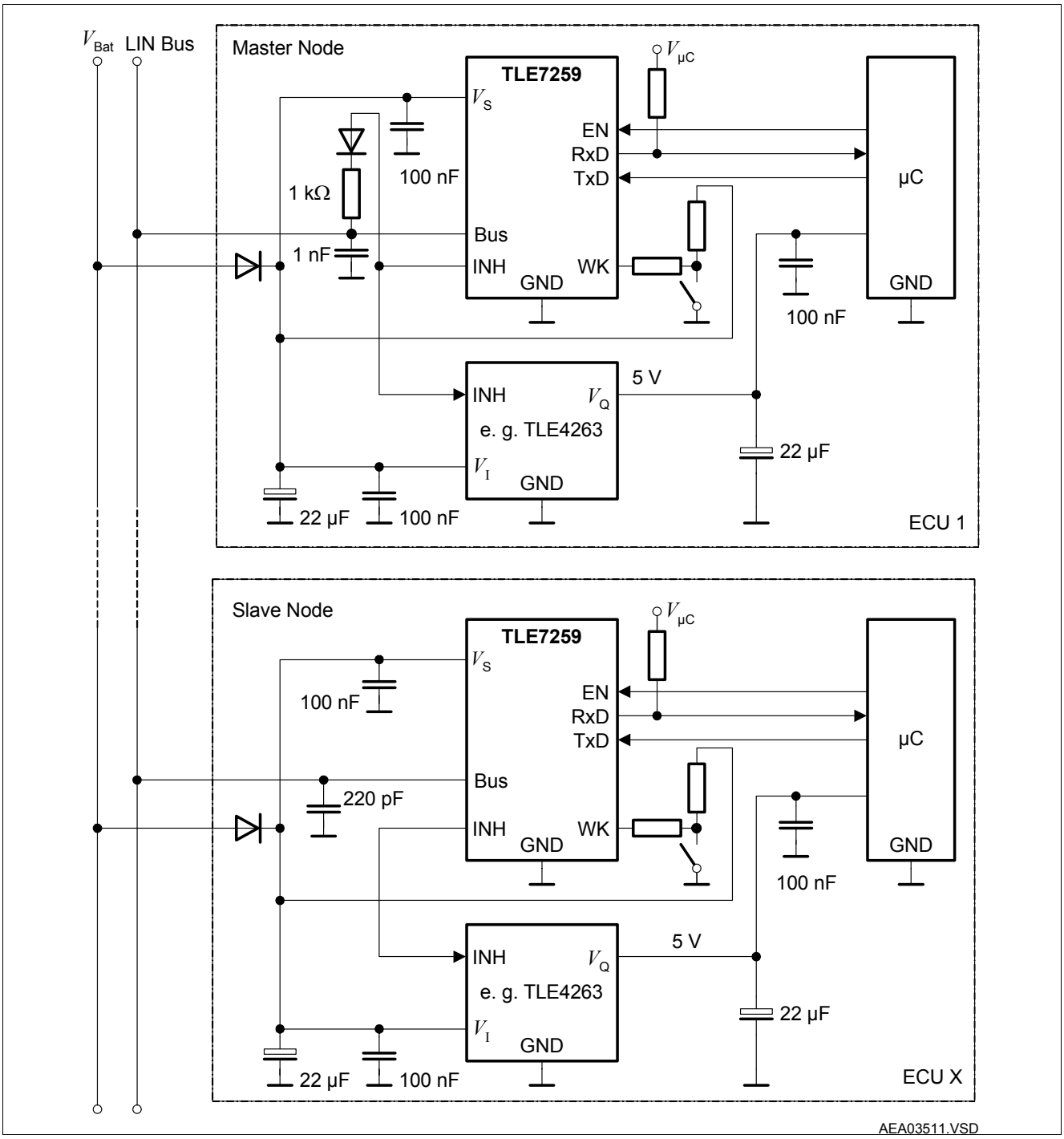


Figure 11 Application Circuit with Bus Short to GND Feature Applied

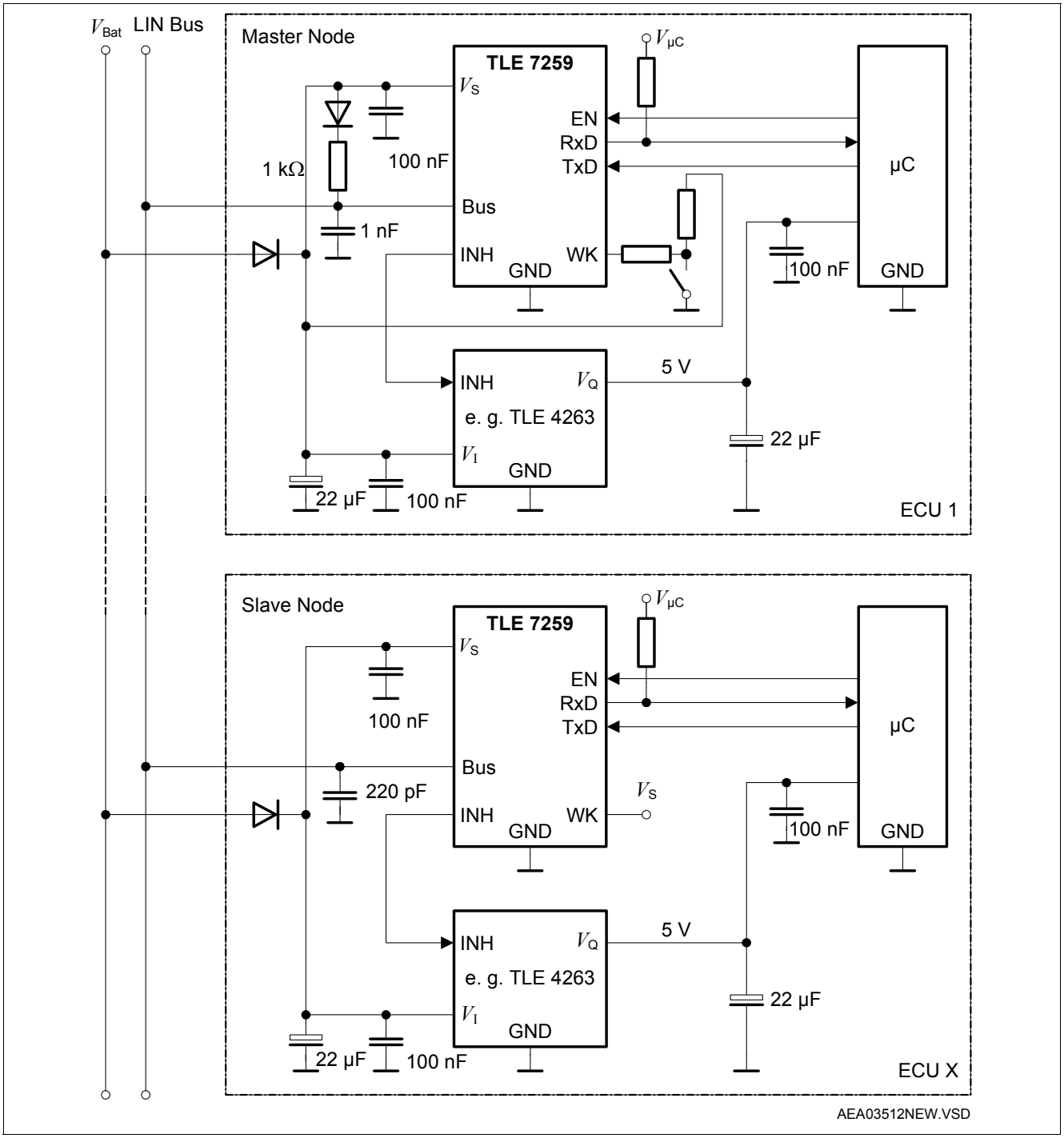
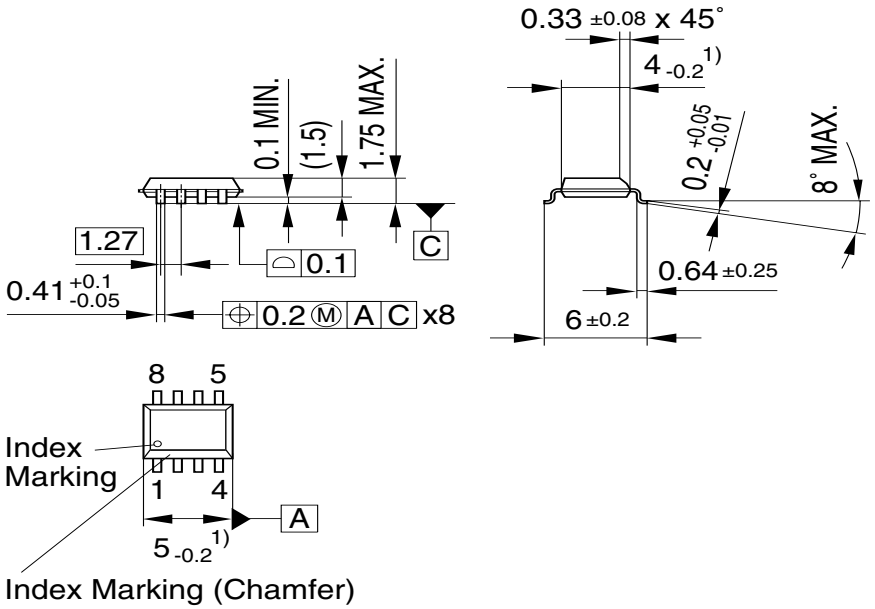


Figure 12 Application Circuit without Bus Short to GND Feature

8 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09032

Figure 13 **P-DSO-8** (Plastic Dual Small Outline)

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages

Dimensions in mm

9 Revision History

Version	Date	Changes
Rev 2.0	2006-07-19	Creation of Data sheet
Rev. 2.1	2007-04-30	Changes are described in a seperate Delta Sheet for TLE7259G Revision 1.0

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