

Rev B1, Page 1/14

FEATURES

- 1024/960/640/320 active photo pixels with 12.7 μm x 600 μm (2000 DPI)
- Pin-selectable resolution of 2000, 1000, 500 and 250 DPI (binning or averaging selectable)
- Integrating L-V conversion followed by a sample & hold circuit
- High sensitivity and uniformity over wavelength
- High pixel clock rate of up to 5 MHz
- Asynchronous, global shutter enables flexible integration times
- 3 V capable analogue output with separate supply pin
- Push-pull output amplifier

APPLICATIONS

- Triangulation sensors
- Contact image sensors
- ♦ CCD replacement



BLOCK DIAGRAM Pixel 1 Pixel 2 3 4 Ν VDDA VDD ESH RES0 Binning/ **Output Amplifier** RES1 VAO Averaging Sample & Hold Control BNA Read Pixel Control SI iC-LFHxxx CLK Power Down Reset GND GNDA

Rev B1, Page 2/14

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DESCRIPTION

iC-LFH Series are integrating light-to-voltage converters with 1024/960/640/320 pixels pitched at 12.7 μm (center-to-center distance). Each pixel consists of a 12.7 μm x 600 μm photodiode, an integration capacitor, and a sample-and-hold circuit.

The control logic makes operation very easy, with only a start and clock signal necessary. A third input (ESH) optionally controls the asynchronous, global shutter.

When the start signal is given, a new integration phase is initiated. Nine clocks are requiered to sample the

current integration value and to reset the integration capacitor. After further 7 clocks, while the internal dark level voltage (VMIN) is output at AO, the value of the pixel #1 can be read out. With further clocks the following pixel voltages are output. The complete line sensor is read out after 1040/976/656/336 clock pulses respectively.

iC-LFHxxx is suitable for high pixel clock rates of up to 5 MHz.

PACKAGING INFORMATION

PIN CONFIGURATION LFH1C

| 4 | \bigcirc | \bigcirc | \bigcirc | \bigcirc |
|---|------------------|------------|------------|------------|
| 3 | (\overline{D}) | \bigcirc | \bigcirc | <u> </u> |
| 2 | \bigcirc | | \bigcirc | <u> </u> |
| 1 | \bigcirc | \bigcirc | \bigcirc | \bigcirc |
| | Α | В | С | D |

PIN FUNCTIONS No. Name Function

| A1 | RES0 | Select Resolution Bit 0 |
|----|--|---|
| A2 | RES1 | Select Resolution Bit 1 |
| A3 | VAO | Pixel Output Supply Voltage |
| A4 | AO | Analog Pixel Output |
| B1 | VDD | Digital Supply +5 V |
| B2 | n/c | 0 11 2 |
| Β3 | n/c | |
| Β4 | VDDA | Analog Supply +5 V |
| C1 | ETP | Enable Test Mode* |
| C2 | GND | Digital Ground |
| C3 | GNDA | Analog Ground |
| C4 | NRES | Power-Down Reset Output (low active) |
| D1 | CLK | Clock |
| D2 | SI | Start of Integration |
| D3 | ESH | Enable Shutter |
| D4 | BNA | Select Binning/Averaging |
| | A1 A2 A3 B1 B2 B3 B4 C1 C2 C3 C4 D1 D2 D3 D4 | A1 RES0 A2 RES1 A3 VAO A4 AO B1 VDD B2 n/c B3 n/c B4 VDDA C1 ETP C2 GND C3 GNDA C4 NRES D1 CLK D2 SI D3 ESH D4 BNA |

*ETP must be connected to GND/GNDA

Rev B1, Page 3/14

aus

PIN CONFIGURATION LFH2C



PIN FUNCTIONS

No. Name Function

- 1 RES0 Select Resolution Bit 0
- 2 RES1 Select Resolution Bit 1
- 3 VDD Digital Supply +5 V
- 4 GND Digital Ground
- 5 ETP Enable Test Mode*
- 6 SI Start of Integration
- 7 CLK Clock
- 8 BNA Select Binning/Averaging
- 9 ESH Enable Shutter
- 10 NRES Power-Down Reset Output (low active)
- 11 GNDA Analog Ground
- 12 VDDA Analog Supply +5 V
- 13 VAO Pixel Output Supply Voltage
- 14 AO Analog Pixel Output

*ETP must be connected to GND/GNDA

PIN CONFIGURATION LFH3C



PIN FUNCTIONS

No. Name Function

- 1 RES0 Select Resolution Bit 0
- 2 RES1 Select Resolution Bit 1
- 3 VDD Digital Supply +5 V
- 4 GND Digital Ground
- 5 ETP Enable Test Mode*
- 6 SI Start of Integration
- 7 CLK Clock
- 8 BNA Select Binning/Averaging
- 9 ESH Enable Shutter
- 10 NRES Power-Down Reset Output (low active)
- 11 GNDA Analog Ground
- 12 VDDA Analog Supply +5 V
- 13 VAO Pixel Output Supply Voltage
- 14 AO Analog Pixel Output

*ETP must be connected to GND/GNDA

Rev B1, Page 4/14

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PIN CONFIGURATION LFH5C



PIN FUNCTIONS

No. Name Function

- 1 RES0 Select Resolution Bit 0
- 2 RES1 Select Resolution Bit 1
- 3 VDD Digital Supply +5 V
- 4 GND Digital Ground
- 5 ETP Enable Test Mode*
- 6 SI Start of Integration
- 7 CLK Clock
- 8 BNA Select Binning/Averaging
- 9 ESH Enable Shutter
- 10 NRES Power-Down Reset Output (low active)
- 11 GNDA Analog Ground
- 12 VDDA Analog Supply +5 V
- 13 VAO Pixel Output Supply Voltage
- 14 AO Analog Pixel Output

*ETP must be connected to GND/GNDA

Rev B1, Page 5/14

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

| Item | Symbol | Parameter | Conditions | | | Unit |
|------|--------|--|---|------|-----------|------|
| No. | | | | Min. | Max. | |
| G001 | VDD | Digital Supply Voltage | | -0.3 | 6 | V |
| G002 | VDDA | Analog Supply Voltage | | -0.3 | 6 | V |
| G003 | VAO | Analog Output AO Supply Voltage | | -0.3 | 6 | |
| G004 | V() | Voltage at SI, CLK, ESH, RES0, RES1, BNA, ETP | | -0.3 | VDD + 0.3 | V |
| G005 | l() | Current in AO | | -10 | 10 | mA |
| G006 | Vd() | ESD Susceptibility at all pins | HBM 100 pF, discharged through $1.5 k\Omega$ | | 4 | kV |
| G007 | Tj | Junction Temperature | | -40 | 150 | °C |
| G008 | Ts | Chip Storage Temperature | | -40 | 150 | °C |

THERMAL DATA

Operating Conditions: VDDA = VDD = $5 V \pm 10 \%$

| Item | Symbol | Parameter | Conditions | | | Unit | |
|------|--------|-------------------------------|---|------|------|------|--|
| No. | - | | | Min. | Тур. | Max. | |
| T01 | Та | Operating Ambient Temperature | See the relevant package specifications | | | | |

Rev B1, Page 6/14

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ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V \pm 10 %, Tj = -25...110 °C unless otherwise noted

| ltem | Symbol | Parameter | Conditions | | | | Unit |
|---------|-------------------------|--|--|------|----------|------|-------------------|
| No. | | | | Min. | Тур. | Max. | |
| Total L | Device | | | | | | |
| 001 | | Digital Supply Voltage Range | | 4.5 | | 5.5 | V |
| 002 | | Analog Supply Voltage Range | $f(C I(c) = 1 M I_{C}$ | 4.5 | | 5.5 | V |
| 003 | | Supply Current in VDD | | _ | 11 | 300 | μΑ |
| 004 | I(VDDA) | | N = 320 N = 640 | | 20 | 25 | mA mA |
| | | | N = 960 | | 26 | 30 | mA |
| | | | N = 1024 | _ | 28 | 32 | mA |
| 005 | Vc()hi | Clamp Voltage hi at SI, CLK, ESH, RES0, RES1, BNA, ETP, NRES | Vc()hi = V() - V(VDD), I() = 1 mA | 0.3 | | 1.8 | V |
| 006 | Vc()lo | Clamp Voltage lo at SI, CLK, ESH, RES0, RES1, BNA, ETP, NRES | Vc()hi = V() - V(GNDA), I() = -1 mA | -1.5 | | -0.3 | V |
| 007 | Vc()hi | Clamp Voltage hi at AO | Vc()hi = V(AO) - V(VAO), I(AO) = 1 mA | 0.3 | | 1.5 | V |
| 008 | Vc()lo | Clamp Voltage lo at AO, VDDA, VDD, GND | Vc()lo = V() - V(GNDA), I() = -1 mA | -1.5 | | -0.3 | V |
| Photo | diode Array | | | | | | |
| 201 | A() | Radiant Sensitive Area | 600 µm x 12.70 µm, per Pixel | | 0.00762 | | mm ² |
| 203 | λ ar | Spectral Application Range | $S(\lambda ar) = 0.25 \times S(\lambda)max$ | 420 | | 980 | nm |
| Analog | gue Output | AO, VAO | | | | | |
| 301 | V(VAO) | Permissible Input Voltage | G(AO) = 1 | 3 | 3.3 | 3.6 | V |
| | 10.00 | | G(AO) = 1.67 | 4.5 | 5.0 | 5.5 | V |
| 302 | I(VAO) | Supply Current in VAO | 10 pF load at AO, f(CLK) = 5 MHz; V(VAO) = 3 3 6 V | | | 25 | mA |
| | | | V(VAO) = 4.55.5 V | | | 3 | mA |
| 303 | G(AO) | Gain | VAO < th(VAO) | 0.9 | 1 | 1.1 | |
| | | T | VAO > th(VAO) | 1.3 | 1.67 | 1.8 | |
| 304 | Vt(VAO)hi | Threshold Voltage Gain Switch hi | | 3.7 | | 4.6 | V |
| 305 | Vt(VAO)lo | Threshold Voltage Gain Switch lo | | 3.5 | | 4.4 | V |
| 306 | Vt(VAO)nys | Hysteresis Gain Switch | | 100 | 400 | 350 | mv |
| 308 | VS(AO)NI | Saturation voltage ni | VS(AO)NI = VAO - V(AO), I(AO) = -2 mA | _ | 120 | 250 | mv |
| 309 | r | Sensitivity | $RES 1/0 = 00, \lambda = 775 \text{ nm};$ G(AO) = 1 | | 0.9 | | V/pWs |
| | | | G(AO) = 1.67 | | 1.5 | | V/pWs |
| 311 | KR | Sensitivity Ratio | K(Binning * 2) / K | | 1.8 | | |
| | | | K(Binning * 4) / K | | 3.3 | | |
| | | | K(Averaging * X) / K; X = 2, 4, 8 | | 1 | | |
| 312 | V0(AO) | Offset Voltage | Integration time 1 ms, no illumination | 100 | 200 | 500 | mV |
| 313 | ⊿V0(AO) | Offset Voltage Deviation during integration mode | $\Delta V0(AO) = V(AO)t1 - V(AO)t2,$ $\Delta t = t2 - t1 = 1 \text{ ms}$ | -150 | | 150 | mV |
| 314 | ⊿V(AO) | Signal Deviation during hold mode | $\Delta V(AO) = V(AO)t1 - V(AO)t2,$ $\Delta t = t2 - t1 = 1 \text{ ms}$ | -150 | | 150 | mV |
| 315 | tp(CLK-AO) | Settling Time | Cl(AO) = 10 pF, CLK lo \rightarrow hi until V(AO) = 0.95 * Vs(AO)hi | | | 200* | ns |
| 316 | PRNU | Pixel Response Nonuniformity | V(AO) = 2.5 V | | ±10 | ±15 | % |
| 317 | INL | Integral Nonlinearity | G(AO) = 1: V(AO) = 0.53.0 V, G(AO) = 1.67: V(AO) = 0.54.5 V | | ±1.5* | | % |
| 318 | V _{noise} (AO) | Output Noise Voltage | V(AO) = 2.5 V | | 1.5* | | mV _{RMS} |
| 319 | DR | Dynamic Range [†] | V(VAO) = 5.0 V; V(AO) _{max} = 5 V V(VAO) = 3.3 V; V(AO) _{max} = 3.3 V | | 70 66 | | dB dB |
| 320 | V(AO)min | Output Reference Voltage | | 150 | 200 | 280 | mV |
| Power | -Down Rese | et NRES | | | | | |
| 801 | VDDon | Power-On Release by VDD | | | 4.0 | 4.4 | V |

Rev B1, Page 7/14

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ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -25...110 °C unless otherwise noted

| ltem | Symbol | Parameter | Conditions | | | | Unit |
|--|---------|-----------------------------|---|--------------------|------|------|------|
| No. | | | | Min. | Тур. | Max. | |
| 802 | VDDoff | Power-Down Reset by VDD | | 3.0 | 3.5 | | V |
| 803 | VDDhys | Hysteresis | VDDhys = VDDon - VDDoff | 350 | 460 | 800 | mV |
| 804 | Vs()lo | Saturation Voltage lo | I() = 1.6 mA | 0 | | 0.3 | V |
| 805 | Vs()hi | Saturation Voltage hi | I() = -1.6 mA, Vs()hi = VDD - V() | 0 | | 0.3 | V |
| 806 | lsc()lo | Short Current lo | V() = lo and pin shorted with VDD | 5 | | 70 | mA |
| 807 | lsc()hi | Short Current hi | V() = hi and pin shorted with GND | -70 | | -5 | mA |
| TTL Input Interface BNA, CLK, ESH, ETP, RES0, RES1, SI | | | | | | | |
| 101 | Vt()hi | Threshold Voltage hi | | | | 2.0 | V |
| 102 | Vt()lo | Threshold Voltage lo | | 0.8 | | | V |
| 103 | Vt()hys | Hysteresis | Vt()hys = Vt()hi - Vt()lo | 200 | | 500 | mV |
| 104 | l()pd | Pull-Down Current | | 5 | 30 | 70 | μA |
| 105 | fclk | Permissible Clock Frequency | Reset integration and digital control Read Pixel and S&H | | | 10 | MHz |
| | | | N = 320 | (0.3)‡ | | 5 | MHz |
| | | | N = 640 | (0.6) [‡] | | 5 | MHz |
| | | <u> </u> | N = 960, 1024 | (1)∓ | | 5 | MHz |

OPTICAL CHARACTERISTICS: Diagrams



Figure 1: Relative spectral sensitivity

^{*} Projected values by sample characterization † $DR = 20 \times log \frac{V(AO)_{max} - VO(AO)_{max}}{V_{noise}(AO)}$

[‡] Relates to a 1 ms hold time; cf. Electrcal Characteristics Nos. 313 and 314.

Rev B1, Page 8/14

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OPERATING REQUIREMENTS: Integration and Read Control

Operating conditions: VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, Tj = -25...110 °C

| Item | Symbol | Parameter | Conditions | | | Unit |
|------------------------------|-----------------|--|------------|------|------|------|
| No. | | | | Min. | Max. | |
| Integration and Read Control | | | | | | |
| 1001 | t _C | Permissible Clock Period CLK | | 100 | | ns |
| 1002 | t _{L1} | Clock Signal CLK Hi-Level | | 50 | | ns |
| | | Duration | | | | |
| 1003 | t _{L2} | Clock Signal CLK Lo-Level Duration | | 50 | | ns |
| 1004 | t _{S1} | Setup Time: | | 50 | | ns |
| | | SI stable before CLK lo \rightarrow hi | | | | |
| 1005 | t _{H1} | Hold Time: | | 50 | | ns |
| | | SI stable after CLK lo \rightarrow hi | | | | |
| 1006 | t _{L3} | Shutter Signal ESH Lo-Level Duration | | 100 | | ns |



Figure 2: Timing diagram





preliminary **iC-LFH Series** HIGH-RESOLUTION LINEAR IMAGE SENSORS

Rev B1, Page 9/14

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DESCRIPTION OF FUNCTIONS

Pixel structure and resolution

One pixel consist of a photodiode, an integration capacitor, and an S&H stage. For reducing the resolution, the pixels can be grouped together by means of pins RES1/0. Changing the resolution can be achieved in two ways, binning or averaging. Averaging does not change the sensitivity, whereas binning increases the sensitivity by the ratio given in the table on the right. Pin BNA selects the mode respectively.

| PINS RES1/0 | | | | | | |
|-------------|----------------------------|-----------------------------|------------|--------------------------------|--|--|
| State | Pin BNA | Pixels | Resolution | Sensitivity ratio ¹ | | |
| 0/0 | - | N pixels | 2000 dpi | 1 | | |
| 0/1 | 0 | N/2 pixels | 1000 dpi | 1 | | |
| | 1 | N/2 pixels | 1000 dpi | 1.8 | | |
| 1/0 | 0 | N/4 pixels | 500 dpi | 1 | | |
| | 1 | N/4 pixels | 500 dpi | 3.3 | | |
| 1/1 | 0 | N/8 pixels | 250 dpi | 1 | | |
| | 1 | N/8 pixels | 250 dpi | 4.7 | | |
| | ¹ all pixels ur | niformly illumi | nated | | | |
| | N = 320/640 | N = 320/640/960/1024 pixels | | | | |



Figure 4: Pixel structure with RES1/0 = 00



Figure 5: Pixel structure with resolution change and averaging mode

Rev B1, Page 10/14

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Figure 6: Pixel structure with resolution change and binning mode

Operation description

Following an internal power-on reset the integration and hold capacitors are discharged. A high signal at SI and a rising edge at CLK triggers a readout cycle and with it a new integration cycle. Six clocks later the internal reset is done and the device is in integration mode. The readout of the analog pixel values starts with the 17th clock pulse.

Operation with the shutter function

Integration can be suspended at any time via pin ESH (asynchronous, global shutter), i.e. the photodiodes are disconnected from their corresponding integration capacitor when ESH is high and the current integration capacitor voltages are maintained. If this pin is open or switched to GND, the pixel photocurrents are summed up by the integration capacitors until the next SI signal.



Figure 7: example integration and readout cycle

iC-LFH Series preliminary indication linear image sensors

Rev B1, Page 11/14

READ CONTROL

The readout of the analog pixel values is controlled by the followoing pins:

- Pin SI
- Pin CLK

A rising CLK edge with a hi value at SI resets the internal read out circuit, initiating a readout of the previously sampled pixel values. While clocking more then N clocks the read out will restart with pixel #1 without sampling. Thus a non-destructive re-read is possible.



Figure 10: Non-destructive restart of readout cycle

Rev B1, Page 12/14

aus

INTEGRATION CONTROL

The integration is controlled by the signals:

- Pin SI
- Pin CLK
- Pin ESH

A new integration phase is started with a rising CLK edge and SI high. After 9 clocks a new integration cy-

cle is initiated. With pin ESH = Io all photodiodes are connected to the internal capacitors and the photodiode currents are integrated. The integration can be suspended by setting pin ESH to hi, disconnecting the photodiodes from their integration capacitors.



Figure 13: Integration cycle with shutter action and readout interrupt

Rev B1, Page 13/14

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DESIGN REVIEW: Function Notes

| iC-LFHxxx 1 | iC-LFHxxx 1 | | | | | |
|----------------|---|---|--|--|--|--|
| No. | Function, parameter/code | Description and application notes | | | | |
| 1 | Sensitivity ratio with binning, Electrical Characteristics No. 309 | Gain increase in binning is lower than stated | | | | |
| 2 | Settling time, Electrical Characteristics No. 314 | Dips in the pixel voltage slow down settling time | | | | |

Table 5: Notes on chip functions regarding iC-LFHxxx chip release 1

| iC-LFHxxx Z | | |
|----------------|--|---|
| No. | Function, parameter/code | Description and application notes |
| 1 | Binning/averaging | Binning/averaging cannot be used |
| 2 | Settling time, Electrical Characteristics No. 314 | Dips in the pixel voltage slow down settling time |

Table 6: Notes on chip functions regarding iC-LFHxxx chip release Z

| iC-LFHxxx Z1 | | |
|-----------------|--|---|
| No. | Function, parameter/code | Description and application notes |
| 1 | Settling time, Electrical Characteristics No. 314 | Dips in the pixel voltage slow down settling time |

Table 7: Notes on chip functions regarding iC-LFHxxx chip release Z1

REVISION HISTORY

| Rel. | Rel. Date* | Chapter | Modification | Page |
|------|------------|-------------------------------|---|------|
| B1 | 2017-09-01 | ELECTRICAL CHARACTERISTICS | Operating conditions: Tj = -25110 °C | 6-7 |
| | | ELECTRICAL CHARACTERISTICS | Item No. 302 added | 6 |
| | | ELECTRICAL CHARACTERISTICS | Item Nos. 309, 311 corrected | 6 |
| | | ELECTRICAL CHARACTERISTICS | OPTICAL CHARACTERISTICS: Diagrams updated | 7 |
| | | OPERATING REQUIREMENTS | Operating conditions: Tj = -25110 °C | 8 |
| | | DESCRIPTION OF FUNCTIONS | PINS RES1/0 table corrected | 9 |

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iC-LFH Series

HIGH-RESOLUTION LINEAR IMAGE SENSORS



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ORDERING INFORMATION

| Туре | Package | Order Designation |
|------------|------------|-----------------------|
| iC-LFH320 | oBGA LFH1C | iC-LFH320 oBGA LFH1C |
| iC-LFH640 | oBGA LFH2C | iC-LFH640 oBGA LFH2C |
| iC-LFH960 | oBGA LFH3C | iC-LFH960 oBGA LFH3C |
| iC-LFH1024 | oBGA LFH5C | iC-LFH1024 oBGA LFH5C |

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