iC-LFH Series

HIGH-RESOLUTION LINEAR IMAGE SENSORS

preliminary

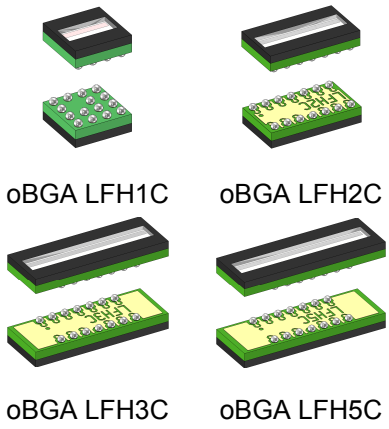
FEATURES

- 1024/960/640/320 active photo pixels with 12.7 µm x 600 µm (2000 DPI)
- Pin-selectable resolution of 2000, 1000, 500 and 250 DPI (binning or averaging selectable)
- Integrating L-V conversion followed by a sample & hold circuit
- High sensitivity and uniformity over wavelength
- High pixel clock rate of up to 5 MHz
- Asynchronous, global shutter enables flexible integration times
- 3 V capable analogue output with separate supply pin
- Push-pull output amplifier

APPLICATIONS

- Triangulation sensors
- Contact image sensors
- CCD replacement

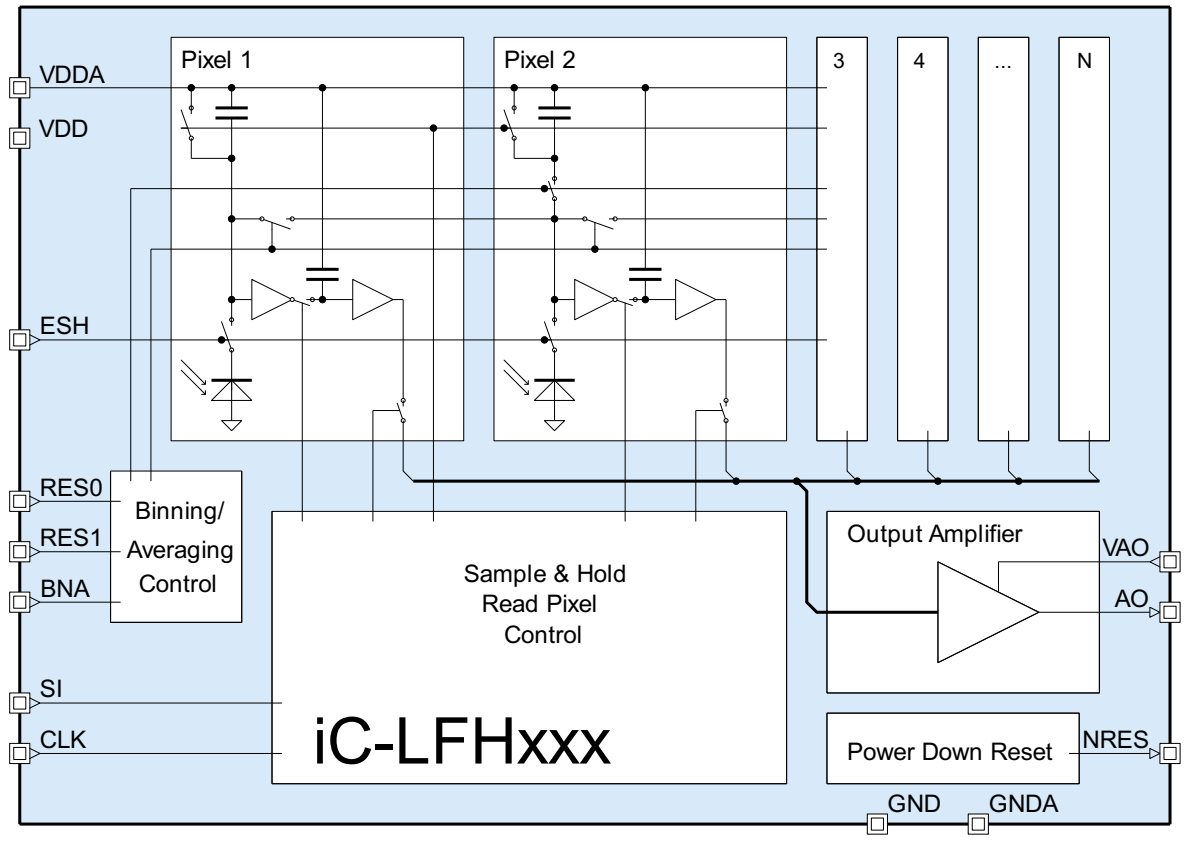
PACKAGES



oBGA LFH1C oBGA LFH2C

oBGA LFH3C oBGA LFH5C

BLOCK DIAGRAM



DESCRIPTION

iC-LFH Series are integrating light-to-voltage converters with 1024/960/640/320 pixels pitched at 12.7 µm (center-to-center distance). Each pixel consists of a 12.7 µm x 600 µm photodiode, an integration capacitor, and a sample-and-hold circuit.

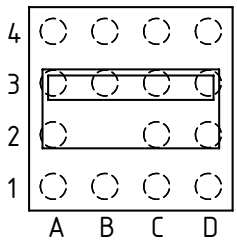
The control logic makes operation very easy, with only a start and clock signal necessary. A third input (ESH) optionally controls the asynchronous, global shutter.

When the start signal is given, a new integration phase is initiated. Nine clocks are requiered to sample the current integration value and to reset the integration capacitor. After further 7 clocks, while the internal dark level voltage (VMIN) is output at AO, the value of the pixel #1 can be read out. With further clocks the following pixel voltages are output. The complete line sensor is read out after 1040/976/656/336 clock pulses respectively.

iC-LFHxxx is suitable for high pixel clock rates of up to 5 MHz.

PACKAGING INFORMATION

PIN CONFIGURATION LFH1C

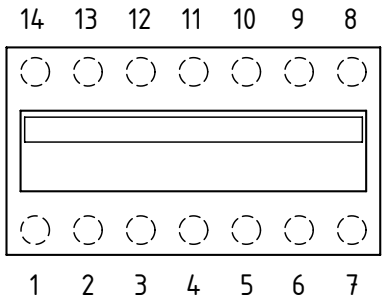


PIN FUNCTIONS

No.	Name	Function
A1	RES0	Select Resolution Bit 0
A2	RES1	Select Resolution Bit 1
A3	VAO	Pixel Output Supply Voltage
A4	AO	Analog Pixel Output
B1	VDD	Digital Supply +5 V
B2	n/c	
B3	n/c	
B4	VDDA	Analog Supply +5 V
C1	ETP	Enable Test Mode*
C2	GND	Digital Ground
C3	GNDA	Analog Ground
C4	NRES	Power-Down Reset Output (low active)
D1	CLK	Clock
D2	SI	Start of Integration
D3	ESH	Enable Shutter
D4	BNA	Select Binning/Averaging

*ETP must be connected to GND/GNDA

PIN CONFIGURATION LFH2C

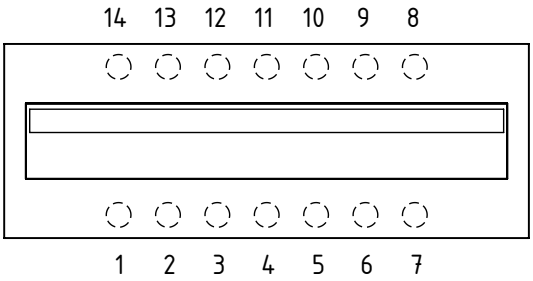


PIN FUNCTIONS

No.	Name	Function
1	RES0	Select Resolution Bit 0
2	RES1	Select Resolution Bit 1
3	VDD	Digital Supply +5 V
4	GND	Digital Ground
5	ETP	Enable Test Mode*
6	SI	Start of Integration
7	CLK	Clock
8	BNA	Select Binning/Averaging
9	ESH	Enable Shutter
10	NRES	Power-Down Reset Output (low active)
11	GNDA	Analog Ground
12	VDDA	Analog Supply +5 V
13	VAO	Pixel Output Supply Voltage
14	AO	Analog Pixel Output

*ETP must be connected to GND/GNDA

PIN CONFIGURATION LFH3C

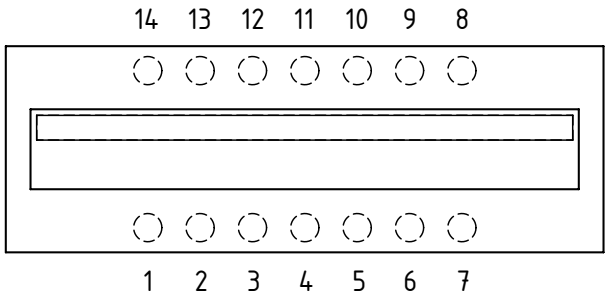


PIN FUNCTIONS

No.	Name	Function
1	RES0	Select Resolution Bit 0
2	RES1	Select Resolution Bit 1
3	VDD	Digital Supply +5 V
4	GND	Digital Ground
5	ETP	Enable Test Mode*
6	SI	Start of Integration
7	CLK	Clock
8	BNA	Select Binning/Averaging
9	ESH	Enable Shutter
10	NRES	Power-Down Reset Output (low active)
11	GNDA	Analog Ground
12	VDDA	Analog Supply +5 V
13	VAO	Pixel Output Supply Voltage
14	AO	Analog Pixel Output

*ETP must be connected to GND/GNDA

PIN CONFIGURATION LFH5C



PIN FUNCTIONS

No.	Name	Function
1	RES0	Select Resolution Bit 0
2	RES1	Select Resolution Bit 1
3	VDD	Digital Supply +5 V
4	GND	Digital Ground
5	ETP	Enable Test Mode*
6	SI	Start of Integration
7	CLK	Clock
8	BNA	Select Binning/Averaging
9	ESH	Enable Shutter
10	NRES	Power-Down Reset Output (low active)
11	GNDA	Analog Ground
12	VDDA	Analog Supply +5 V
13	VAO	Pixel Output Supply Voltage
14	AO	Analog Pixel Output

*ETP must be connected to GND/GNDA

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Digital Supply Voltage		-0.3	6	V
G002	VDDA	Analog Supply Voltage		-0.3	6	V
G003	VAO	Analog Output AO Supply Voltage		-0.3	6	
G004	V()	Voltage at SI, CLK, ESH, RES0, RES1, BNA, ETP		-0.3	VDD + 0.3	V
G005	I()	Current in AO		-10	10	mA
G006	Vd()	ESD Susceptibility at all pins	HBM 100 pF, discharged through 1.5 kΩ		4	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Chip Storage Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VDDA = VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature	See the relevant package specifications				

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -25...110 °C unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Digital Supply Voltage Range		4.5		5.5	V
002	VDDA	Analog Supply Voltage Range		4.5		5.5	V
003	I(VDD)	Supply Current in VDD	f(CLK) = 1 MHz			300	µA
004	I(VDDA)	Supply Current in VDDA	N = 320 N = 640 N = 960 N = 1024		11 20 26 28	15 25 30 32	mA mA mA mA
005	Vc()hi	Clamp Voltage hi at SI, CLK, ESH, RES0, RES1, BNA, ETP, NRES	Vc()hi = V() − V(VDD), I() = 1 mA	0.3		1.8	V
006	Vc()lo	Clamp Voltage lo at SI, CLK, ESH, RES0, RES1, BNA, ETP, NRES	Vc()hi = V() − V(GNDA), I() = -1 mA	-1.5		-0.3	V
007	Vc()hi	Clamp Voltage hi at AO	Vc()hi = V(AO) − V(VAO), I(AO) = 1 mA	0.3		1.5	V
008	Vc()lo	Clamp Voltage lo at AO, VDDA, VDD, GND	Vc()lo = V() − V(GNDA), I() = -1 mA	-1.5		-0.3	V
Photodiode Array							
201	A()	Radiant Sensitive Area	600 µm x 12.70 µm, per Pixel		0.00762		mm^2
203	λar	Spectral Application Range	S(λar) = 0.25 x S(λ)max	420		980	nm
Analogue Output AO, VAO							
301	V(VAO)	Permissible Input Voltage	G(AO) = 1 G(AO) = 1.67	3 4.5	3.3 5.0	3.6 5.5	V V
302	I(VAO)	Supply Current in VAO	10 pF load at AO, f(CLK) = 5 MHz; V(VAO) = 3...3.6 V V(VAO) = 4.5...5.5 V			2.5 3	mA mA
303	G(AO)	Gain	VAO < th(VAO) VAO > th(VAO)	0.9 1.3	1 1.67	1.1 1.8	
304	Vt(VAO)hi	Threshold Voltage Gain Switch hi		3.7		4.6	V
305	Vt(VAO)lo	Threshold Voltage Gain Switch lo		3.5		4.4	V
306	Vt(VAO)hys	Hysteresis Gain Switch		100		350	mV
308	Vs(AO)hi	Saturation Voltage hi	Vs(AO)hi = VAO − V(AO), I(AO) = -2 mA		120	250	mV
309	K	Sensitivity	RES1/0 = 00, λ = 775 nm; G(AO) = 1 G(AO) = 1.67		 0.9 1.5		 V/pWs V/pWs
311	KR	Sensitivity Ratio	K(Binning ∗ 2) / K K(Binning ∗ 4) / K K(Binning ∗ 8) / K K(Averaging ∗ X) / K; X = 2, 4, 8		1.8 3.3 4.7 1		
312	V0(AO)	Offset Voltage	Integration time 1 ms, no illumination	100	200	500	mV
313	ΔV0(AO)	Offset Voltage Deviation during integration mode	ΔV0(AO) = V(AO)t1 − V(AO)t2, Δt = t2 − t1 = 1 ms	-150		150	mV
314	ΔV(AO)	Signal Deviation during hold mode	ΔV(AO) = V(AO)t1 − V(AO)t2, Δt = t2 − t1 = 1 ms	-150		150	mV
315	tp(CLK-AO)	Settling Time	Cl(AO) = 10 pF, CLK lo → hi until V(AO) = 0.95 ∗ Vs(AO)hi			200*	ns
316	PRNU	Pixel Response Nonuniformity	V(AO) = 2.5 V		±10	±15	%
317	INL	Integral Nonlinearity	G(AO) = 1: V(AO) = 0.5...3.0 V, G(AO) = 1.67: V(AO) = 0.5...4.5 V		±1.5*		%
318	V_{noise}(AO)	Output Noise Voltage	V(AO) = 2.5 V		1.5*		mV_{RMS}
319	DR	Dynamic Range†	V(VAO) = 5.0 V; $V(AO)_{max}$ = 5 V V(VAO) = 3.3 V; $V(AO)_{max}$ = 3.3 V		70 66		dB dB
320	V(AO)min	Output Reference Voltage		150	200	280	mV
Power-Down Reset NRES							
801	VDDon	Power-On Release by VDD			4.0	4.4	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -25...110 °C unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
802	VDDoff	Power-Down Reset by VDD		3.0	3.5		V
803	VDDhys	Hysteresis	VDDhys = VDDon − VDDoff	350	460	800	mV
804	Vs()lo	Saturation Voltage lo	I() = 1.6 mA	0		0.3	V
805	Vs()hi	Saturation Voltage hi	I() = -1.6 mA, Vs()hi = VDD − V()	0		0.3	V
806	Isc()lo	Short Current lo	V() = lo and pin shorted with VDD	5		70	mA
807	Isc()hi	Short Current hi	V() = hi and pin shorted with GND	-70		-5	mA
TTL Input Interface BNA, CLK, ESH, ETP, RES0, RES1, SI							
I01	Vt()hi	Threshold Voltage hi				2.0	V
I02	Vt()lo	Threshold Voltage lo		0.8			V
I03	Vt()hys	Hysteresis	Vt()hys = Vt()hi − Vt()lo	200		500	mV
I04	I()pd	Pull-Down Current		5	30	70	µA
I05	fclk	Permissible Clock Frequency	Reset integration and digital control Read Pixel and S&H; N = 320 N = 640 N = 960, 1024	 (0.3)‡ (0.6)‡ (1)‡		10 5 5 5	MHz MHz MHz MHz

OPTICAL CHARACTERISTICS: Diagrams

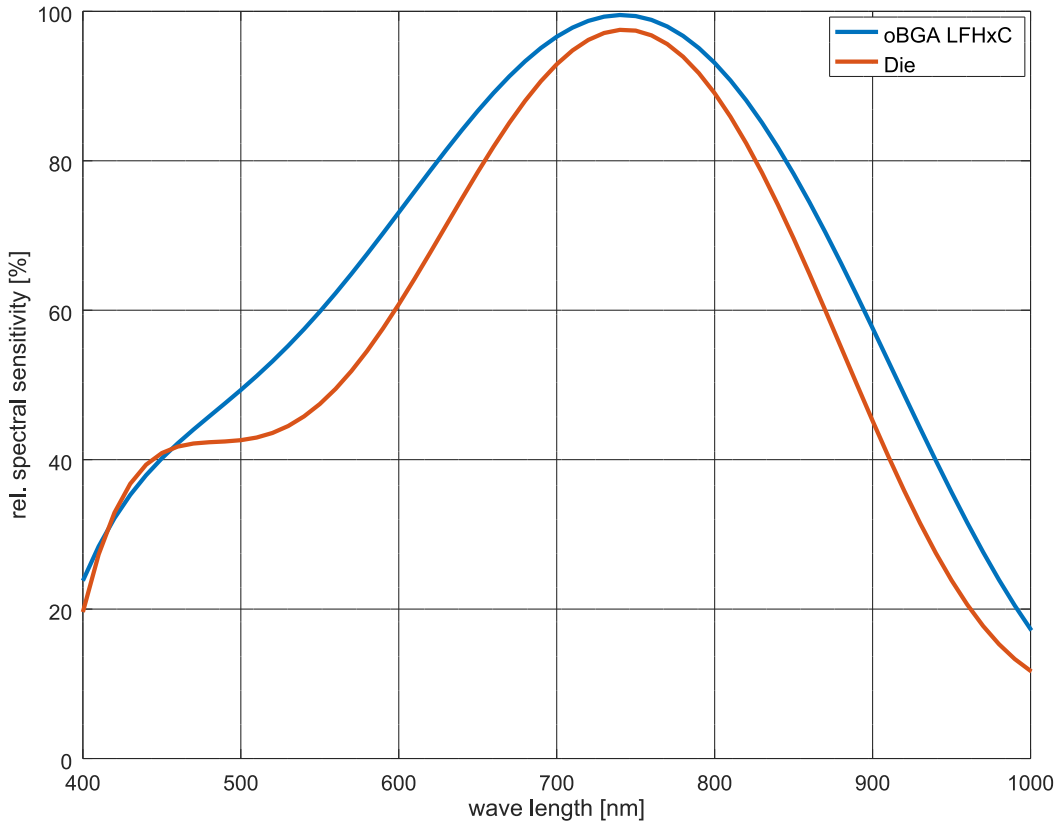


Figure 1: Relative spectral sensitivity

* Projected values by sample characterization

† $DR = 20 \times log \frac{V(AO)_{max} - V0(AO)_{max}}{V_{noise}(AO)}$

‡ Relates to a 1 ms hold time; cf. Electrcal Characteristics Nos. 313 and 314.

OPERATING REQUIREMENTS: Integration and Read Control

Operating conditions: VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, Tj = -25...110 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Integration and Read Control						
I001	t_C	Permissible Clock Period CLK		100		ns
I002	t_{L1}	Clock Signal CLK Hi-Level Duration		50		ns
I003	t_{L2}	Clock Signal CLK Lo-Level Duration		50		ns
I004	t_{S1}	Setup Time: SI stable before CLK lo → hi		50		ns
I005	t_{H1}	Hold Time: SI stable after CLK lo → hi		50		ns
I006	t_{L3}	Shutter Signal ESH Lo-Level Duration		100		ns

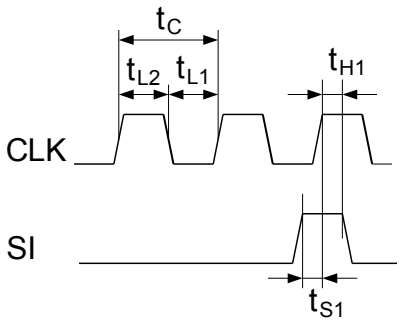


Figure 2: Timing diagram

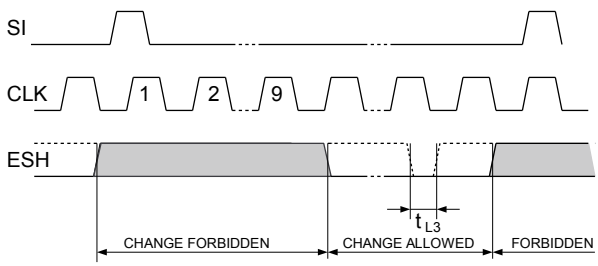


Figure 3: Timing diagram shutter

DESCRIPTION OF FUNCTIONS

Pixel structure and resolution

One pixel consist of a photodiode, an integration capacitor, and an S&H stage. For reducing the resolution, the pixels can be grouped together by means of pins RES1/0. Changing the resolution can be achieved in two ways, binning or averaging. Averaging does not change the sensitivity, whereas binning increases the sensitivity by the ratio given in the table on the right. Pin BNA selects the mode respectively.

PINS RES1/0				
State	Pin BNA	Pixels	Resolution	Sensitivity ratio[1]
0/0	-	N pixels	2000 dpi	1
0/1	0	N/2 pixels	1000 dpi	1
	1	N/2 pixels	1000 dpi	1.8
1/0	0	N/4 pixels	500 dpi	1
	1	N/4 pixels	500 dpi	3.3
1/1	0	N/8 pixels	250 dpi	1
	1	N/8 pixels	250 dpi	4.7
	[1]all pixels uniformly illuminated N = 320/640/960/1024 pixels			

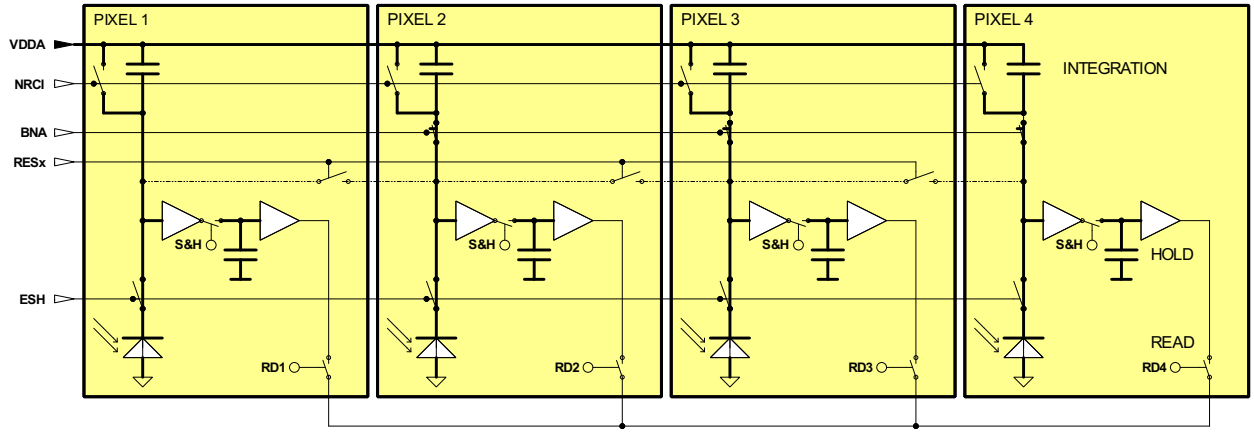


Figure 4: Pixel structure with RES1/0 = 00

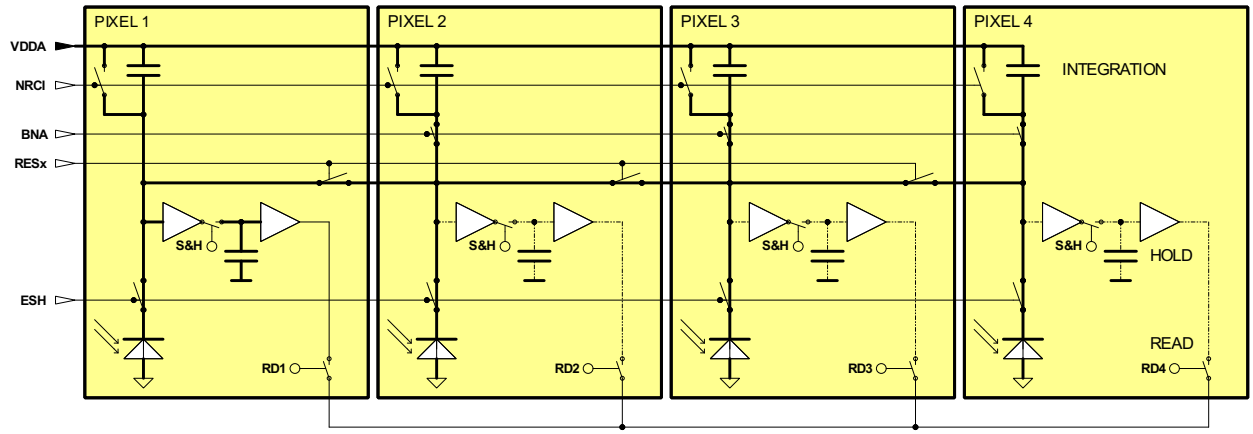


Figure 5: Pixel structure with resolution change and averaging mode

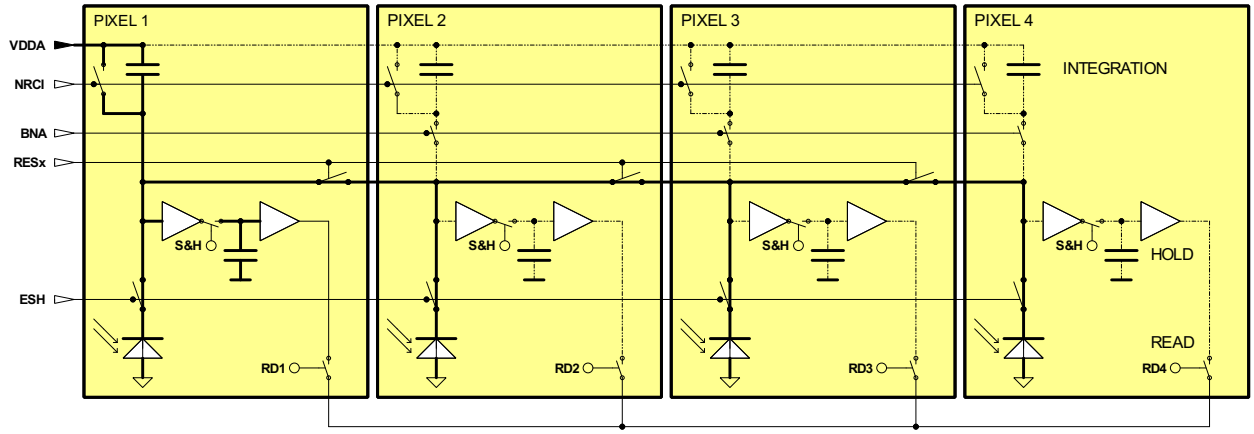


Figure 6: Pixel structure with resolution change and binning mode

Operation description

Following an internal power-on reset the integration and hold capacitors are discharged. A high signal at SI and a rising edge at CLK triggers a readout cycle and with it a new integration cycle. Six clocks later the internal reset is done and the device is in integration mode. The readout of the analog pixel values starts with the 17th clock pulse.

Operation with the shutter function

Integration can be suspended at any time via pin ESH (asynchronous, global shutter), i.e. the photodiodes are disconnected from their corresponding integration capacitor when ESH is high and the current integration capacitor voltages are maintained. If this pin is open or switched to GND, the pixel photocurrents are summed up by the integration capacitors until the next SI signal.

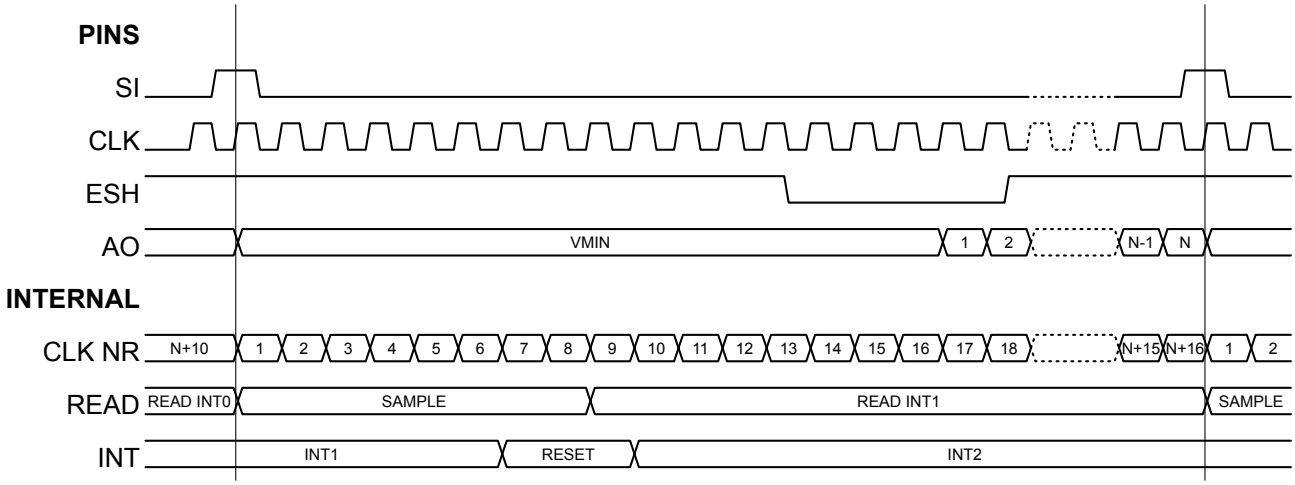


Figure 7: example integration and readout cycle

READ CONTROL

The readout of the analog pixel values is controlled by the followoing pins:

- Pin SI
- Pin CLK

A rising CLK edge with a hi value at SI resets the internal read out circuit, initiating a readout of the previously sampled pixel values. While clocking more then N clocks the read out will restart with pixel #1 without sampling. Thus a non-destructive re-read is possible.

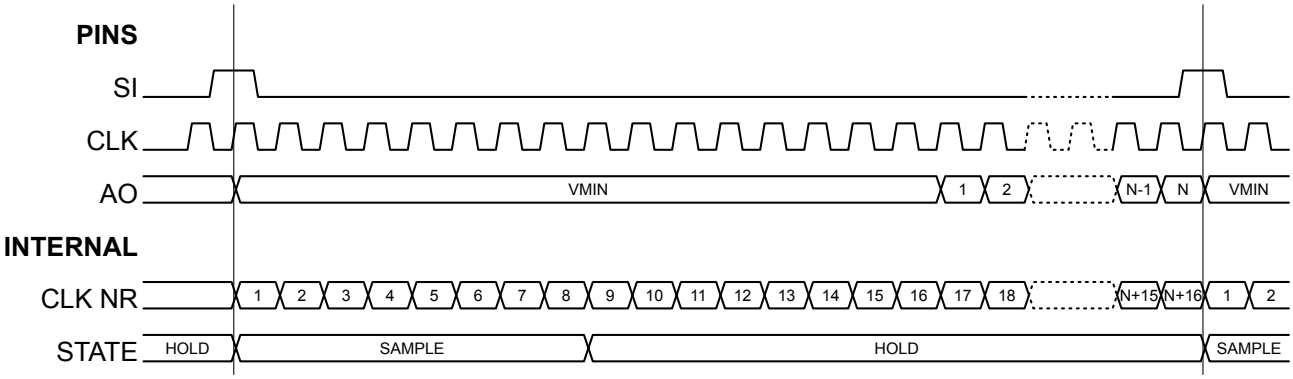


Figure 8: Complete readout cycle

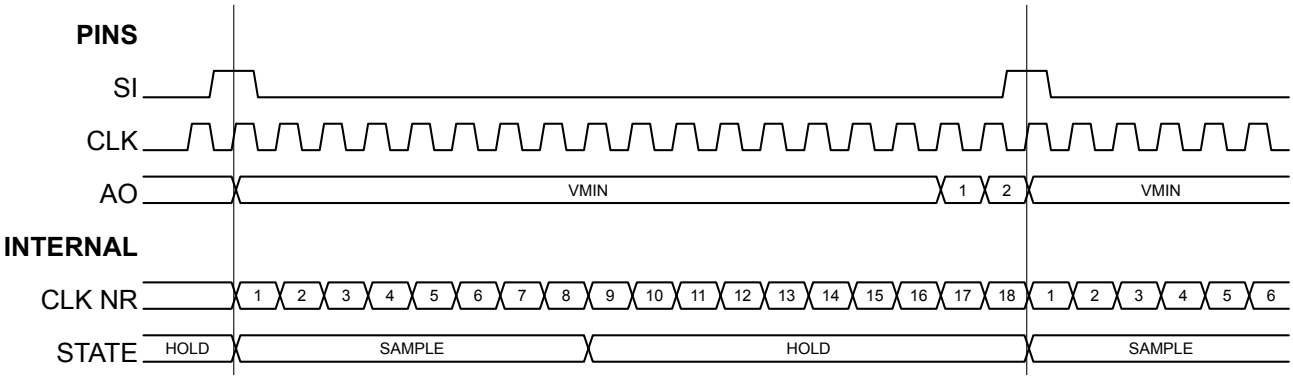


Figure 9: Interrupting the readout cycle

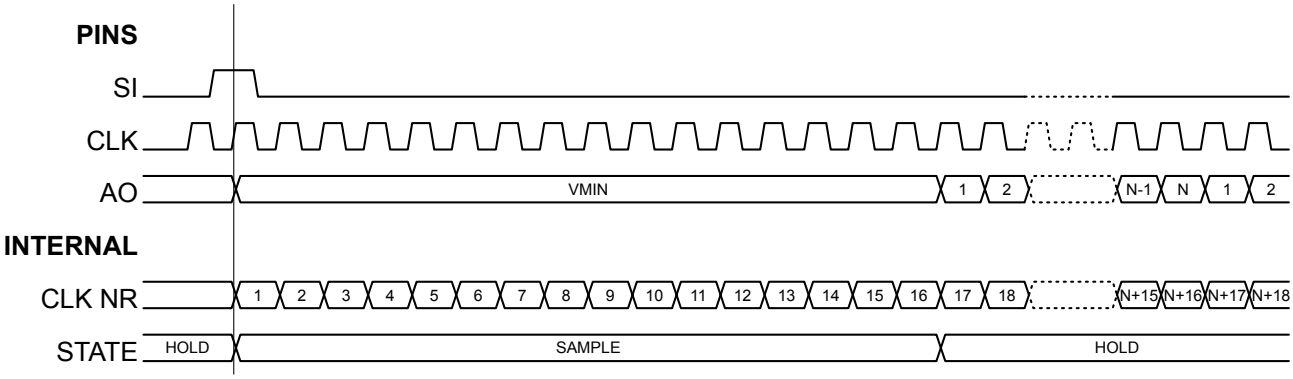


Figure 10: Non-destructive restart of readout cycle

INTEGRATION CONTROL

The integration is controlled by the signals:

- Pin SI
- Pin CLK
- Pin ESH

A new integration phase is started with a rising CLK edge and SI high. After 9 clocks a new integration cycle is initiated. With pin ESH = lo all photodiodes are connected to the internal capacitors and the photodiode currents are integrated. The integration can be suspended by setting pin ESH to hi, disconnecting the photodiodes from their integration capacitors.

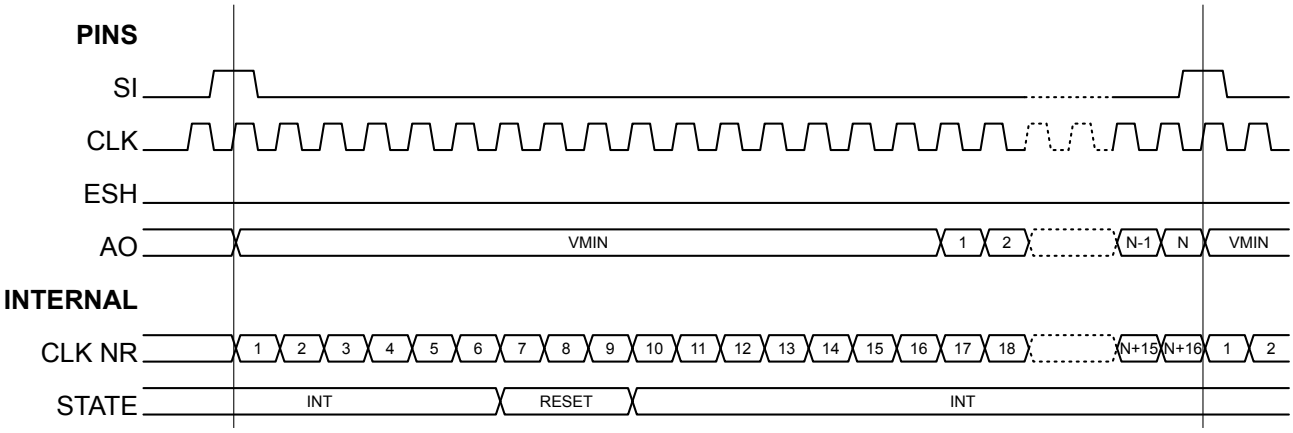


Figure 11: Integration cycle

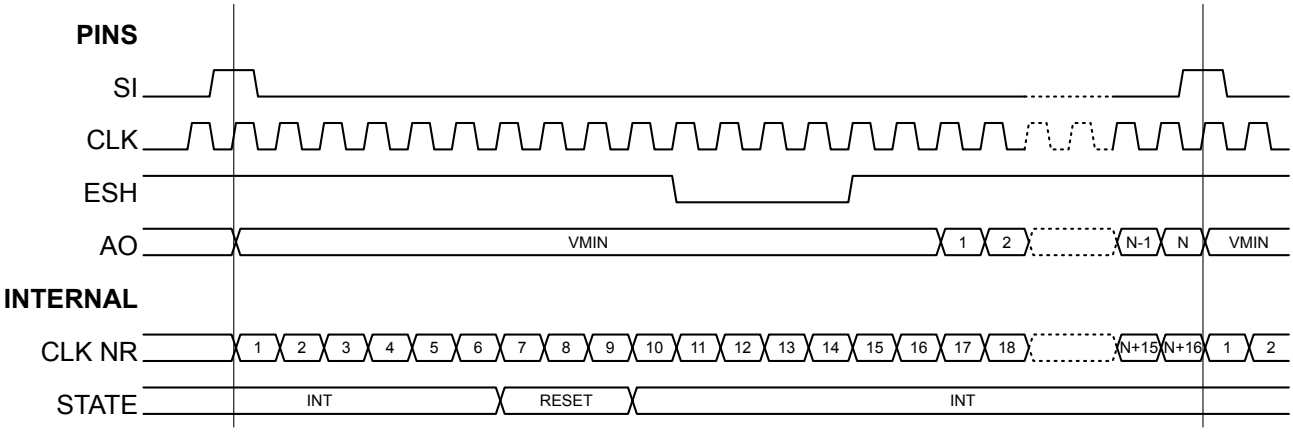


Figure 12: Integration cycle with shutter action

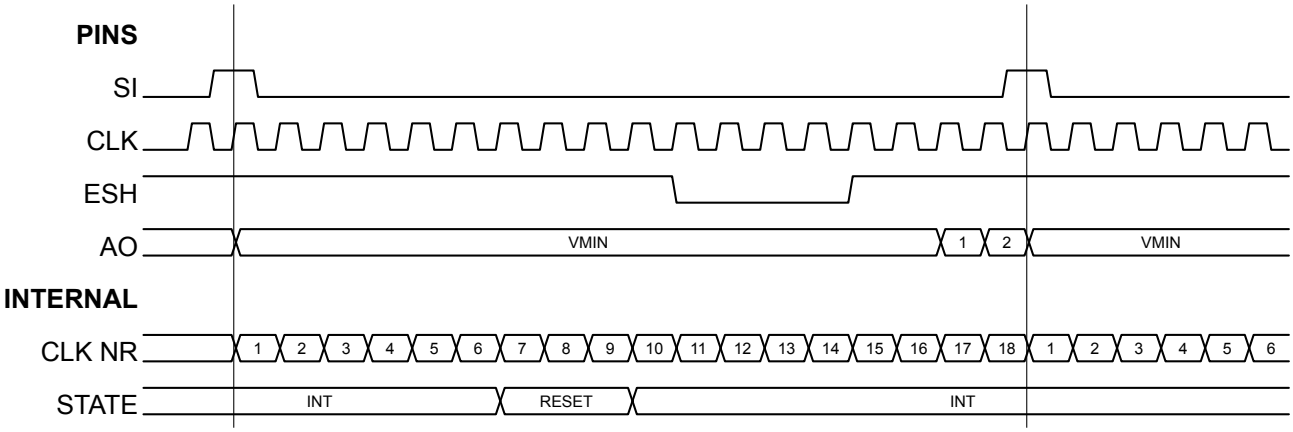


Figure 13: Integration cycle with shutter action and readout interrupt

DESIGN REVIEW: Function Notes

iC-LFHxxx 1		
No.	Function, parameter/code	Description and application notes
1	Sensitivity ratio with binning, Electrical Characteristics No. 309	Gain increase in binning is lower than stated
2	Settling time, Electrical Characteristics No. 314	Dips in the pixel voltage slow down settling time

Table 5: Notes on chip functions regarding iC-LFHxxx chip release 1

iC-LFHxxx Z		
No.	Function, parameter/code	Description and application notes
1	Binning/averaging	Binning/averaging cannot be used
2	Settling time, Electrical Characteristics No. 314	Dips in the pixel voltage slow down settling time

Table 6: Notes on chip functions regarding iC-LFHxxx chip release Z

iC-LFHxxx Z1		
No.	Function, parameter/code	Description and application notes
1	Settling time, Electrical Characteristics No. 314	Dips in the pixel voltage slow down settling time

Table 7: Notes on chip functions regarding iC-LFHxxx chip release Z1

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2017-09-01	ELECTRICAL CHARACTERISTICS	Operating conditions: Tj = -25...110 °C	6-7
		ELECTRICAL CHARACTERISTICS	Item No. 302 added	6
		ELECTRICAL CHARACTERISTICS	Item Nos. 309, 311 corrected	6
		ELECTRICAL CHARACTERISTICS	OPTICAL CHARACTERISTICS: Diagrams updated	7
		OPERATING REQUIREMENTS	Operating conditions: Tj = -25...110 °C	8
		DESCRIPTION OF FUNCTIONS	PINS RES1/0 table corrected	9

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-LFH320	oBGA LFH1C	iC-LFH320 oBGA LFH1C
iC-LFH640	oBGA LFH2C	iC-LFH640 oBGA LFH2C
iC-LFH960	oBGA LFH3C	iC-LFH960 oBGA LFH3C
iC-LFH1024	oBGA LFH5C	iC-LFH1024 oBGA LFH5C

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