IS61C64AL

8K x 8 HIGH-SPEED CMOS STATIC RAM

MARCH 2006

FEATURES

- High-speed access time: 10 ns
- CMOS low power operation
  - — 1 mW (typical) CMOS standby
  - — 125 mW (typical) operating
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation: no clock or refresh required
- Lead-free available

DESCRIPTION

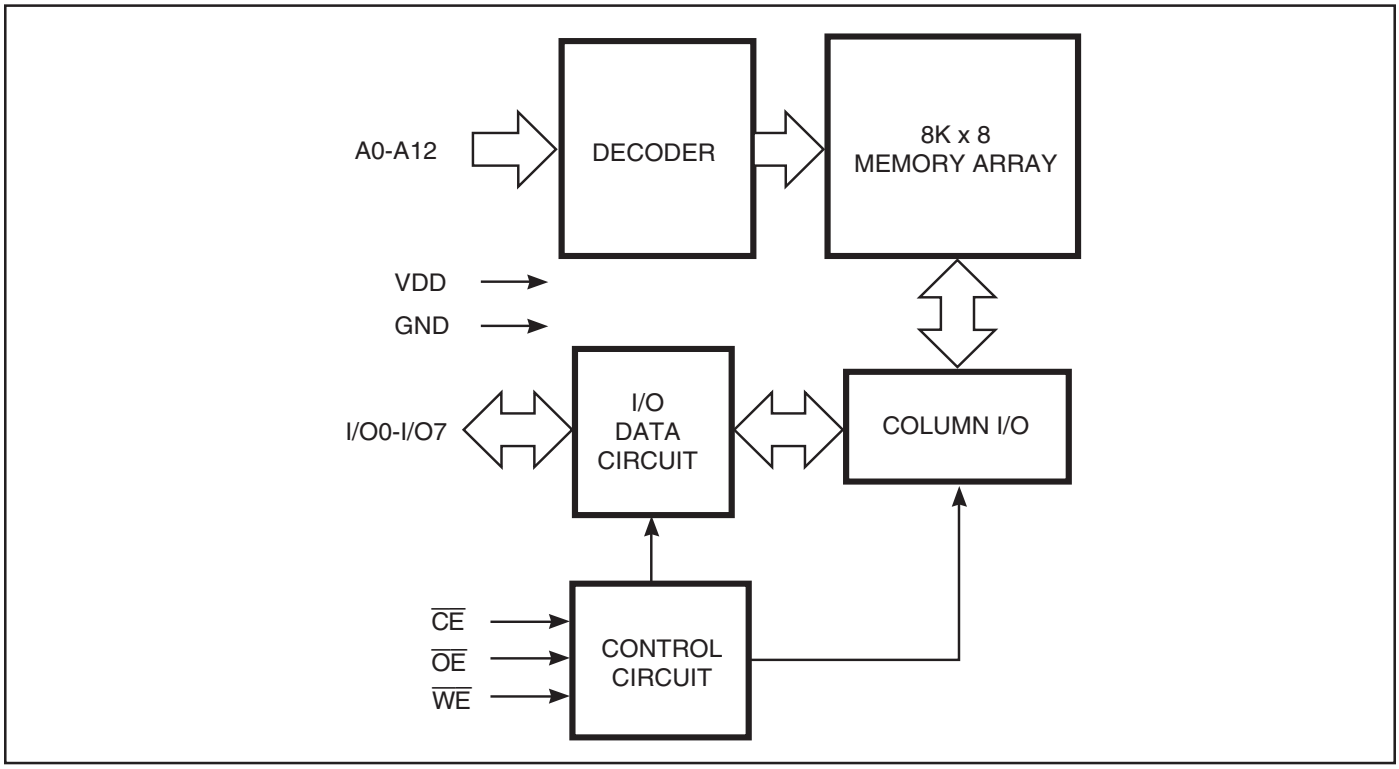
The *ISSI* IS61C64AL is a very high-speed, low power, 8192-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 150 µW (typical) with CMOS input levels.

Easy memory expansion is provided by using one Chip Enable input, $\overline{CE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61C64AL is packaged in the JEDEC standard 28-pin, 300-mil SOJ, and TSOP.

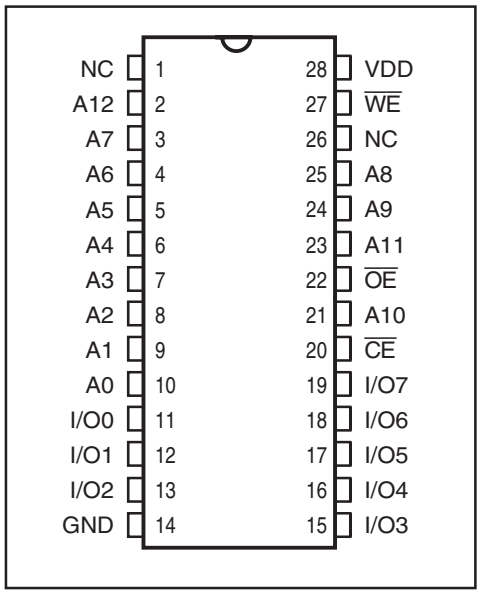
FUNCTIONAL BLOCK DIAGRAM



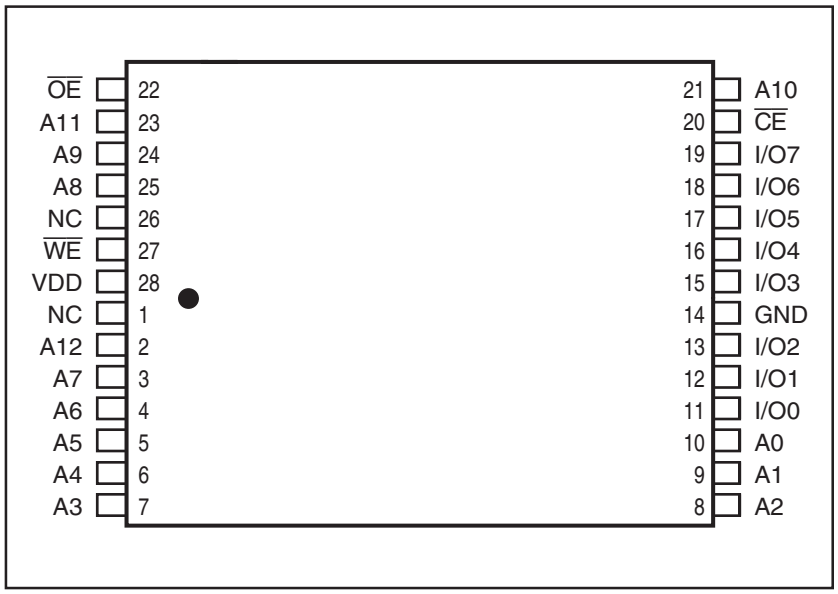
TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

PIN CONFIGURATION
28-Pin SOJ



PIN CONFIGURATION
28-Pin TSOP (Type 1)



PIN DESCRIPTIONS

A0-A12	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connect
V_{DD}	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	V_{DD}[1]
Commercial	0°C to +70°C	-10	5V ± 5%
Industrial	–40°C to +85°C	-10	5V ± 5%

Note:
1. If operated at 12ns, V_{DD} range is 5V ± 10%.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	Com.	–1	1	µA
			Ind.	–2	2	

Note:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = 0	Com.	—	20	—	20	mA
			Ind.	—	25	—	25	
I_{CC2}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	45	—	35	mA
			Ind.	—	50	—	45	
			typ.[2]	25		25		
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	1	—	1	mA
			Ind.	—	2	—	2	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com.	—	350	—	350	µA
			Ind.	—	450	—	450	
			typ.[2]	200		200		

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C. Not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 ns Min.	-10 ns Max	-12 ns Min.	-12 ns Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACS}	$\overline{CE}$ Access Time	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	—	6	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	6	ns
t_{LZCS}[2]	$\overline{CE}$ to Low-Z Output	2	—	3	—	ns
t_{HZCS}[2]	$\overline{CE}$ to High-Z Output	—	5	—	7	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	10	—	12	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

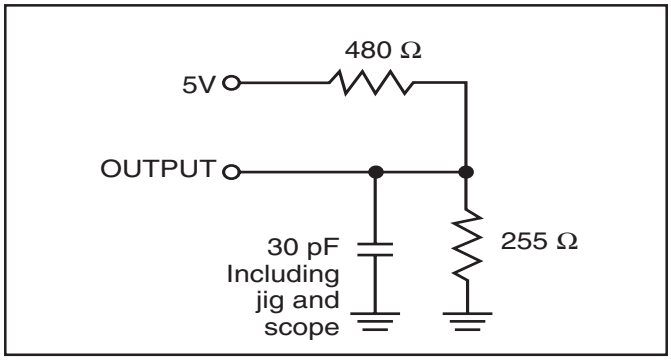


Figure 1

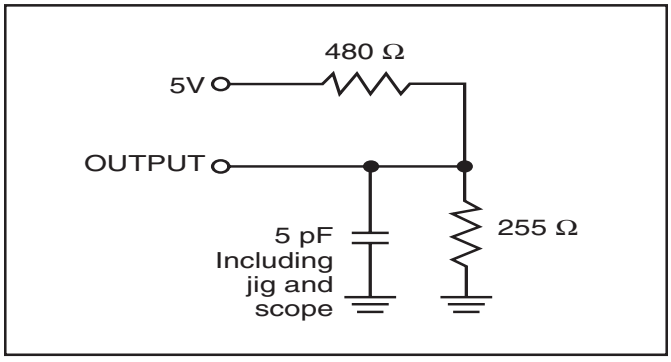
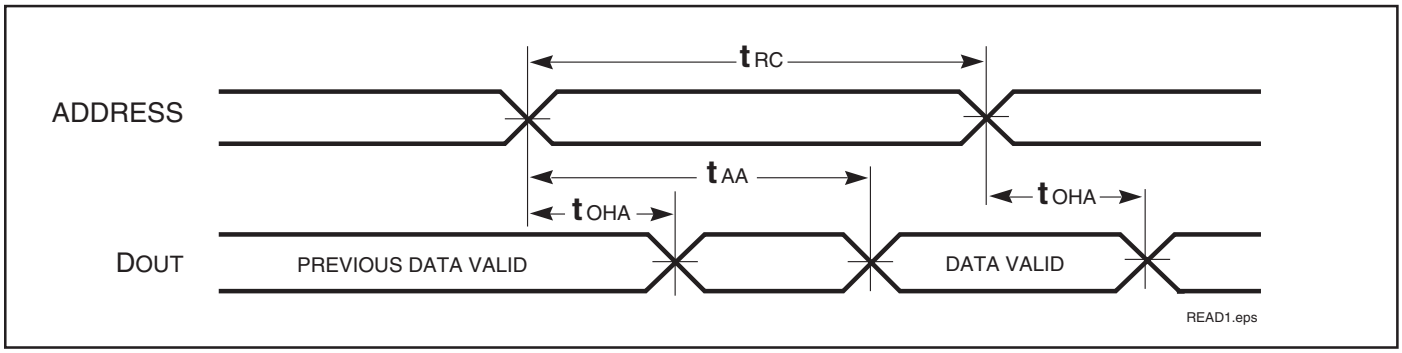
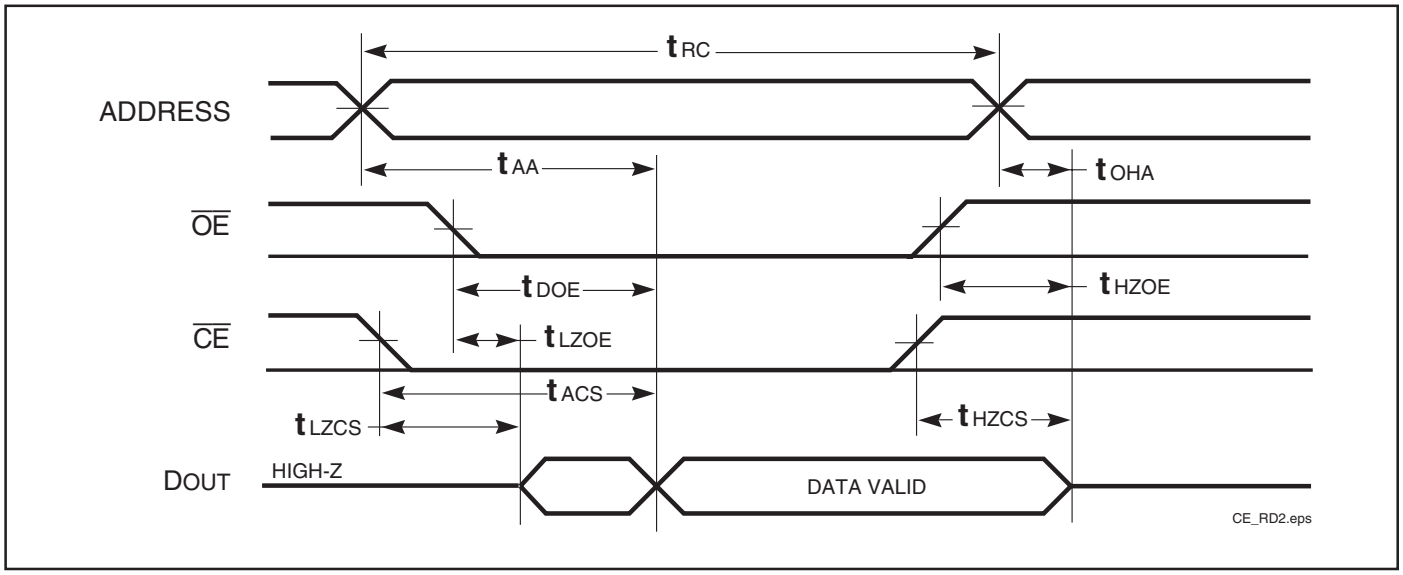


Figure 2

AC WAVEFORMS
READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



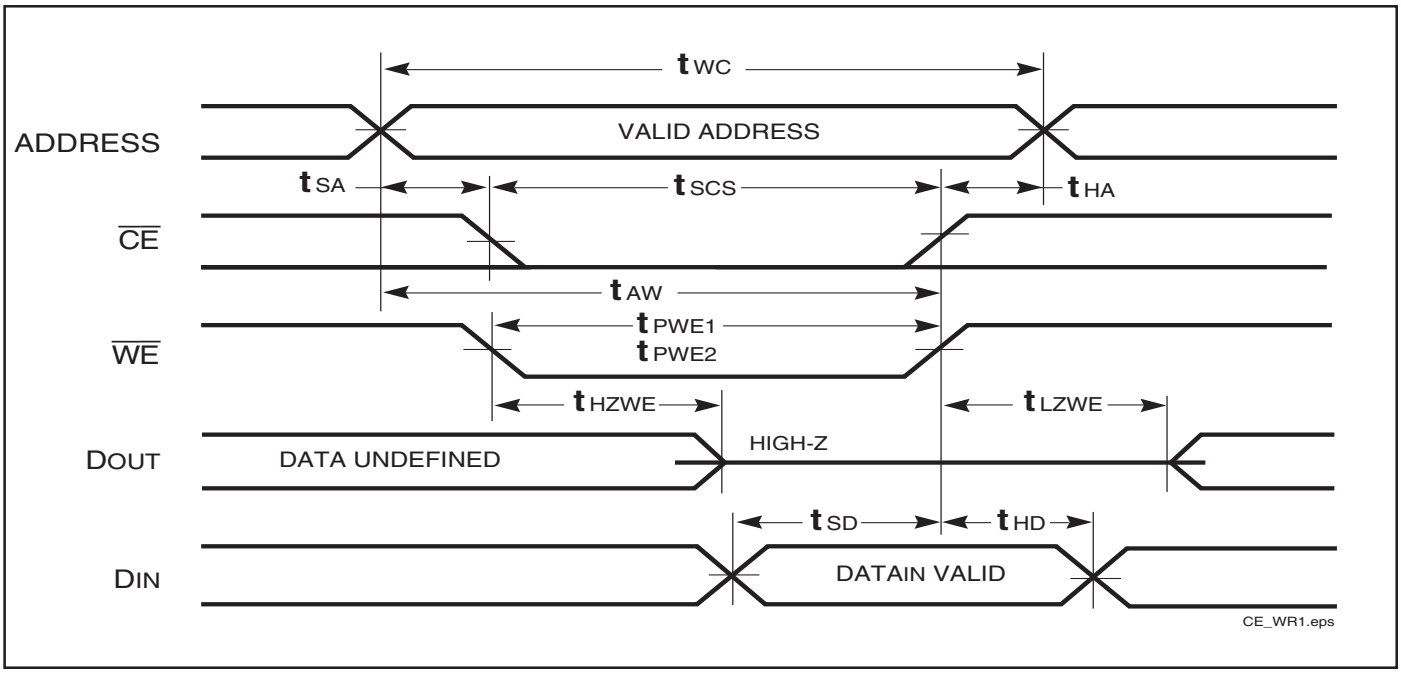
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

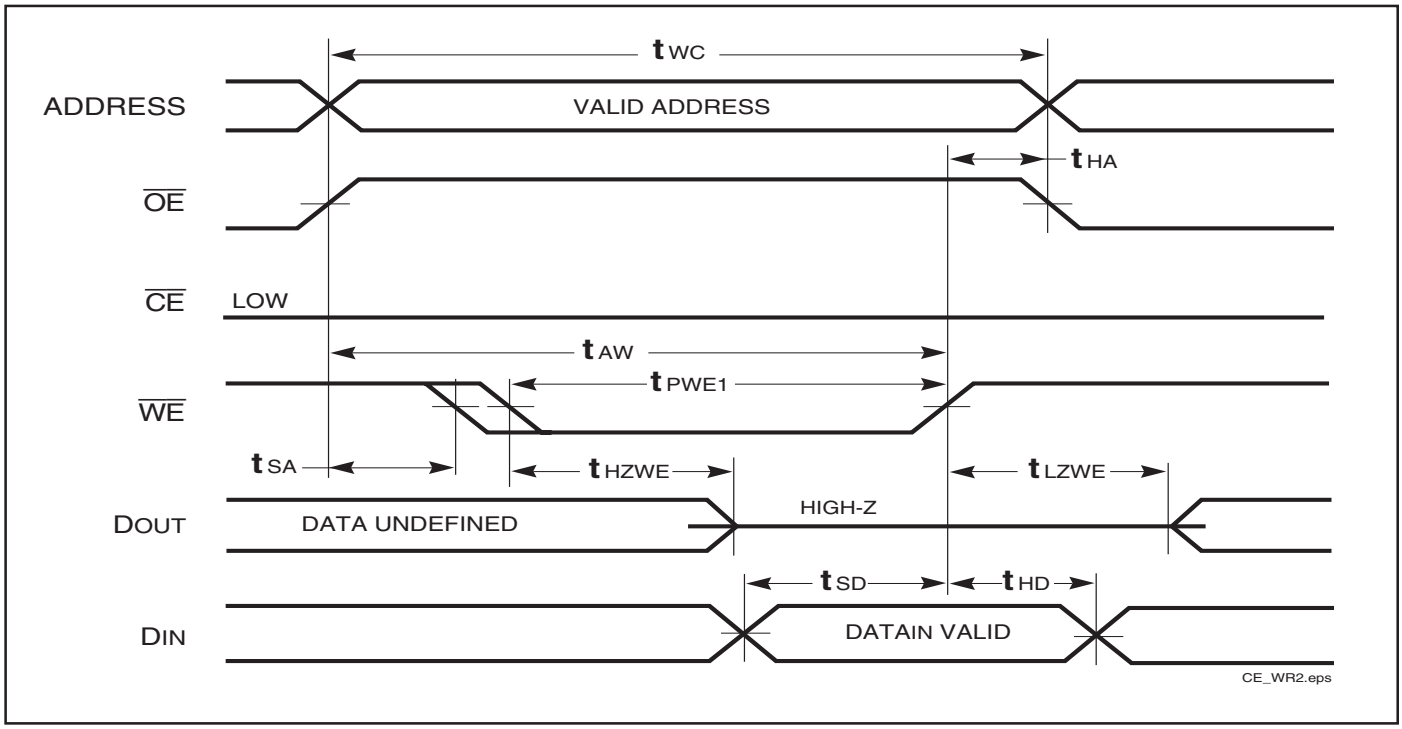
Symbol	Parameter	-10 ns Min.	-10 ns Max	-12 ns Min.	-12 ns Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{SCS}	$\overline{CE}$ to Write End	9	—	10	—	ns
t_{AW}	Address Setup Time to Write End	9	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ LOW)	9	—	9	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ HIGH)	8	—	8	—	ns
t_{SD}	Data Setup to Write End	7	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

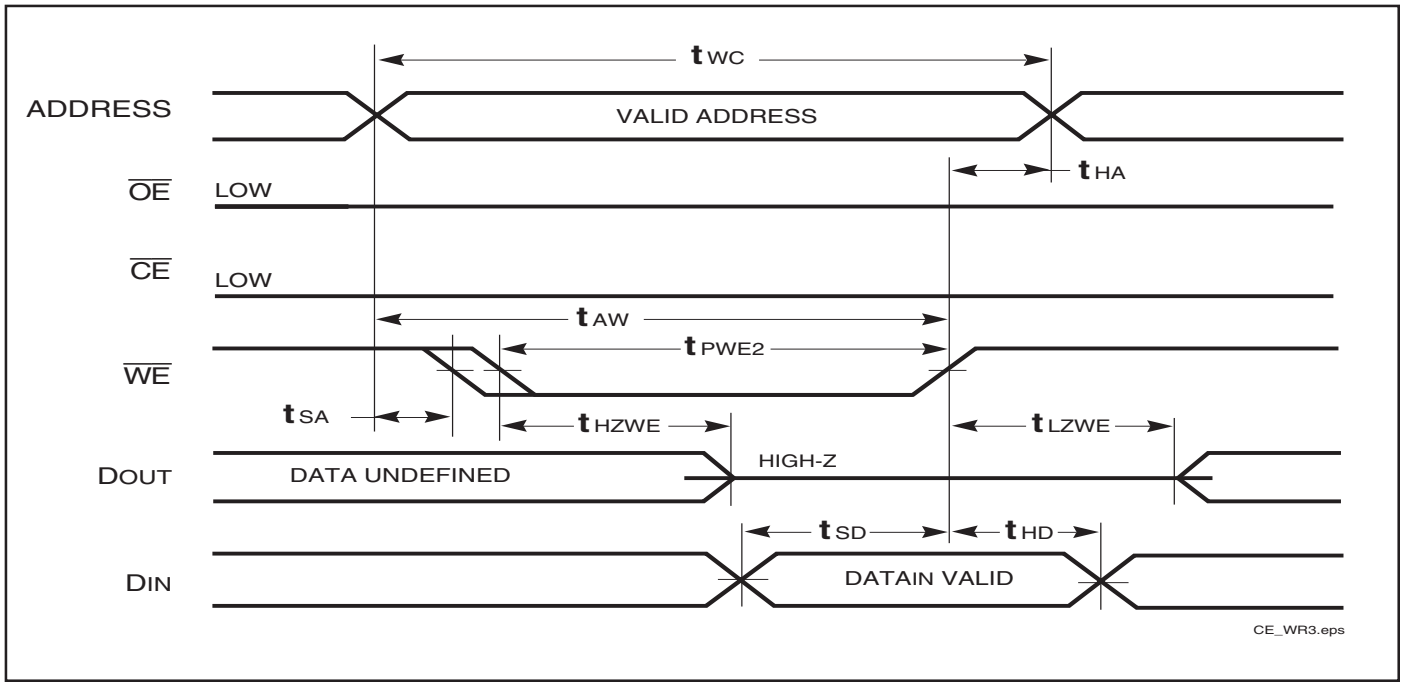
AC WAVEFORMS
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

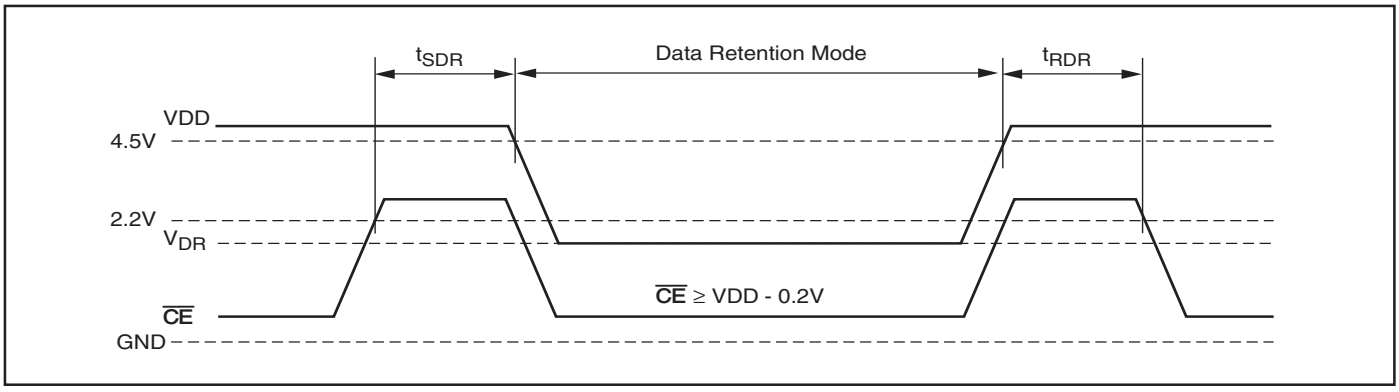
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	50	90	µA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—		100	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:
1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



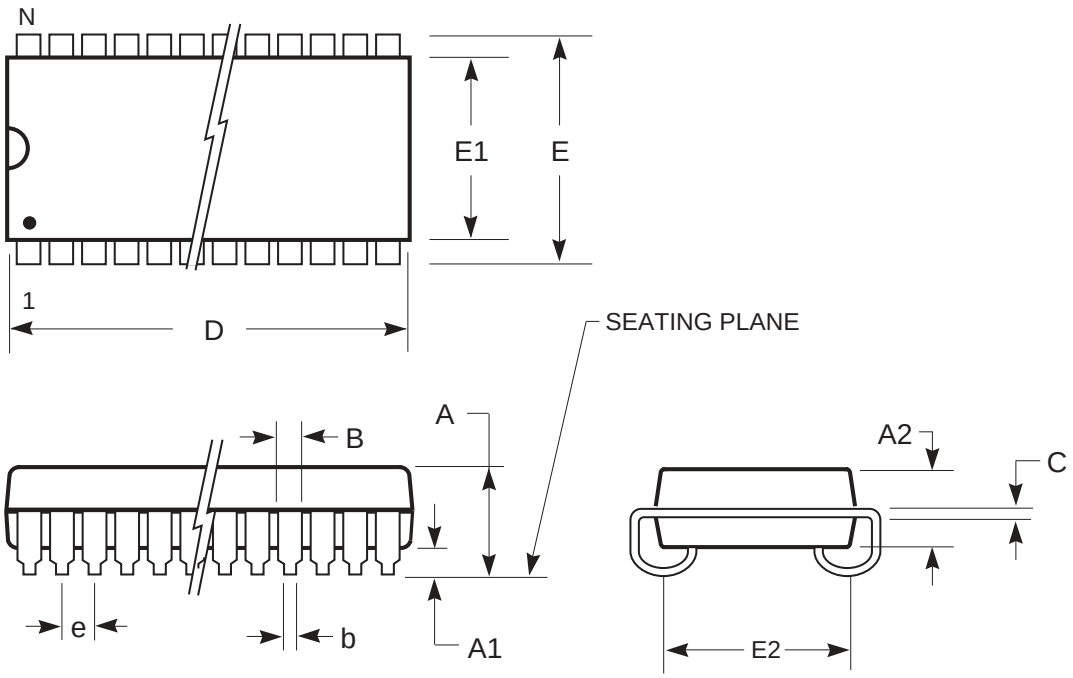
ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61C64AL-10JI	300-mil Plastic SOJ
	IS61C64AL-10JLI	300-mil Plastic SOJ, Lead-free
	IS61C64AL-10TI	Plastic TSOP
	IS61C64AL-10TLI	Plastic TSOP, Lead-free

PACKAGING INFORMATION

300-mil Plastic SOJ
Package Code: J



	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**24/26**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	17.02	—	17.27	0.670	—	0.680
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e	1.27 BSC			0.050 BSC		

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

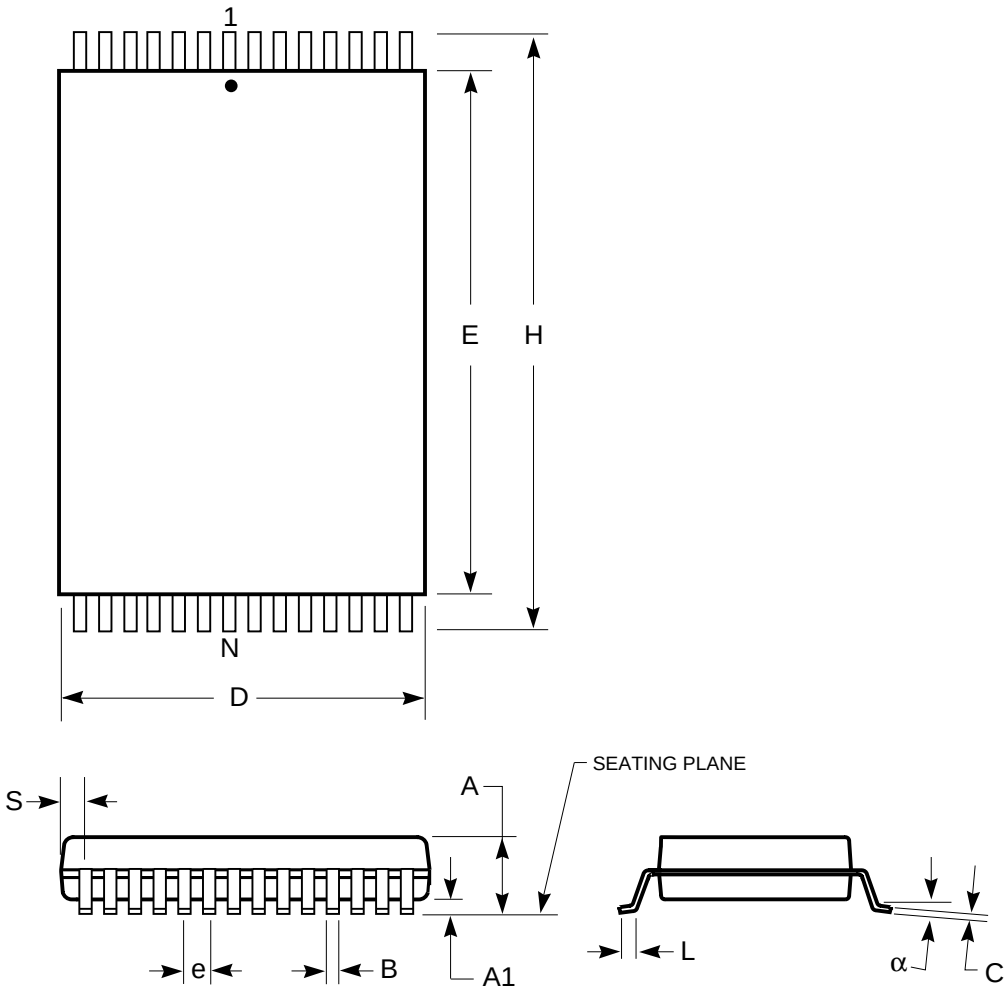
ISSI®

300-mil Plastic SOJ
Package Code: J

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**28**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	18.29	—	18.54	0.720	—	0.730
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e	1.27 BSC			0.050 BSC		

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**32**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	20.83	—	21.08	0.820	—	0.830
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e	1.27 BSC			0.050 BSC		

Plastic TSOP - 28-pins
Package Code: T (Type I)



Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		28		
A	1.00	1.20	0.037	0.047
A1	0.05	0.20	0.002	0.008
B	0.16	0.27	0.006	0.011
C	0.10	0.20	0.004	0.008
D	7.90	8.10	0.308	0.316
E	11.70	11.90	0.456	0.465
H	13.20	13.60	0.515	0.531
e	0.55 BSC		0.022 BSC	
L	0.30	0.70	0.011	0.027
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.