Lead-free Green

A product Line of
Diodes Incorporated

PI3DPX1205A

DP-Alt DP1.4/USB3.1 10Gbps Type-C Linear ReDriver Mux with Latency-free and built-in Aux/SBU Mux

Description

PI3DPX1205A is the DP-Alt 1.4 (Max 10Gbps) 6:4 Active Mux Linear Redriver supporting DP Link-Training Transparent for Source-side application. The device is compliant to the VESA DP Alt 1.4 and USB 3.1 Gen 2 industry standard.

Each of the DP1.4 and USB3.1 Gen2 differential signals can be easily adjustable with equalization, output swing and gain values by the I2C control setting. It can optimize the DP/USB 10Gbps signal performance over a variety of physical mediums by reducing Inter-symbol interference jitters.

Non-blocking Linear Redriver provides 2x better additive jitter performance than the other conventional CMOS ReDriver. Linear Equalization does not block the Receiver DFE's adaptive channel controls, supporting DisplayPort Transparent LT(Link Training).

This non-blocking linear redriver is named as "Trace Loss Cancel-ing" technology, and supports the cascading connections between Host and Device high speed link. It means multiple Linear Redriver can be placed any locations to work seamlessly to compensate high insertion loss

Features

- Flexible DP 1.4 / USB 3.1 Gen 2 Type-C switching for DP-Alt Output
- Latency-free DisplayPort redriver for variable video frame rate control
- DP1.4 (8.1 Gbps) and USB3.1 Gen 2 (10 Gbps) standard compliant
- Receiver equalization, Flat gain, -1dB compression Output swing for each DP/USB mode.
- Non-blocking No-latency Linear Re-Driving with transparent DisplayPort Link Training support
- Doubled signal integrity performance than CMOS-based ReDriver
- Built-in control logic for Type-C plug/unplug normal and flipping orientations with I2C programming mode
- Slave I2C mode speed up to 1MHz
- Single Power Supply : 3.3V
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

  https://www.diodes.com/quality/product-definitions/

Applications

- Notebook, Desktop, AIO PCs
- Tablets and Mobile devices
- Docking, Embedded systems

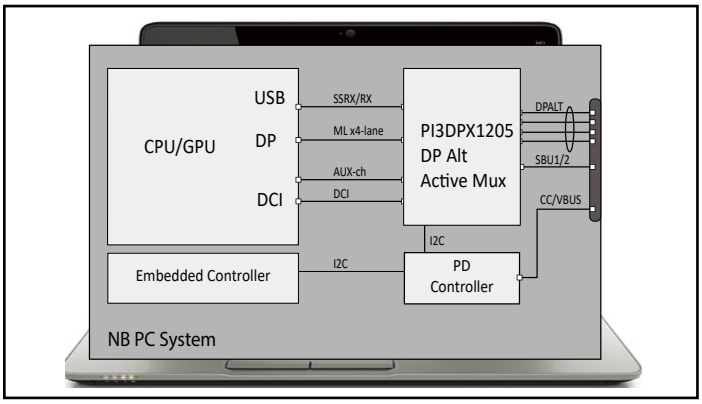


Figure 1-1 NB PC Application Diagram

Ordering Information

Ordering Number	Package Code	Package Description
PI3DPX1205AZLBEX	ZLB	40-Contact, Very Quad Flat No-Lead (TQFN) (4x6mm)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

2. General Information

2.1 Revision History

Date	Revision	Description of Changes
July 2016	–	Preliminary Datasheet release
Aug 2016	–	Ch3: Low power mode, ePad Via, DCI information, AC-cap recommendation added
Nov 2016	–	Ch5: AC/DC electrical parameters and output eye waveforms added
Dec 2016	–	Ch4: Max power numbers added Ch5: Programming guide, 10Gbps PCB routing, DP CTS and Interoperability report added ES sample errata (no known issues) removed
Feb 2017	–	Ch4. Additional parameters/values in the Electrical char tables added
May 2017	–	Ch3: 4-bit EQ and FG setting change for high speed Eye signal optimization. Related register spec updated Ch5: DP / USB3 compliance report added
Jun 2017	–	Application schematic updated for AuxPN and AuxSBU1/2 connection. Redriver Jitter performance comparison table added. Aux listener features removed. I_{PD} power down current increased to 100uA from 66uA
Sep 2017	–	4.28 BYTE 9-11 read only registers changed as reserved.
Nov 2017	1	All TX 4kΩ impedance changed from 4kΩ to 4.5kΩ (p2, p8, p9, p14). Replace reference schematic Rx capacitor circuit with 3.3uF and 220kΩ pull-down resistor (p35, p48)
Sept 2018	2	Updated Features Updated Section 3-2 Pin Description Updated Figure 3-1 Pin-out Updated Figure 6-13 Application Reference Schematic Deleted Section 1.2 Similar Products Comparison Deleted Section 1.3 Related Products Deleted Section 6.7 Channel Output Signal measurement vs. EQ/FG/SW Setting
Nov 2019	3	Updated Section 3.2 Pin Description Updated Section 5.1 Absolute Maximum Rating
May 2020	4	Not Recommended

Contents

3. Pin Configuration

3.1 Package Pin-out (Top View)

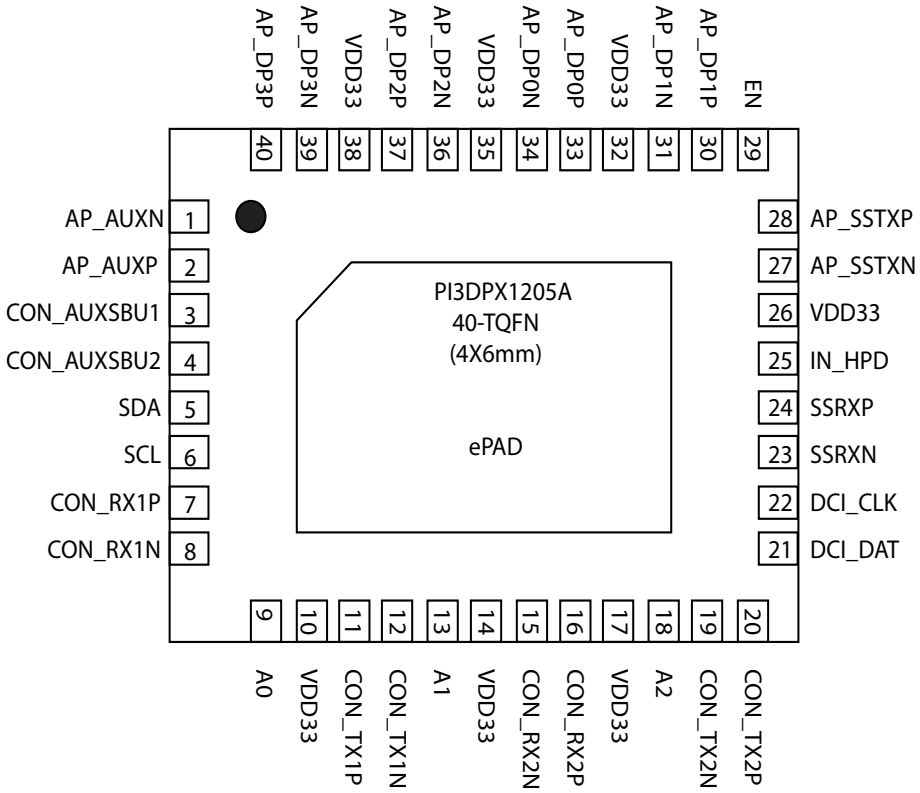


Figure 3-1. PI3DPX1205A pin-out

3.2 Pin Description

Pin Name	Pin No	IO	Description
AP_DP1P/N AP_DP0P/N AP_DP2P/N AP_DP3P/N	30, 31 33, 34 37, 36 40, 39	I	DisplayPort Main Link Input channels
AP_AUXP/N	2, 1	IO	Host AP/UFP-side DisplayPort Aux Channel, connected to Source
AP_SSTXP/N	28, 27	I	Super-Speed USB 3.1 Receiver channel
AP_SSRXP/N	24, 23	O	Super-Speed USB 3.1 Transmitter channel
CON_RX1P/N CON_RX2P/N	7, 8 16, 15	IO	Type-C receptacle RX/TX channel CML input/output With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VBiasTx, or Hi-Z
CON_TX1P/N CON_TX2P/N	11, 12 20, 19	O	CML output With selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VBiasTx, or Hi-Z
CON_AUXSBU1 CON_AUXSBU2	3, 4	IO	Down-Face-Port(DFP) Low Speed Signal Port. This port is off when IN_HPD pin input is Low for power saving. User can use I2C register bit control to always activate the port for application needed.
EN	29	I	Chip Enable. With internal 300kΩ pull-up resistor. “Low”: Chip Power Down “High”: Normal Operation (Default)
A0	9	I	I2C address select. 2-level input pins. Internal 300kΩ pull-down resistor.
A1	13	I	The I2C address select. 2-level input pins. With internal 200kΩ pull-down resistor.
A2	18	I	The I2C address select. 2-level input pins. With internal 300kΩ pull-down resistor.
SDA	5	IO	SDA is I2C control bus data. Open drain structure.
SCL	6	I	SCL is I2C control clock. Open drain structure.
IN_HPD	25	I	Hot plug detection from Sink. With internal 300kΩ pull-down resistor.
DCI_CLK DCI_DAT	22, 21	O	DCI Interface Output
VDD33	10, 14, 17, 26, 32, 35, 38	P	3.3V Power Supply
GND	ePAD	G	Ground

4. Functional Description

4.1 Detail Features

- DisplayPort Alt 6:4 differential Active Mux Redriver
- Flexible DP Alt Type-C switching support for USB3.1 Gen2 10Gbps and DP 8.1Gbps.
- Ultra Low standby power with auto power saving for the DisplayPort and USB mode.
- Selectable adjustment of Receiver equalization, Flat gain and -1dB compression linear output swing.
- Built-in control logic for Type-C plug/unplug normal and flipping orientations.
- Active linear redriver for signal integrity
- Supported DCI VDD =3.3V only, and DCI speed covers 1MHz to 133MHz.
- Slave I2C only. Supported speed up to 1MHz.
- I2C I/O buffer supports the 1.8V/3.3V signal condition.
- IN_HPD could be selected as active high or active low by I2C mode (byte4 [1])
- Single power supply 3.3±0.3V
- Not support 5V tolerance for all pins.

DisplayPort 1.4

- DP LT-transparent through linear Redriver design
- Hot Plug Detect
- Not support the I2C_Over_AUX, HBR AUX

USB 3.1

- Selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND
- Selectable output termination between 50Ω to VbiasTx, 4.5KΩ to VbiasTx or Hi-Z with receiver termination detection
- Possible operation modes: PD, Unplug, Deep slumber mode, Slumber mode and Active mode.
- Receives and transmits the signal in Unplug, Deep slumber, Slumber mode and Active mode.
- Active mode means all channels are always ready to transmit. No Ton/Toff due to the signal detector in this mode.
- Slumber mode, Deep slumber mode and Unplug mode: The channel is partially/fully off due to the power saving. Signal detector is monitoring the input signal actively. If the input signal is detected, the channel will switch to the active mode. ON-time is operation mode selection dependent.

4.2 Functional Block Diagram

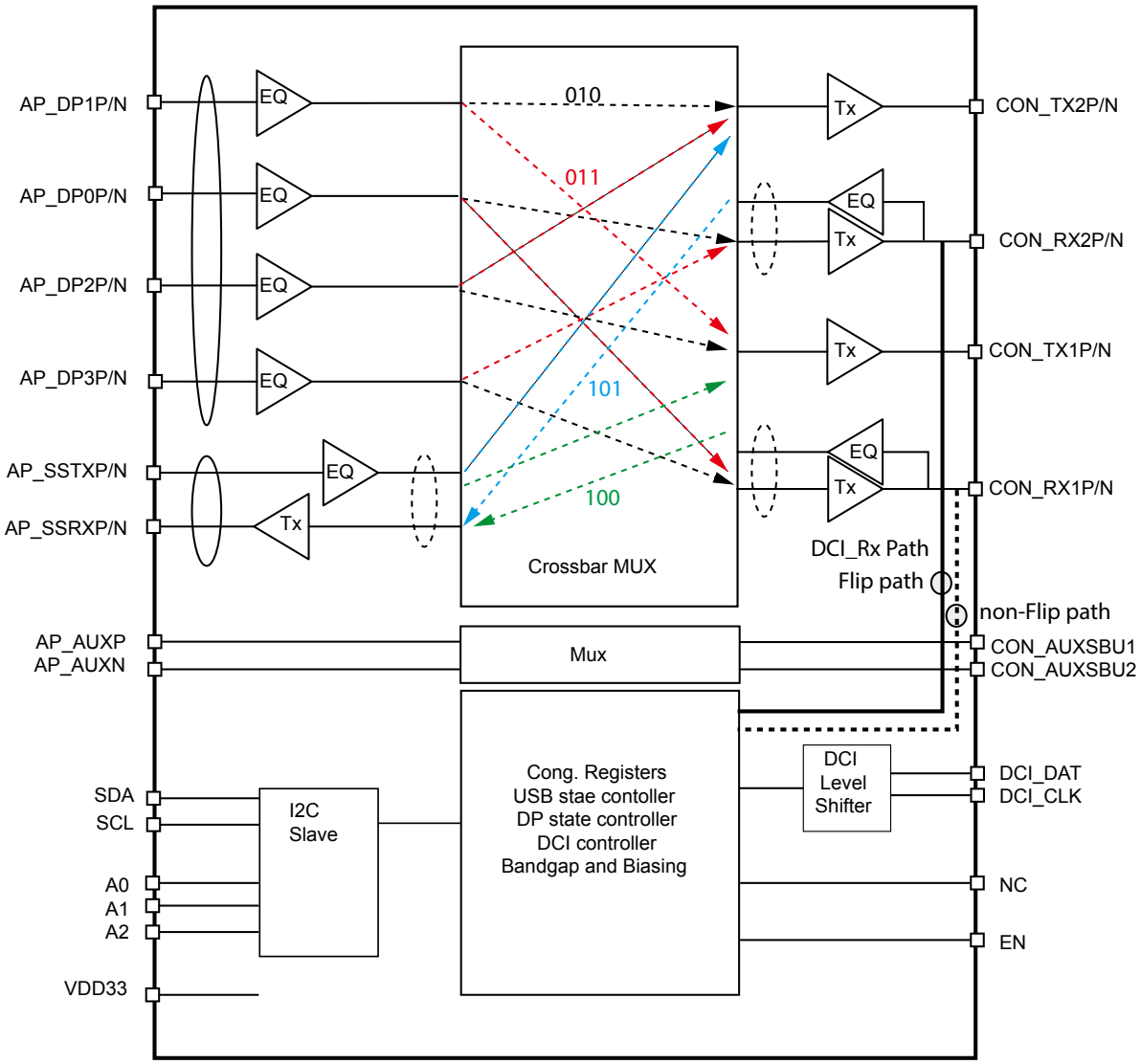


Figure 4-1 PI3DPX1205A DP-Alt Crossbar Active Mux ReDriver Block Diagram

4.3 Active Mux ReDriver mode setting

BYTE3 CONF<2:0> are the operating mode of selection bit, I2C 0x3[6:4]

Table 4-1. AP-side input to Connector-side output Switching map

BYTE3 0x3[6:4]	AP_ SSTX	AP_ SSRX	AP_ DP1	AP_ DP0	AP_ DP2	AP_ DP3	AP_ AUXP	AP_ AUXN	DCI	Response to IN_HPD/ AUX CMD	Mode Description
000	X	X	X	X	X	X	X	X	X	X	Safe Sate
001	X	X	X	X	X	X	X	X	X	X	Safe State
010	X	X	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	CON_ SBU1	CON_ SBU2	X	All channel response	4 lane DP1.4
011	X	X	CON_ TX1	CON_ RX1	CON_ TX2	CON_ RX2	CON_ SBU2	CON_ SBU1	X	All channel response	4 lane DP1.4 flipped
100	CON_ TX1	CON_ RX1	X	X	X	X	X	X	Between RX1 + SS	X	USB3.x
101	CON_ TX2	CON_ RX2	X	X	X	X	X	X	Between RX2 + SS	X	USB3.x flipped
110	CON_ TX1	CON_ RX1	CON_ TX2	CON_ RX2	X	X	CON_ SBU1	CON_ SBU2	Between RX1 + SS	TX2 & RX2 response	USB3+2lane DP1.4
111	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	X	X	CON_ SBU2	CON_ SBU1	Between RX2+ SS	TX1 & RX1 response	USB3+2lane DP1.4 flipped

4.3.1 IN_HPD control (I2C Byte DP_HPD_PIN_EN# 0x12[2])

Table 4-2. DP_HPD_PIN_EN# enable or disable the IN_HPD control

DP_HPD_PIN_EN#	IN_HPD	DP Channel
1	x	Enabled
0	0	Disabled
0	1	Enabled

4.3.2 IN_HPD assert and De-assert De-bounce timer

Table 4-3. IN_HPD De-bounce timer

IN_HPD transition	De-bounce timer timeout	Notes
Assert: Low -> High	~0s	
De-assert: High -> Low	~ 325ms typ	Any Low-> High transition within timeout will reset the timer.

4.4 EQ/FG/SW controls

Table 4-4. Equalization Setting

EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
0	0	0	0	3.2	3.8	4.9	5.7	6.1	I2C Default
0	0	0	1	3.5	4.2	5.5	6.4	6.9	
0	0	1	0	3.8	4.7	6.1	7.1	7.7	
0	0	1	1	4.2	5.1	6.6	7.7	8.4	
0	1	0	0	4.7	5.6	7.2	8.3	9	
0	1	0	1	5	6	7.7	8.9	9.6	
0	1	1	0	5.4	6.4	8.2	9.4	10.1	
0	1	1	1	5.7	6.8	8.6	9.9	10.6	
1	0	0	0	6.2	7.3	9	10.2	11	
1	0	0	1	6.5	7.6	9.4	10.7	11.4	
1	0	1	0	6.8	7.9	9.8	11.1	11.8	
1	0	1	1	7	8.2	10.1	11.4	12.1	
1	1	0	0	7.4	8.5	10.4	11.7	12.4	
1	1	0	1	7.6	8.8	10.7	12	12.7	
1	1	1	0	7.8	9.1	11	12.3	13	
1	1	1	1	8.1	9.3	11.3	12.6	13.3	

Table 4-5. Flat Gain Setting

FG[1:0]	Flat Gain Settings V/V
00	-1.5 dB
01	0 dB (Default)
10	+1 dB
11	+2.5 dB

Table 4-6. Output -1 dB Compression Swing Setting (I2C mode: 0x5[1:0] to 0x8[1:0])

CONx_SW[1:0]	Output Linear Swing Settings
00	900mVppd
01	1000mVppd
10	1100mVppd
11	1200mVppd (Default)

Table 4-7. EN is the channel enable pin

EN	Channel Enable Setting
0	Disabled
1	Enabled (Default)

4.5 USB mode

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If load is detected, it will return to Low Power Mode and receiver detection will be active again per 6ms.

Table 4-8. The I/O termination resistance under different conditions

Symbol	Parameter	Resistance	Units
RX terminal			
Rin-pd	Input resistance at power down mode	67k to GND	Ω
Rin-U0	Input resistance at U0 condition	50 to VDD	Ω
Rin-U1	Input resistance inU1 (1)	50 to VDD	Ω
Rin-U2/U3	Input resistance in U2/U3 (1)	50 to VDD	Ω
Rin-RXDet	Input resistance in RXDET (1)	67k to VbiasRx	Ω
TX terminal			
Rout-pd	Output resistance at power down mode	HIZ	Ω
Rout-U0	Output resistance at U0 condition	50 to VbiasTx1	Ω
Rout-U1	Output resistance in U1 mode (1)	4.5k to VbiadTx1	Ω
Rout-U2/U3	Output resistance in U2/U3 mode (1)	4.5k to VbiasTx2	Ω
Rout-RXDet	Output resistance in RXDET mode (1)	4.5k to VbiasTx2	Ω

Notes: (1) The value of Rin-RxDet will be updated only after the receiver evaluation has been done. Thus, the value can be 50Ω or 67kΩ pull-low.

4.6 DisplayPort mode

By default, all channels will go to active modes if IN_HPD = 1. The ON/OFF of each DP channel is controlled by the Aux lane count and D3 command.

4.6.1 DisplayPort Main Link

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DPTX drives doubly terminated, AC-coupled differential pairs, as shown in Figure 3-34 in a manner compliant with the Main-Link Transmitter electrical specification.

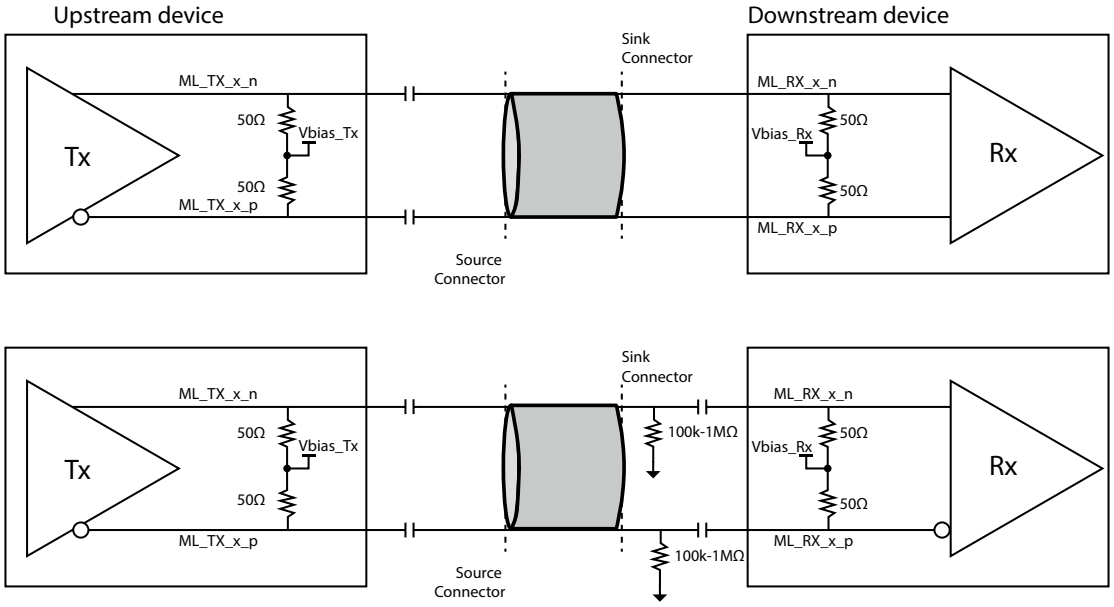


Figure 4-2 DisplayPort Main Link Connection Diagram

DP Low Power Mode Description

PM_State	Mode	Description
1	Active mode	Data transfer (normal operation); The AUX monitor is actively monitoring for Link Training unless it is disabled through I2C interface. At power-up all Main Link outputs are Enabled by default. AUX Link Training is necessary to overwrite the DPCD registers to Enable/Disable Main Link outputs.
2	Standby mode	Low power consumption (I2C interface is active; AUX monitor is inactive); Main Link outputs are disabled; the Sink device has de-asserted HPD
3	D3 power saving mode (Sleep)	Low power consumption(I2C interface is active; AUX monitor active); Main Link outputs are disabled; The Sink device has asserted HPD, and sufficiently enabled the AUX CH to at least monitor incoming AUX CH differential signals. The Main-Link RX disabled.
4	Power down mode(OFF)	Lowest power consumption (EN = 0); all outputs are high-impedance; I2C interface is turned off, all inputs are ignored, I2C register is reset and AUX DPCD is reset:

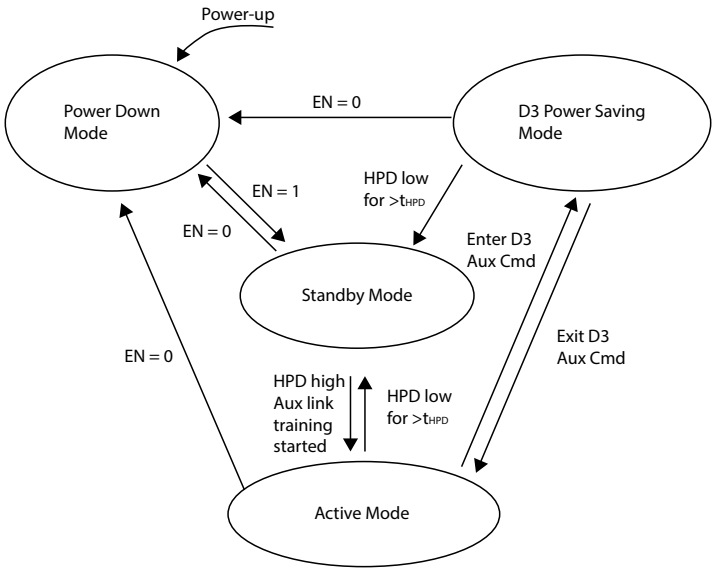


Figure 4-3 DisplayPort Operation mode

4.6.2 DisplayPort Aux Channel

The AUX CH of DP is a half-duplex, bidirectional channel. The DP device with DPTX such as a Source device is the master of the AUX CH (called AUX CH Requester), while the device with DPRX such as a Sink device is the slave (AUX CH Replier). As the master, the Source device must initiate a Request Transaction, to which the Sink device responds with a Reply Transaction.

The system design of a DFP_D on a USB Type-C connector connected to a UFP_D on a USB Type-C connector using a USB Type-C to USB Type-C Cable. The 2MΩ pull-down resistors on SBU1 and SBU2 are representative of the leakage of ESD and EMI/RFI components including termination to ensure no floating nodes, and are intended to show compliance with SBU Termination in USB Type-C r1.1. The plug orientation switch may be replaced by AUX polarity inversion logic in the DisplayPort transmitter or receiver, controlled by the plug orientation detection mechanism associated with the USB Type-C Receptacle.

Note: The 3.3V levels in the Adapters are derived from VCONN because not all DisplayPort UFP_D devices provide DP_PWR.

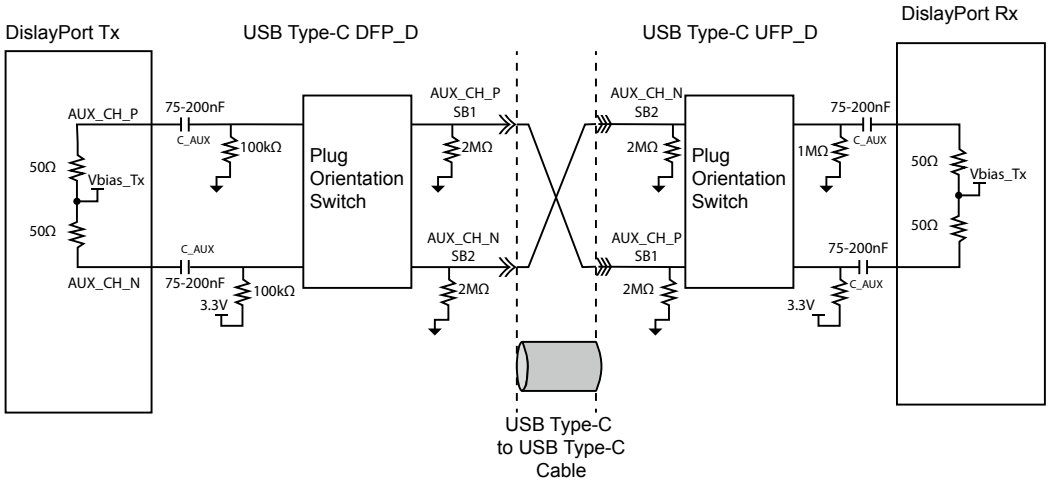


Figure 4-4 AUX Signaling Using USB Type-C to USB Type-C Cables

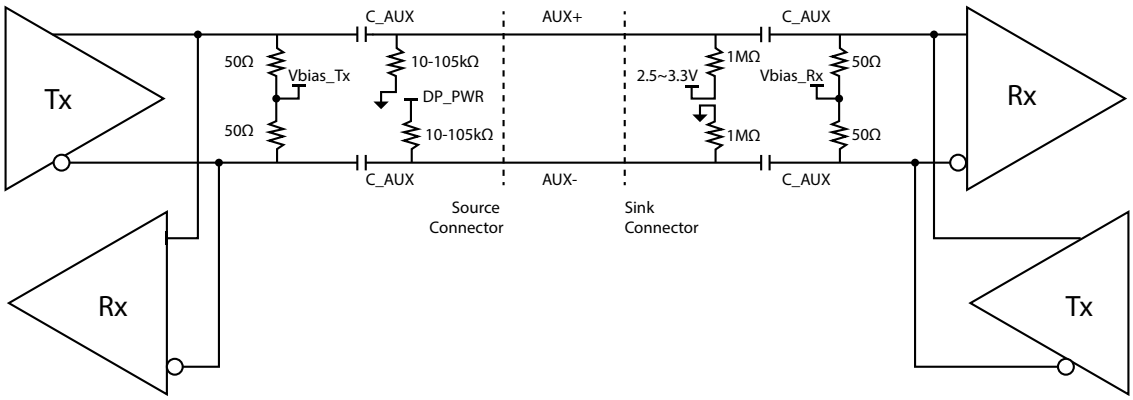


Figure 4-5 DisplayPort Aux Channel Connection

4.7 DCI (Direct Connect Interface)

DCI (also Referred to ExI for Embedded DFx Interface) is an Intel proprietary debugging interface for closed chassis debugging. The DCI data path overlays on the Type C active switch SS port, with the input data overlaid on the SSRx pair (SSRXP -> DCI_DAT, SSRXN -> DCI_CLK) and the output data path overlaid on the SSTx pair.

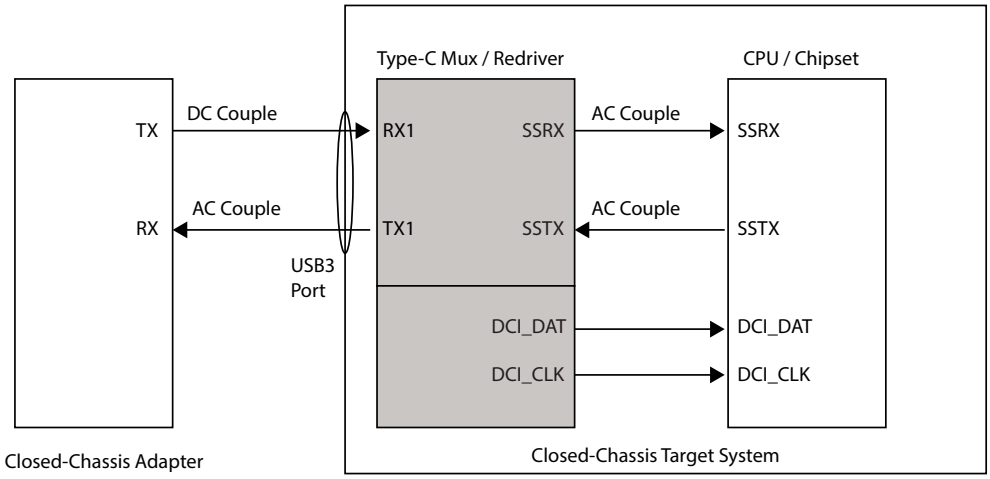


Figure 4-6 CCA to Target System Interconnect through a Type C Repeater

4.8 I2C Programming Sequence

4.8.1 I2C Address

	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Slave address (First byte is slave address)	1	0	1	0	A2	A1	A0	0/1 (W/R)

Note:
(1) A0, A1, A2 are pin-strapping selectable

4.8.2 I2C Operation

- I2C interface operates as a slave device.
- The device supports Bulk read/write
- Support operating speed up to 1MHz
- Supported 7-bit addressing
- The data byte format is 8-bit bytes with the most significant bit (MSB) first.
- Will never hold the clock line SCL LOW to force the master into a wait state.
- No response when the data on common bus is matched to the device address.
- If I2C master want read/write invalid register, i.e. the I2C slave just write/read from a dummy RO register with FF by default.

4.8.3 Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

4.8.4 Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first. It will never hold the clock line SCL LOW to force the master into a wait state.

4.8.5 Start & Stop Condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below

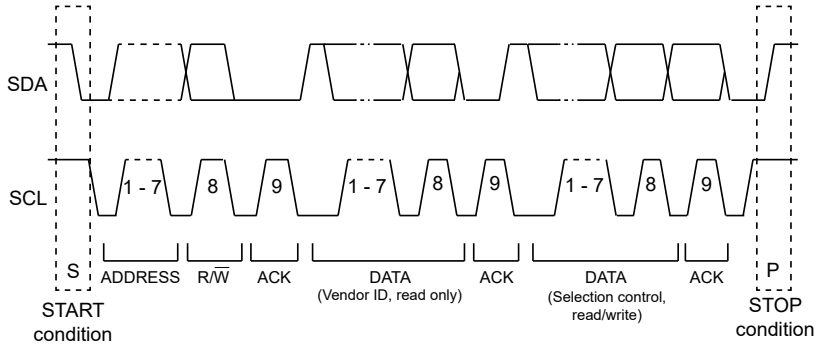


Figure 4-7 I2C Start and STOP Condition

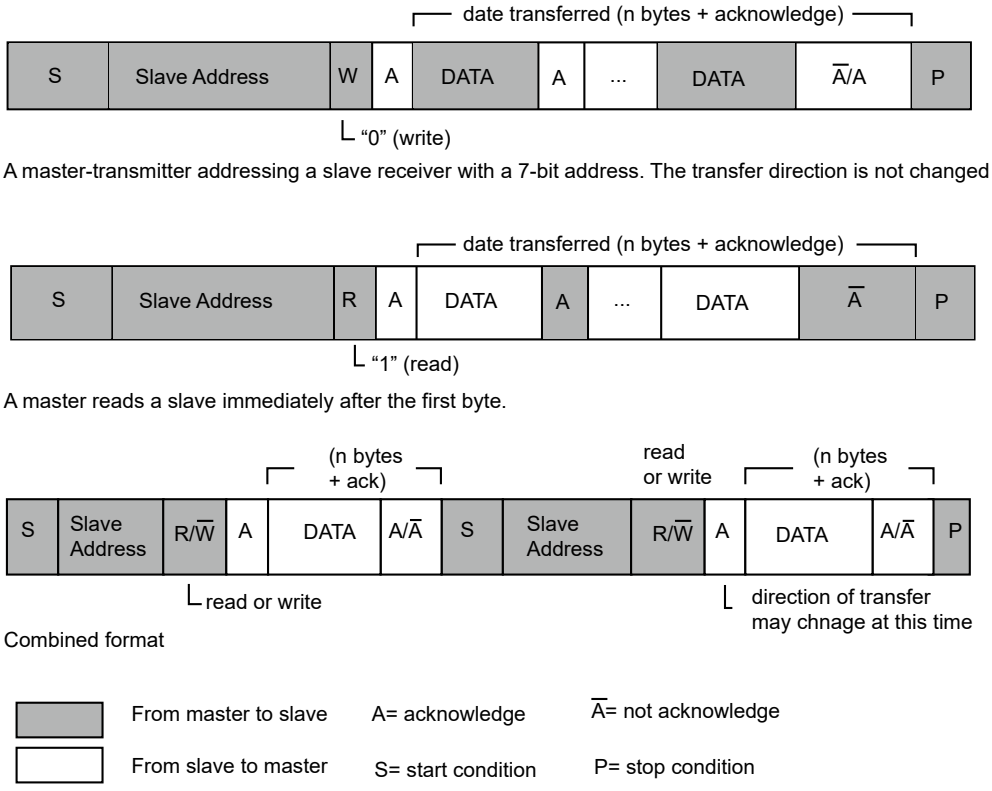


Figure 4-8 Bulk Read/write Protocol

4.9 Detail Programming Registers

4.9.1 Register Map

Byte	Read after power up	
0	03h	Revision and Vendor ID Register
1	11h	Device Type / Device ID register
2	20h	Byte count register
3	00h	Byte count register 32 Bytes
4	0Dh	Override the power down control
5	03h	Equalization, Flat gain, and -1dB linear Swing setting of CON_RX2
6	03h	Equalization, Flat gain and -1dB linear Swing setting of CON_TX2
7	03h	Equalization, Flat gain and -1dB linear Swing setting of CON_TX1
8	03h	Equalization, Flat gain and -1dB linear Swing setting of CON_RX1
9	60h	Path selection and flip control
10	FCh	Feature control of the CON_RX2 and CON_TX
11	FCh	Feature control of the CON2 and CON3
12	58h	Threshold, feature Enable/Disable and timing setting
13	00h	Reserved
14	FFh	
15	C8h	
16	DCh	
17	14h	
18	04h	
19 ~30	00h	
31	01h	

4.9.2 BYTE 0 (Revision and Vendor ID Register)

Bit	Type	Default	Control affected	Comment
7	RO	0	Revision ID	Rev# = 0000
6	RO	0		
5	RO	0		
4	RO	0		
3	RO	0	Vendor ID	Pericom
2	RO	0		
1	RO	1		
0	RO	1		

4.9.3 BYTE 1 (Device Type/Device ID register)

Bit	Type	Default	Control affected	Comment
7	RO	0	Device Type	Device Type Active Mux = 0001
6	RO	0		
5	RO	0		
4	RO	1		
3	RO	0	Device ID	Device ID PI3DPX1205 = 0001
2	RO	0		
1	RO	0		
0	RO	1		

4.9.4 BYTE 2 (Byte count register)

Bit	Type	Default	Control affected	Comment
7	RO	0	Register Byte count	I2C byte count = 32 bytes
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0		
2	RO	0		
1	RO	0		
0	RO	0		

4.9.5 BYTE 3 (Byte count Register 32 bytes)

Bit	Type	Default	Control affected	Comment
7	R/W	0	Reserved	
6	R/W	0	CONF<2>	Preset assignment for the Preset Application Mode
5	R/W	0	CONF<1>	
4	R/W	0	CONF<0>	
3	R/W	0	Reserved	
2	R/W	0	PIN_RXDET_EN#	Far end Receiver termination detection Enable (Active Low) 0 - Detection is enabled. 1 - Detection is disabled.
1:0	R/W	0		Reserved

4.9.6 BYTE 4 (Override the power down control)

Bit	Type	Default	Control affected	Comment
7	R/W	0	PD_CON_RX1	Channel power down override 0- Normal operation 1 – Force the channel to power down state
6	R/W	0	PD_CON_TX1	
5	R/W	0	PD_CON_TX2	
4	R/W	0	PD_CON_RX2	
3	R/W	1	Reserved	
2	R/W	1	Reserved	
1	R/W	0	IN_HPD_ActiveHigh_EN#	0 - IN_HPD Active High 1 - IN_HPD Active Low
0	R/W	1	Reserved	

4.9.7 BYTE 5 (Equalization, Flat gain and -1dB linear Swing setting of CON_RX2)

Bit	Type	Default	Control affected	Comment
7	R/W	0	RX2_EQ<3>	RX2 setting configuration Equalizer Flat gain Swing
6	R/W	0	RX2_EQ<2>	
5	R/W	0	RX2_EQ<1>	
4	R/W	0	RX2_EQ<0>	
3	R/W	0	RX2_FG<1>	
2	R/W	1	RX2_FG<0>	
1	R/W	1	RX2_SW<1>	
0	R/W	1	RX2_SW<0>	

4.9.8 BYTE 6 (Equalization, Flat gain and -1dB linear Swing setting of CON_TX2)

Bit	Type	Default	Control affected	Comment
7	R/W	0	CON_TX2_EQ<3>	CON_TX2 setting configuration Equalizer Flat gain Swing
6	R/W	0	CON_TX2_EQ<2>	
5	R/W	0	CON_TX2_EQ<1>	
4	R/W	0	CON_TX2_EQ<0>	
3	R/W	0	CON_TX2_FG<1>	
2	R/W	1	CON_TX2_FG<0>	
1	R/W	1	CON_TX2_SW<1>	
0	R/W	1	CON_TX2_SW<0>	

4.9.9 BYTE 7 (Equalization, Flat gain and -1dB linear Swing setting of CON_TX1)

Bit	Type	Default	Control affected	Comment
7	R/W	0	CON_TX1_EQ<3>	CON_TX1 setting configuration Equalizer Flat gain Swing
6	R/W	0	CON_TX1_EQ<2>	
5	R/W	0	CON_TX1_EQ<1>	
4	R/W	0	CON_TX12_EQ<0>	
3	R/W	0	CON_TX1_FG<1>	
2	R/W	1	CON_TX1_FG<0>	
1	R/W	1	CON_TX1_SW<1>	
0	R/W	1	CON_TX1_SW<0>	

4.9.10 BYTE 8 (Equalization, Flat gain and -1dB linear Swing setting of CON_RX1)

Bit	Type	Default	Control affected	Comment
7	R/W	0	CON_RX1_EQ<3>	CON_RX1 setting configuration Equalizer Flat gain Swing
6	R/W	0	CON_RX1_EQ<2>	
5	R/W	0	CON_RX1_EQ<1>	
4	R/W	0	CON_RX1_EQ<0>	
3	R/W	0	CON_RX1_FG<1>	
2	R/W	1	CON_RX1_FG<0>	
1	R/W	1	CON_RX1_SW<1>	
0	R/W	1	CON_RX1_SW<0>	

4.9.11 BYTE 9-11 (Reserved)

4.9.12 BYTE 12 (Threshold, feature Enable/Disable and timing setting)

Bit	Type	Power up condition	Control affected	Comment
7	R/W	0	IDET_VTH<1>	High Speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd 11 95mVppd
6	R/W	1	IDET_VTH<0>	
5	R/W	0	Reserved	
4	R/W	1	Reserved	
3	R/W	1	Reserved	
2	R/W	0	DP_HPD_PIN_EN#	Enable the IN_HPD Pin, so the redriver will response to this pin. 0 – Enabled 1 – Disabled
1	R/W	0	AUX _EN#	Enable/Disable the AUX listener. 0 – Enabled 1 – Disabled
0	R/W	0	Reserved	

4.9.13 BYTE 13 - 31 : Reserved

5. Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential.....–0.5 V to +3.8 V
DC SIG Voltage..... –0.5 V to V_{DD} + 0.5 V
CML Continuous Input Current.....+30 to +30mA
Storage Temperature .....–65 °C to +150 °C
Max junction temperature.....125°C
ESD HBM.....±2kV
ESD CDM.....±500V

Note:
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect in operability and degradation of device reliability and performance.

5.2 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max	Units
V_{DD}	VDD Supply Voltage	3.0	3.3	3.6	V
V_{DD_I2C}	VDD I2C Supply Voltage			3.6	V
V_{NOISE}	Supply Noise up to 50 MHz(1)		100		mVpp
T_A	Commercial Temperature Ambient range (C-temp part)	0		70	°C

Notes:
(1) Allowed supply noise (mVpp sign wave) under typical condition

5.3 Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{PD}	Typical Pin Power Down current, VDD=3.3V	EN = 0		26	100	µA
I_{DDQ_PD}	I2C Power Down current, VDD=3.3V	EN=1 I2C Byte4<7:4>=1111		112	340	µA
DP1.4 Mode						
I_{DD_DP}	Power supply current in DP mode EN =1, VDD=3.3V	1-lane DP		33	55	mA
		2-lane DP		66	110	mA
		4-lane DP		132	210	mA
USB 3.1 Gen2 Mode						
I_{U0}	Current in USB U0 mode, VDD=3.3V	EN=1, USB U0 mode		80	112	mA
I_{U1}	Current in USB U1 mode, VDD=3.3V	EN=1, USB U1 mode		16	20	mA
$I_{U2/U3}$	Current in USB U2/U3 modes. VDD=3.3V	EN=1, USB U2/U3 mode		0.5	0.6	mA
I_{RXDET}	Current in USB RXDET mode, VDD=3.3V	EN=1, USB RXDET mode		0.5	0.6	mA

5.4 AC/DC Characteristics

5.4.1 LVCMOS I/O DC Specifications

Symbol	Parameter	Min.	Typ.	Max	Units
2-level control pins					
V_{IH}	DC input logic High	V_{DD}*0.65			V
V_{IL}	DC input logic Low			V_{DD}*0.35	V
I_{IH}	Input High current			25	uA
I_{IL}	Input Low current	-25			uA

5.4.2 USB Differential Channel

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
USB differential Input						
$C_{RXPARASITIC}$	The parasitic capacitor for RX				1.0	pF
$R_{RX-DIFF-DC}$	DC Differential Input Impedance		72		120	Ω
$R_{RX-SINGLE\_DC}$	DC single ended input impedance	DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max	18		30	
$Z_{RX-HIZ-DC-PD}$	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25			kΩ
$C_{AC\_COUPLING}$	AC coupling capacitance		75		265	nF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{RX-CM-AC-P}$	Common mode peak voltage	AC up to 5GHz			150	mVpeak
$V_{RX-CM-DC-Active-Idle-Delta-P}$	Common mode peak voltage(1)	Between U0 and U1. AC up to 5GHz			200	mVpeak
USB differential Output						
$V_{TX-DIFF-PP}$	Ouput differential p-p voltage swing	Differential Swing $\|V_{TX-D+}-V_{TX-D-}\|$			1.2	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance		72		120	Ω
$V_{TX-RCV-DET}$	The amount of voltage change allowed during RxDet				600	mV
$C_{ac\_coupling}$	AC coupling capacitance		75		265	nF
$T_{TX-EYE(10Gbps)}$	Transmitter eye, Include all jittter	At the silicon pad. 10Gbps	0.646			UI
$T_{TX-EYE(5Gbps)}$	Transmitter eye, Include all jittter	At the silicon pad. 5Gbps	0.625			UI
$T_{TX-DJ-DD(10Gbps)}$	Transmitter deterministic jittter	At the silicon pad. 10Gbps			0.17	UI
$T_{TX-DJ-DD(5Gbps)}$	Transmitter deterministic jittter	At the silicon pad. 5Gbps			0.205	UI
$C_{TXPARASITIC}$	The parasitic capacitor for TX				1.1	pF
$R_{TX-DC-CM}$	Common mode DC output Impedance		18		30	Ω
$V_{TX-DC-CM}$	The instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	$\|V_{TX-D+}+V_{TX-D-}\|/2$	0		2.2	V
V_{TX-C}	Common-Mode Voltage	$\|V_{TX-D+}+V_{TX-D-}\|/2$	VDD-2V		VDD	V
$V_{TX-CM-AC-PP-Active}$	Active mode TX AC common mode voltage	$V_{TX-D+}+V_{TX-D-}$ for both time and amplitude			100	mVpp
$V_{TX-CM-DC-Active\_Idle-Delta}$	Common mode delta voltage $\|Avg_{uo}(\|V_{TEX-D+} + V_{TX-D-}\|)/2-Avg_{u1}(\|V_{TX-D+} + V_{TX-D-}\|)/2\|$	Between U0 to U1			200	mV-peak
$V_{TX-Idle-Diff-AC-pp}$	Idle mode AC common mode delta voltage$\|V_{TX-D+}-V_{TX-D-}\|$	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals .			10	mVppd
$V_{TX-Idle-Diff-DC}$	Idle mode DC common mode delta voltage$\|V_{TX-D+}-V_{TX-D-}\|$	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.			10	mV
G_p	Peaking gain (Compensation at 5GHz, relative to 100MHz, 100mV_{p-p} sine wave input)	EQ<3:0>=0000 EQ<3:0>=0101 EQ<3:0>=1010 EQ<3:0>=1111		5.7 8.9 11.1 12.6		dB
		Variation around typical	-3		+3	dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
G_F	Flat gain (100MHz, EQ<3:0>=0000, SW<1:0>=01)	FG<1:0>=00 FG<1:0>=01 FG<1:0>=10 FG<1:0>=11		-1.5 0 +1 +2.5		dB
		Variation around typical	-3		+3	dB
V_{SW_100M}	-1dB compression point output swing (at 100MHz)	SW<1:0>=00 SW<1:0>=01		900 1000		mVppd
V_{SW_5G}	-1dB compression point output swing (at 5GHz)	SW<1:0>=00 SW<1:0>=01		600 750		mVppd
DD_{NEXT}[Note3]	Differential near-end crosstalk	100MHz to 5GHz		-45		dB
DD_{FEXT}[Note3]	Differential far-end crosstalk	100MHz to 5GHz		-45		dB
$V_{NOISE-INPUT}$	Input-referred noise	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01		0.6		mV_{RMS}
		100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01		0.5		
$V_{NOISE-OUTPUT}$	Output-referred noise[2]	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01		0.8		mV_{RMS}
		100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01		1		
S11	Input return loss	10 MHz to 4.1 GHz differential		-13.0		dB
		1 GHz to 4.1 GHz common mode		-5.0		
S22	Output return loss	10 MHz to 4.1 GHz differential		-15		dB
		1 GHz to 4.1 GHz common mode		-6.0		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Signal and Frequency Detectors						
V_{TH_UPM}	Unplug mode detector threshold	Threshold of LFPS when the input impedance of the redriver is 67kohm to VbiasRx only. Used in the unplug mode.	200		800	mVppd
V_{TH_DSM}	Deep slumber mode detector threshold	LFPS signal threshold in Deep slumber mode	100		600	mVppd
V_{TH_AM}	Active mode detector threshold	Signal threshold in Active and slumber mode	65		175	mVppd
F_{TH}	LFPS frequency detector	Detect the frequency of the input CLK pattern	100		400	MHz
T_{ON_UPM}	Turn on of unplug mode	TX pin to RX pin latency when input signal is LFPS			3	mS
$T_{ON\text{-}DSM}$	Turn on of deep slumber mode				5	µS
T_{ON_SM}	Turn on of slumber mode				20	ns

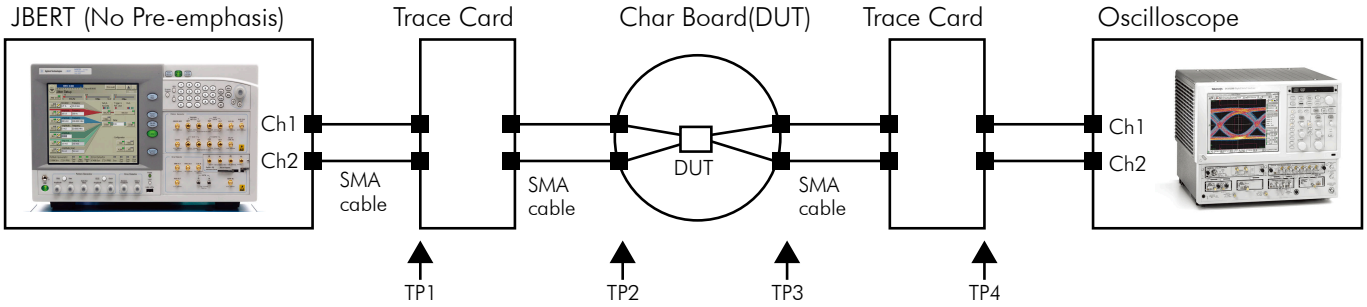
Note:
(1) Measured using a vector-network analyzer (VNA) with -15dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
(2) Guaranteed by design and characterization.
(3) Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk

5.4.3 DisplayPort Differential Channel

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{ID}	Peak to peak differential input voltage			400	1200	mV
V_{ODO}	Differential overshoot voltage				15%*V3P3	V3P3
V_{ODU}	Differential undershoot voltage				25%*V3P3	V3P3
Isc	Output short current				60	mA
Vtx diff-lev1	Differential pk-pk level 1		340	400	460	mV
Vtx diff-lev2	Differential pk-pk level 2		510	600	680	mV
Vtx diff-lev3	Differential pk-pk level 3		690	800	920	mV
Vtx diff-lev4	Differential pk-pk level 4		1020	1200	1380	mV
G_P	Peaking gain: Compensation at 4 GHz, relative to 100 MHz, 100 mVpp sine wave input	EQ<3:0>=0000 EQ<3:0>=0101 EQ<3:0>=1010 EQ<3:0>=1111		4.9 7.7 9.8 11.3		dB
		Variation around typical	-3		+3	dB
G_F	Flat gain: 100 MHz, 100mVpp sine wave input	FG<1:0>=00 FG<1:0>=01 FG<1:0>=10 FG<1:0>=11		-1.5 0 +1 +2.5		dB
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1 dB compression point of output swing at 100 MHz	SW<1:0>=10 SW<1:0>=11		1100 1200		mVppd
T_R /T_F	Rise and Fall Time	20% to 80 %		30		ps
$T_{SK(D)}$	Intra-pair differential skew				50	ps
$T_{SK(O)}$	Intra-pair differential skew				50	ps

5.4.4 Hot Plug/Unplug Detect Circuitry

Parameter	Min	Typ	Max	Unit	Notes
HPD Voltage	2.25		3.6	V	
Hot Plug Detection Threshold	2.0			V	
Hot Unplug Detection Threshold			0.8	V	
HPD pin Termination	200			kΩ	To GND
HPD de-assert debounce timer	200		450	ms	Any HPD Low to High edge will reset the debounce timer



1) Trace card between TP1 and TP2 is designed to emulate 6-48" of FR4. Trace width -4 mils,100Ω differnetial impedance
2) All jitter is measured at a BER of 10-9
3) Residual jitter reflects the total jitter measured at TP4 jitter minus TP1 jitter
4) VDD = 3.3V, RT = 50Ω
5) The input signal from JBERT does not have any pre-emphasis.

Figure 5-1 AC Electrical Parameter test setup

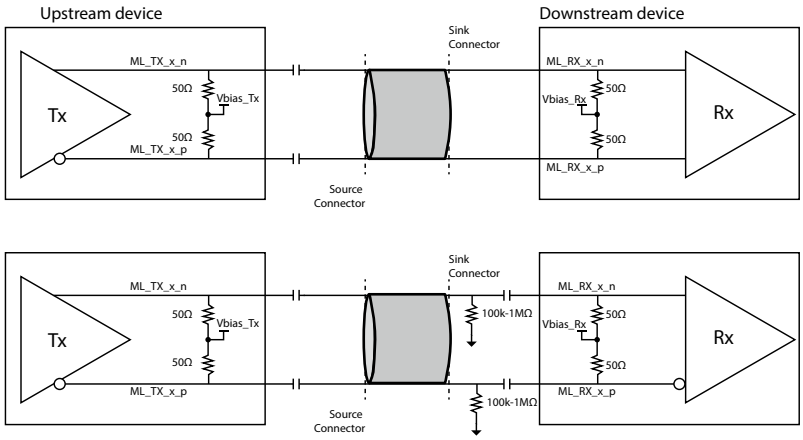


Figure 5-2 High-speed Chanel Test Circuit

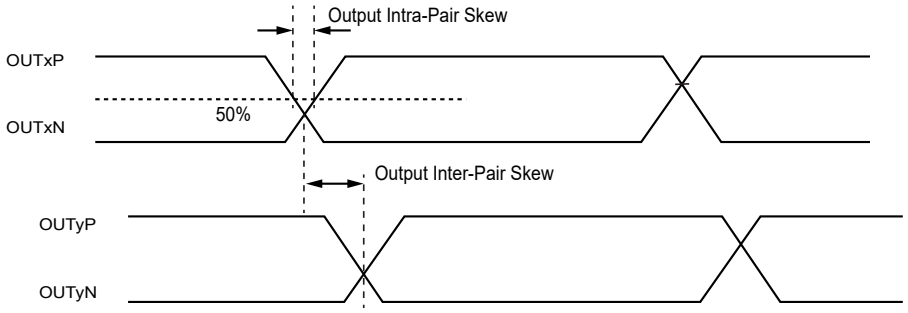


Figure 5-3 Intra and Inter-pair Differential Skew definition

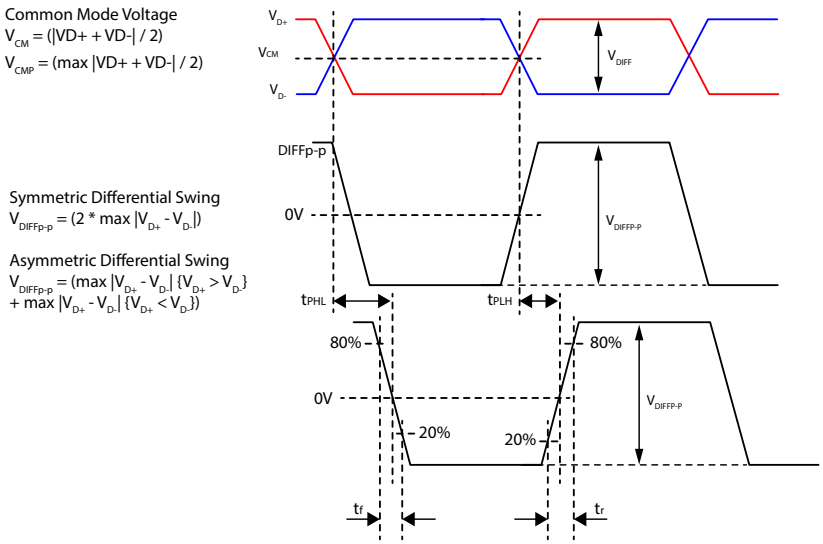


Figure 5-4 Definition of Peak-to-peak Differential voltage

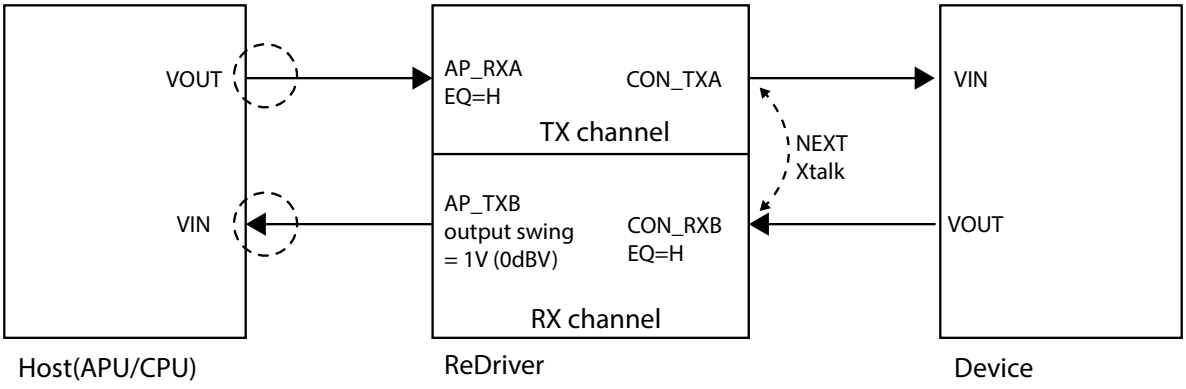


Figure 5-5 NEXT Crosstalk definition

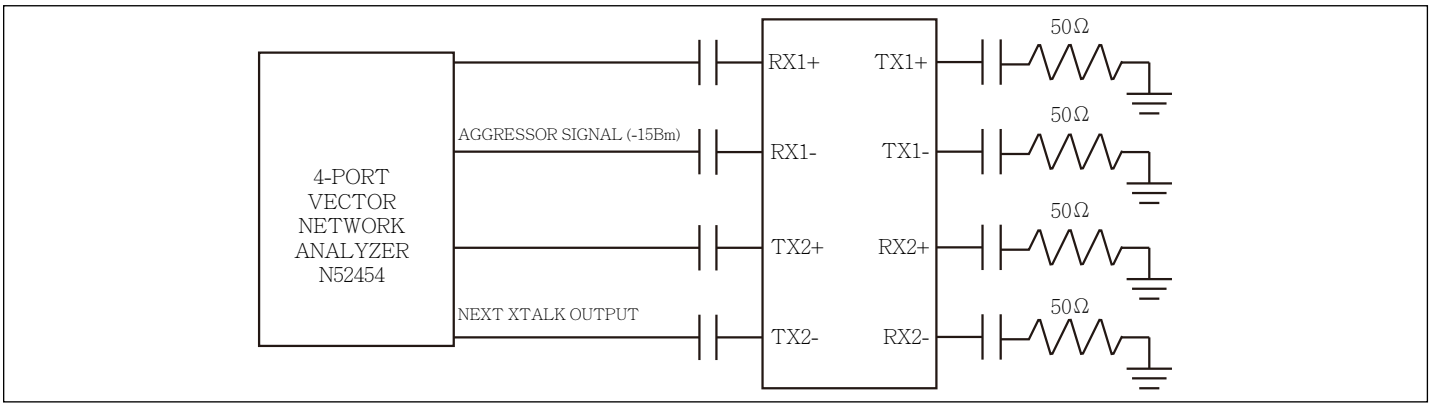


Figure 5-6 Channel-isolation test configuration

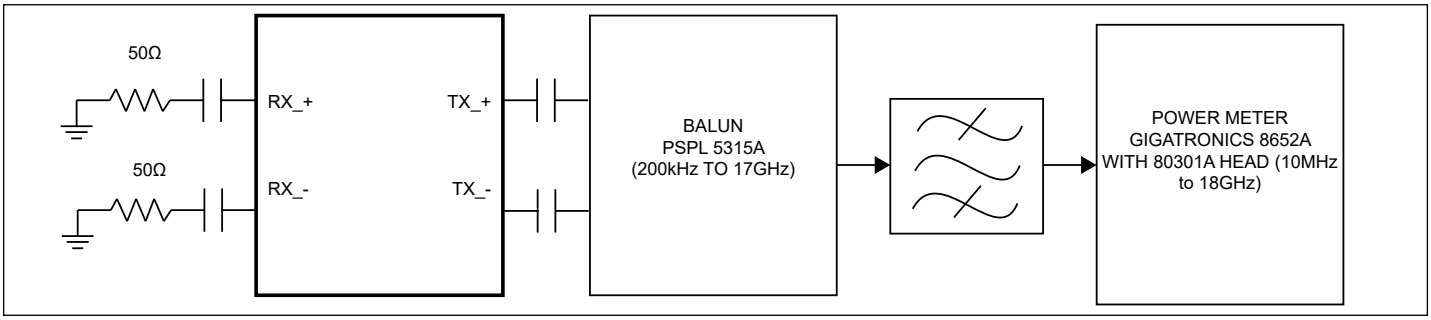


Figure 5-7 Noise test configuration

5.4.5 AI2C Bus SCL/SDA Specification

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IL}	DC input logic Low		-0.5		0.4	V
V_{IH}	DC input logic High		1.2		V_{DD}	V
V_{OL1}	DC output logic Low voltage	(open-drain or open-collector) at 3 mA sink current;	0		0.4	V
I_{OL}	Low-level output current	V_{OL} = 0.4V	20			mA
		V_{OL} = 0.6V	6			mA
I_i	Input current each I/O pin		-10		10	uA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	Bus Operation Frequency				1000	KHz
t_{BUF}	Bus Free Time Between Stop and Start condition		1.3			us
$t_{HD:STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us
$t_{SU:STA}$	Repeated start condition setup time		0.26			us
$t_{SU:STO}$	Stop condition setup time		0.26			us
$t_{HD:DAT}$	Data hold time		0			ns
$t_{SU:DAT}$	Data setup time		50			ns
t_{LOW}	Clock Low period		0.5			us
t_{HIGH}	Clock High period		0.26		50	us
t_F	Clock/Data fall time				120	ns
t_R	Clock/Data rise time				120	ns

Notes:
(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I2C physical layer specification.
(4) VIL = 0.4V and VIH = 1.2V because the silicon needs to support both SCL/SDA with 1.8V/3.3V signaling level.

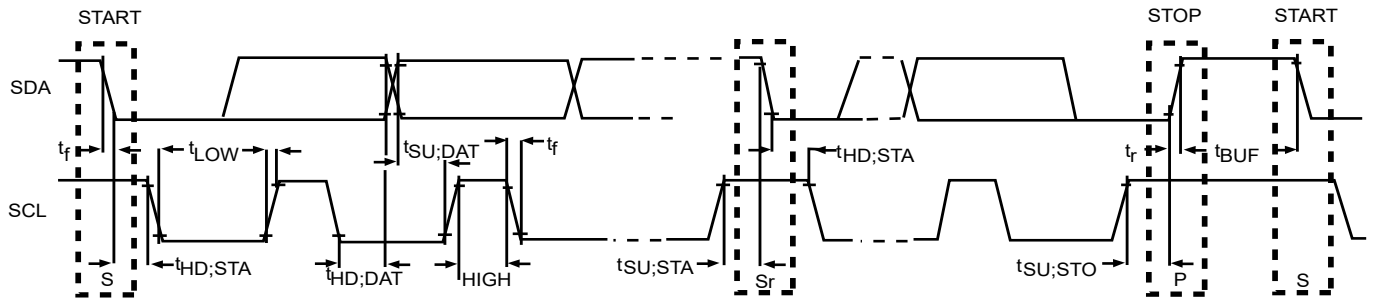


Figure 5-8 Definition of timing for F/S-mode on the I2C-bus

6. Application

Note: Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

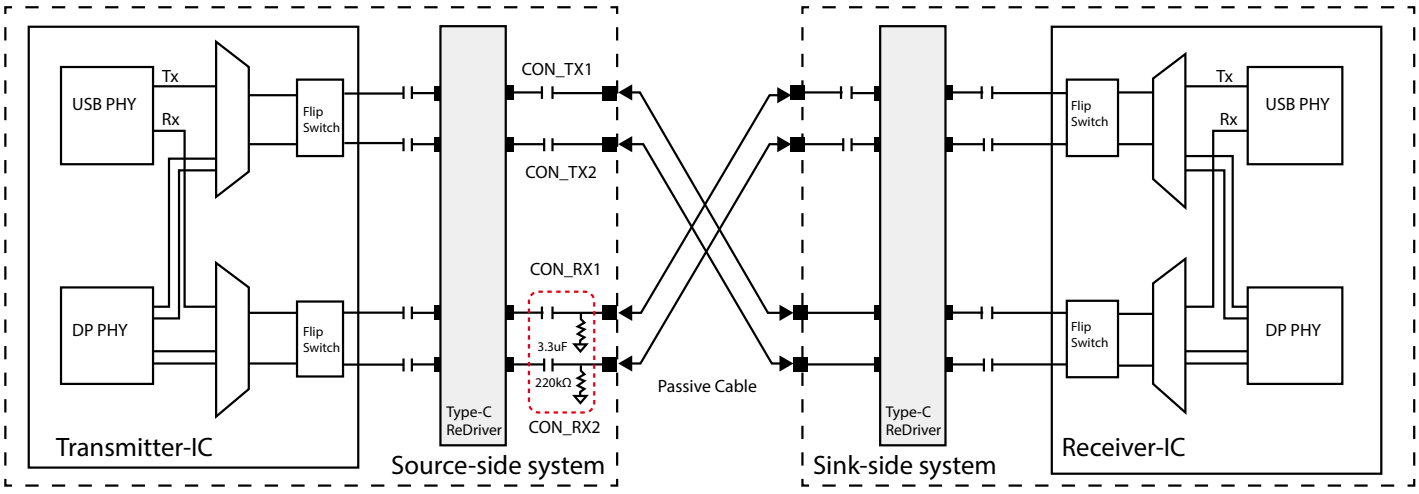
6.1 BiCMOS vs. CMOS Redriver Jitter performance comparison

Linear SiGe Redriver jitter test result was shown below. As known, SiGe Redriver can cover most of the Notebook PC routing trace length.

Redriver Type	Test Item	Input Jitter (TP1)	Output Jitter (TP2)	Output-Input Jitter	SQRT (Output2-Input2)	Units
CMOS-type Redriver	Random Jitter	0.765	0.954		0.57	rms-ps
	Deterministic Jitter	9.632	20.86	11.23		ps
BICMOS-type Redriver	Random Jitter	0.740	0.775		0.23	rms-ps
	Deterministic Jitter	9.138	15.70	6.57		ps

Figure 6-1 BiCmos vs CMOS Redriver performance comparison

6.2 Type-C high speed channel AC-cap connection diagram



Note: AC-cap is recommanded for potential Type-C Sink Device compatibility (interoperability) issues because of the different Type-C legacy implementation, not latest Type-C Logo compiant devices.

Figure 6-2 AC-capacitor circuits with Type-C passive cable

6.3 Power-up Timing

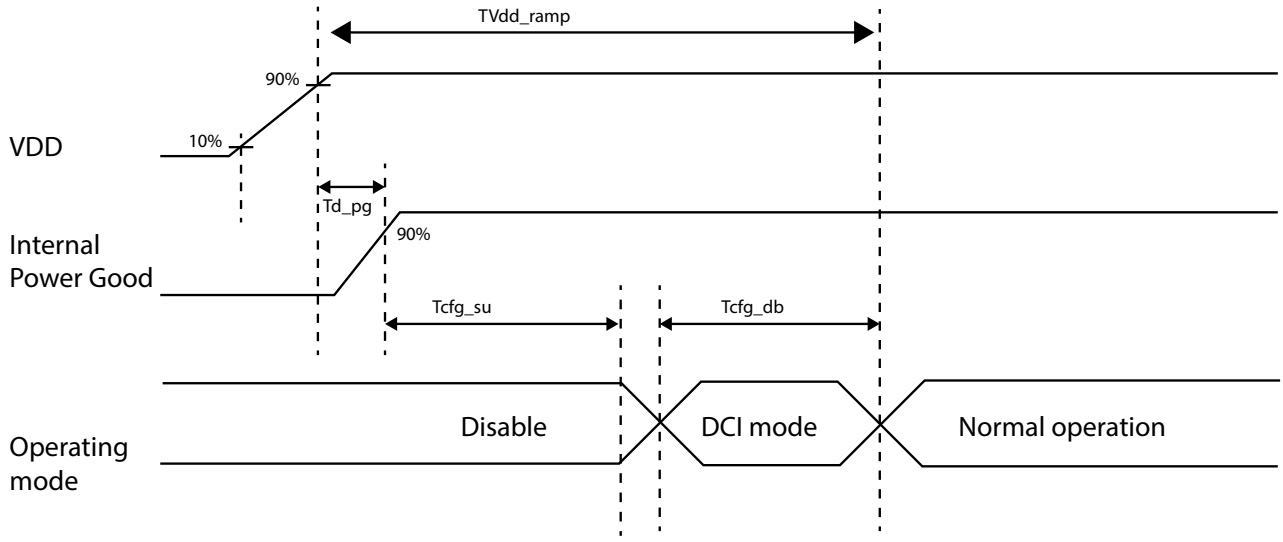


Figure 6-3 Power-up timing

Table 6-1. Power-up Timing

	Parameter	Min	Max	Unit
Td_pg	Internal Power Good		2000	µs
Tcfg_su	Configuration pin setup time		100	µs
TDCI	DCI mode	20	60	ms
TVdd_ramp	VDD supply ramp requirement		100	ms

6.4 Application Block Diagram

In order to allow manufacturer to change EQ setting without modifying PD Controller's firmware,

- PD Controller vendor shall reserve 8x6=48bytes writable registers to store PI3DPX1205A EQ table.
- EC writes the EQ table into PD Controller every time the system is powered up or reset.
- PD Controller writes corresponding EQ/FG/SW settings and features into PI3DPX1205A byte4, 5, 6, 7, 8 and 12 via I2C every time before changing channel mapping setting byte3.
- PD Controller updates HPD state via PI3DPX1205A I2C byte4 and byte12.

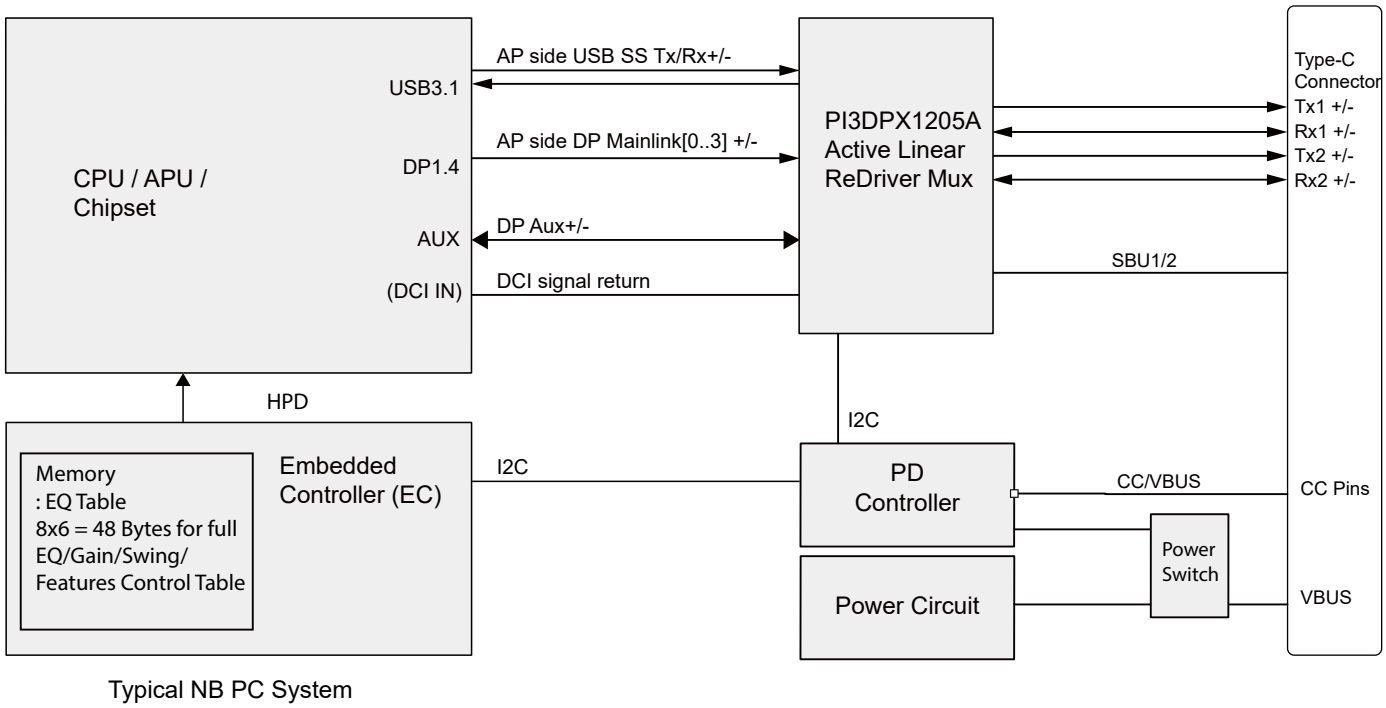


Figure 6-4 Source-side System Application Block Diagram

6.5 Interrupt Handler Programming Flow

The majority PD is controllable via an I2C interface and can be used with downward facing ports (DFP) or upward facing ports (UFP) in laptop and desktop PCs, tablets, smart phones, display monitors, and other peripherals or accessories containing a USB Type-C connector. When attached to a port partner supporting alternate mode, the PD automatically attempts to negotiate mode entry for discovered alternate modes.

Please note that PI3DPX1205A does not support sub-address. All registers must be read or written sequentially from I2C Byte 0x00. For example, in order to read I2C Byte 0x01, PI3DPX1205A I2C registers must be read sequentially from Byte 0x00 to 0x01, 0x02 to 0x03. In order to write I2C Byte 0x03, it must be written sequentially from Byte 0x00, 0x01, 0x02 to 0x03.

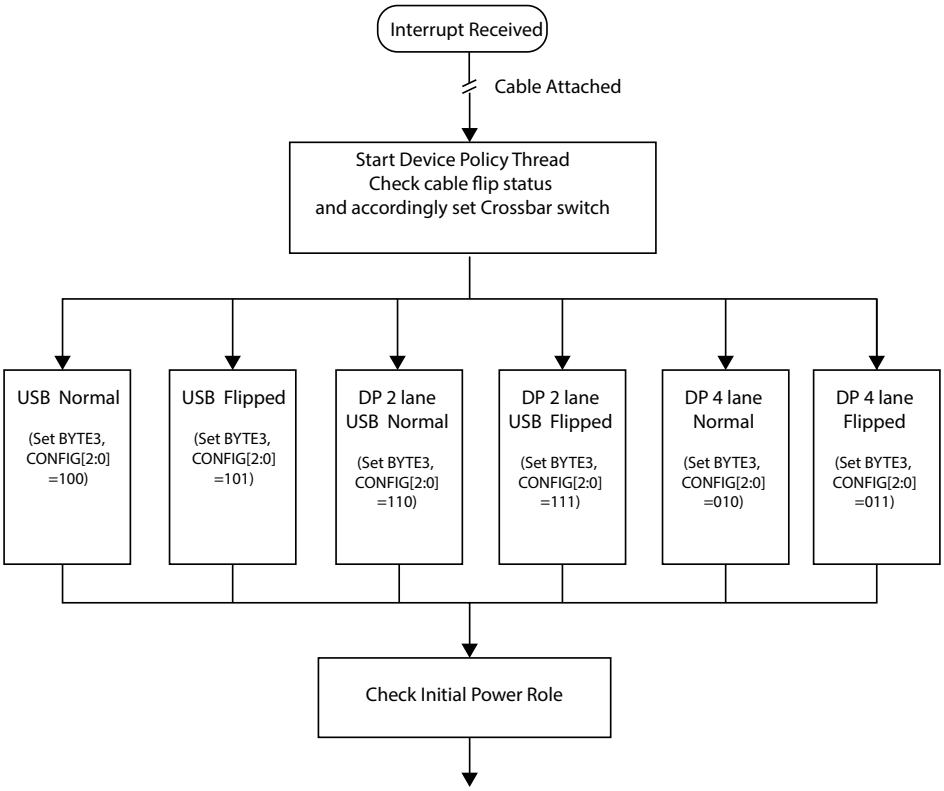


Figure 6-5 Interrupt Handler Implementation Flow

6.5.1 Initialization Code example code

```
#define IDET_VTH 0
#define DP_HPD_PIN_ENB 0
#define AUX_ENB 1
#define RX1_EQ 0
#define RX1_FG 0
#define RX1_SW 0
#define TX1_EQ 0
#define TX1_FG 0
#define TX1_SW 0
#define TX2_EQ 0
#define TX2_FG 0
#define TX2_SW 0
#define RX2_EQ 0
#define RX2_FG 0
#define RX2_SW 0

#define PI3DPX1205A_BYTE12 ((IDET_VTH) << 6 | (DP_HPD_PIN_ENB) << 2 | (AUX_ENB) << 1)
#define PI3DPX1205A_BYTE8 ((RX1_EQ) <<4 | (RX1_FG) <<2 | RX1_SW)
#define PI3DPX1205A_BYTE7 ((TX1_EQ) <<4 | (TX1_FG) <<2 | TX1_SW)
#define PI3DPX1205A_BYTE6 ((TX2_EQ) <<4 | (TX2_FG) <<2 | TX2_SW)
#define PI3DPX1205A_BYTE5 ((RX2_EQ) <<4 | (RX2_FG) <<2 | RX2_SW)

//PI3DPX1205A Init routine
//return 0 if fail
int pi3dpx1205a_init(struct i2c_client *client)
{
    int res;
    u8 data[13];

res = pi3dpx1205a_readn(client, 13, u8 &data);

if (res <13)
    return 0; //Fail

data[12]= PI3DPX1205A_BYTE12;
    data[[8]= PI3DPX1205A_BYTE8;
    data[[7]= PI3DPX1205A_BYTE7
    data[[6]= PI3DPX1205A_BYTE6;
    data[[5]= PI3DPX1205A_BYTE5;

res = pi3dpx1205a_writen(client, 13, &data);

if (res <13)
    return 0; //Fail

    return res;
}
```

6.5.2 Read/Write Byte 3 to set Active MUX example code

```
//Write PI3DPX1205A Byte 3 to set switch mode
//input: confg   (please refer to Fig. 3;  For safe mode, confg[2:0]=00x)
//return value: no of byte written
int pi3dpx1205a_set_mux(struct i2c_client *client, u8 confg)
{

      //Read byte 3
int reg = pi3dpx1205a_read(client, 3)

      if (reg < 0)
            return 0;

      reg &= 0x8F;
      reg |= (confg <<4);

return pi3dpx1205a_write(client, 3, reg);
}

/Read PI3DPX1205A Byte 3 to get switch mode
//return value: Byte3
int pi3dpx1205a_get_mux(struct i2c_client *client)
{

int reg = pi3dpx1205a_read(client, 3)

      if (reg > 0)
      {
            reg &= 0x70;
            return (reg >>4);
      }
return reg;
}
```

6.5.3 I2C Multi-Byte Read / I2C Block Read using i2c_smbus_read_i2c_block_data()

```
//Read PI3DPX1205A I2C reg from BYTE0 to BYTE len-1
//return value: no of byte read
int pi3dpx1205a_readn( struct i2c_client *client, u8 len, u8 *val)
{

        //Read I2C Byte0 to Byte len-1
        return i2c_smbus_read_i2c_block_data(client, 0, len, val);

}

//Read PI3DPX1205A I2C reg Byte N
//return value: Byte N
int pi3dpx1205a_read( struct i2c_client *client, u8 N)
{

        u8 data[N+1];
        int res;

        //Read I2C Byte0 to Byte N
        res = pi3dpx1205a_readn(client, N+1, &data);

        if (res >0)
                return data[N];

        return res;
}
```

6.5.4 I2C Multi-Byte Write / I2C Block Write using i2c_smbus_write_i2c_block_data()

```
//Write PI3DPX1205A I2C reg from BYTE0 to BYTE len-1
//return value: no of byte written
int pi3dpx1205a_writen( struct i2c_client *client, u8 len, u8 *val)
{

    //Write I2C Byte0 to Byte len-1
    If (len >1)
            return i2c_smbus_write_i2c_block_data(client, *val[0], len, val[1]);
    return i2c_smbus_write_byte(client, *val[0]);
}

//Write PI3DPX1205A I2C reg Byte N
//return value: no of byte written
int pi3dpx1205a_write( struct i2c_client *client, u8 N, u8 val)
{

    u8 data[N+1];
    int res;

    //Read I2C Byte0 to Byte N
    res = pi3dpx1205a_readn(client, N+1, &data);

    if (res >0)
    {
            data[N]=val;
            return pi3dpx1205a_writen(client, N+1, &data);
    }

return res;
}
```

6.6 Redriver Placement Consideration

6.6.1 USB3.1 10Gbps System Design Challenges

- Jitter budget is basis for Tx and Rx compliance specs.
- Loss budget is basis for compliance channels, including pad cap, package, PCB routing

	DJ (ps)	RJ (ps)	TJ (ps)	Term	
Tx Jitter	17.0	14.1	31.1	Transmitter	Practical route length is <6". Consider a linear redriver if design exceeds 8.5db
Channel Jitter	36.0		36.0	Channel	
Rx Jitter	27.1	14.1	41.2	Receiver	
Total	80.1	19.9	100.0	System	

6.6.2 Typical Routing Configuration

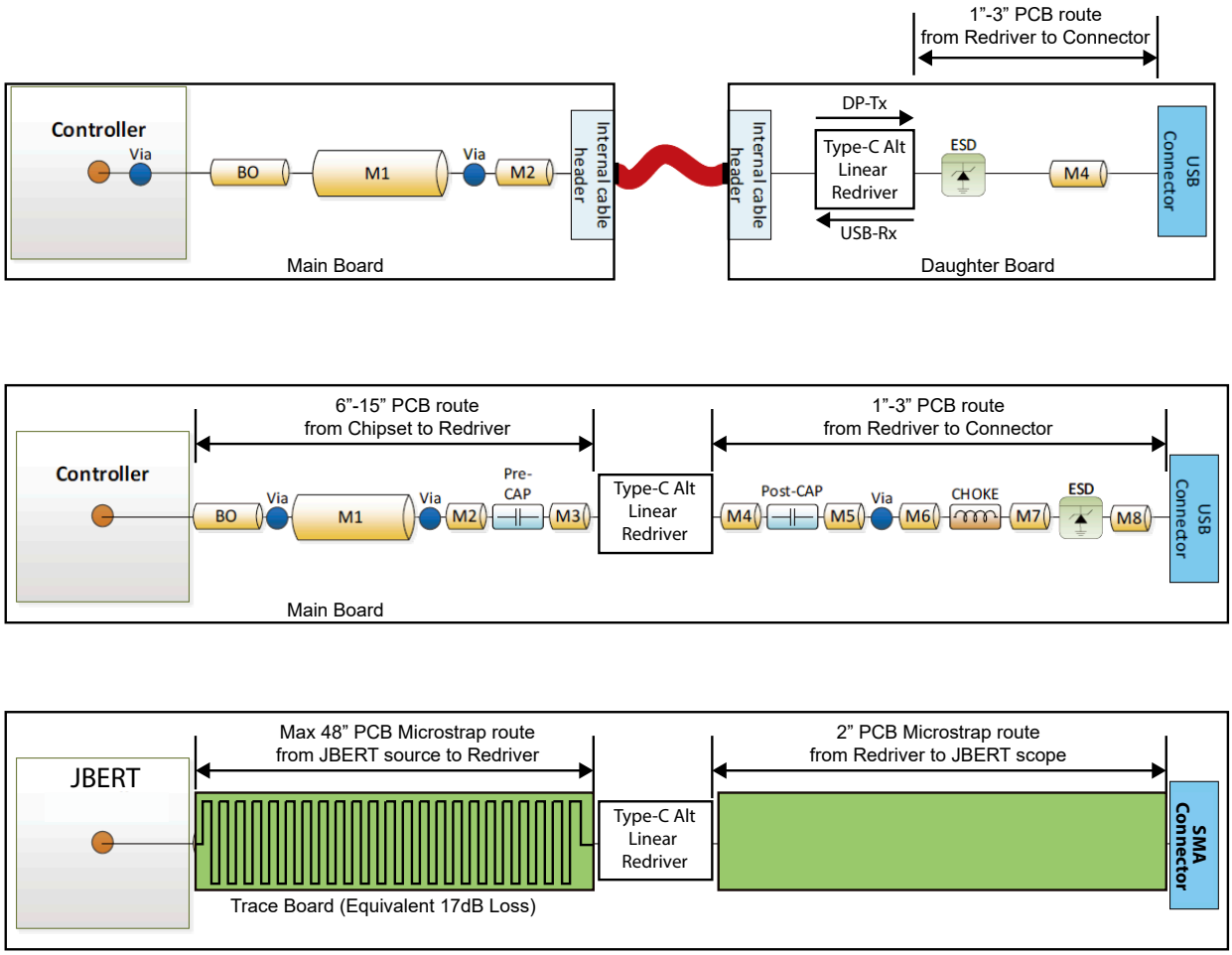


Figure 6-6 Redriver placement in the Source-side application

6.6.3 Type-C 10Gbps PCB routing estimates

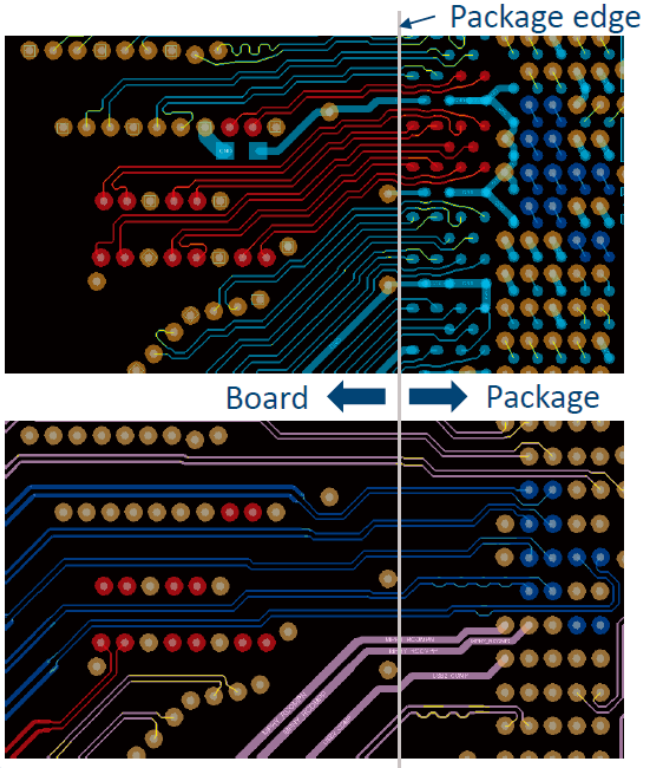
	USB Gen1 5Gbps	USB Gen2 10Gbps	Comments
Loss Budget	6.5dB @ 2.5GHz	8.5dB @ 5GHz	Loss budgets are for host/device from silicon to port connector.
USB 3.1 only	5.5” –6.5”	5.0” –6.0”	
USB 3.1 + discrete alt mode mux	4.0” –5.0”	3.0” –4.0”	USB Type-C need MUX for flippability and switching between USB3.1 and alternate modes. Mux loss is ~1.5dB. It reduces max length by ~1dB/inch.
USB 3.1 + integrated alt mode mux	5.5” –6.5”	5.0” –6.0”	

Note: (1) These are estimates only. Work with your supplier to determine actual supported length. (2) Estimates assume silicon pad cap, jitter & swing at WC recommended/allowed by spec, direct route on PCB from package to Type C™ receptacle, integrated mux has no significant impact on silicon pad cap. (3) Actual lengths also depend upon silicon (swing, jitter, EQ, pad cap), package (loss,impedance, crosstalk) and PCB materials.

6.6.4 PCB Crosstalk Minimization recommendation

Breakout Tx and Rx I/O on different PCB layers.

- Non-interleaved routing. Eliminates a key source of near end crosstalk.
- Places requirements on Tx & Rx I/O placement as shown below.



Board surface layer:
• Tx BGAs at outer region
• Breakout as Microstrip

Board inner layer:
• Rx BGAs at inner region
• Breakout as Stripline

Figure 6-7 Breakout Tx and Rx I/O on different PCB layers

6.7 Application Reference Schematic

- AUXP/N and AUXSBU1/2 polarity connection between CPU Chipset and Type-C Connector is swapped.

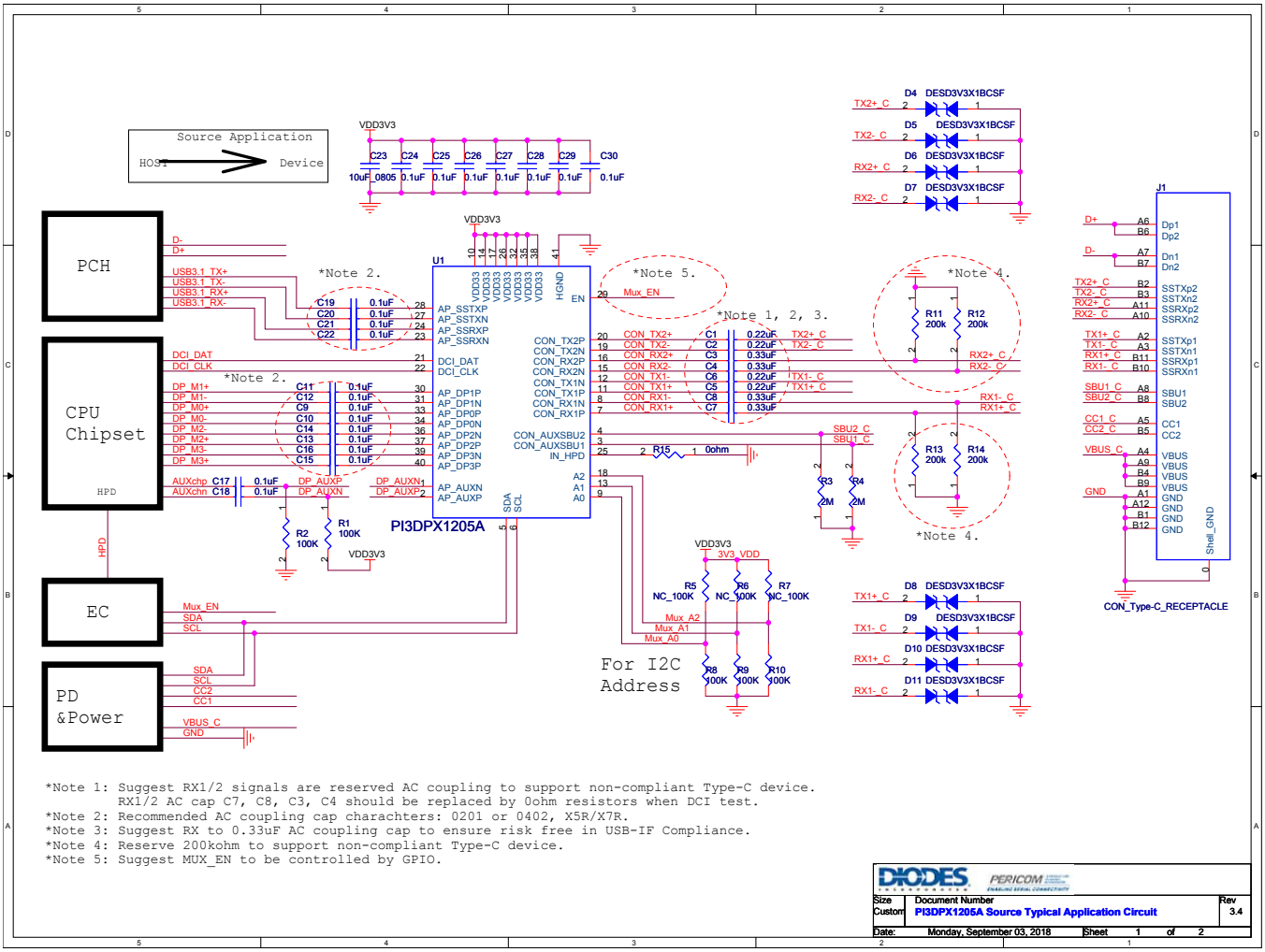


Figure 6-8 Application Reference Schematic

6.8 PCB Layout Guideline

6.8.1 General Power and Ground Guideline

To provide a clean power supply for Diodes high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

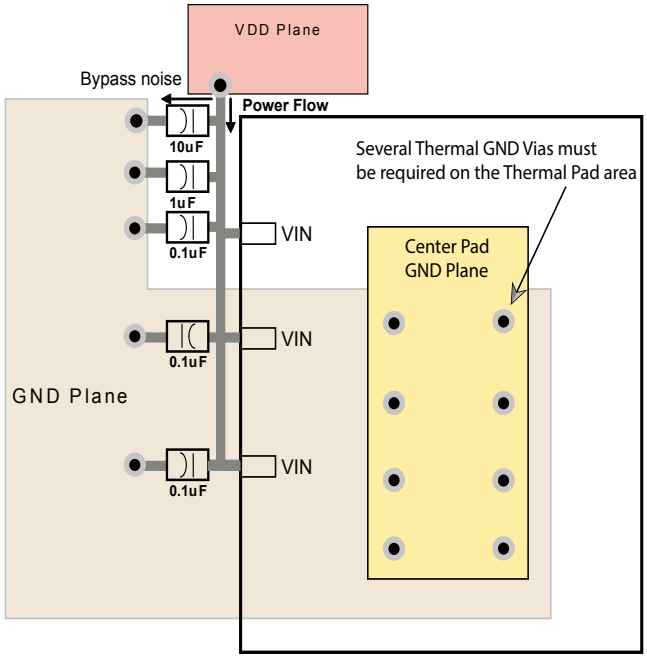


Figure 6-9 Decoupling Capacitor Placement Diagram

6.8.2 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

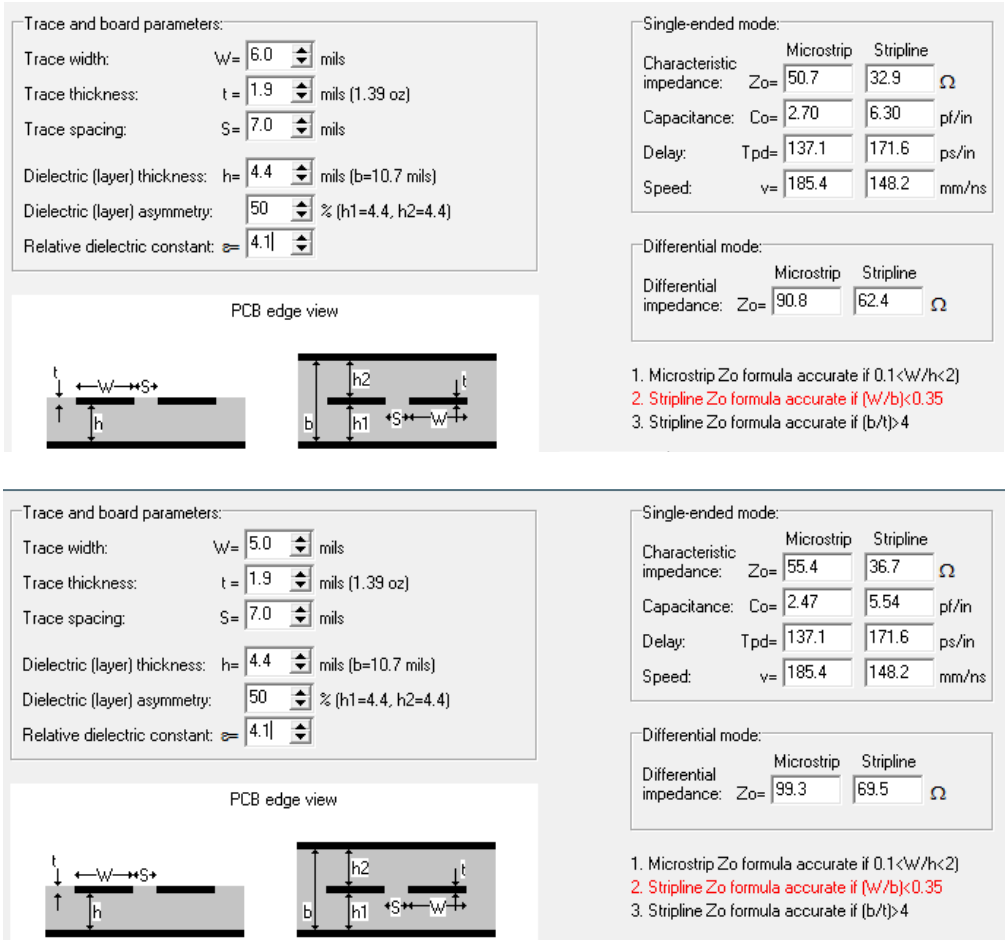


Figure 6-10 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

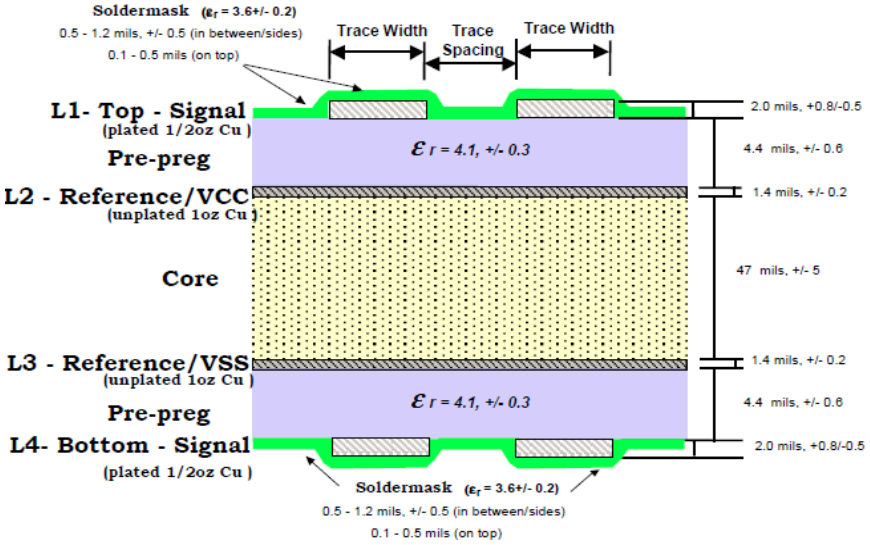


Figure 6-11 4-Layer PCB Stack-up Example

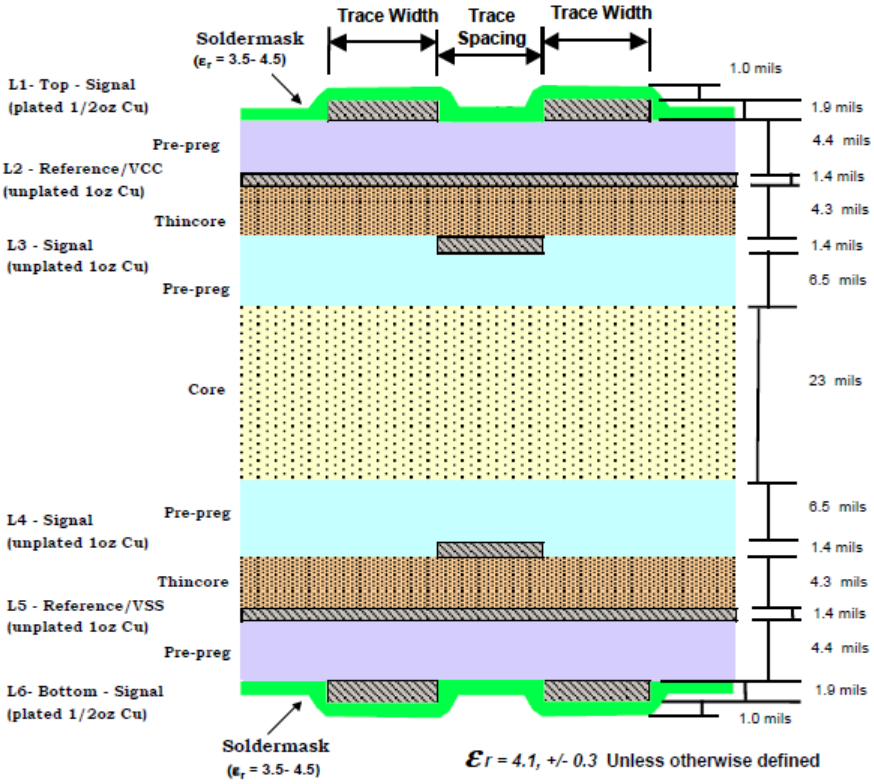


Figure 6-12 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

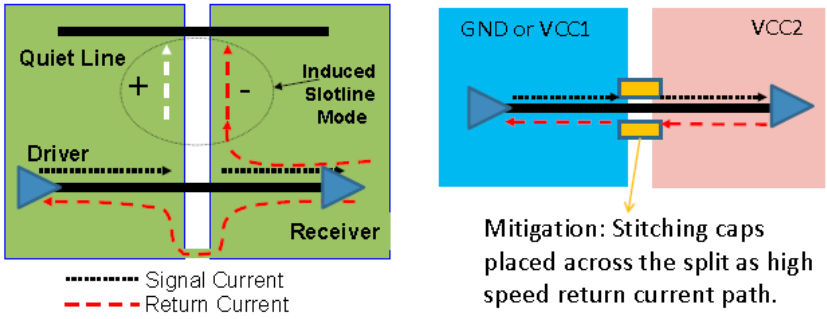


Figure 6-13 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

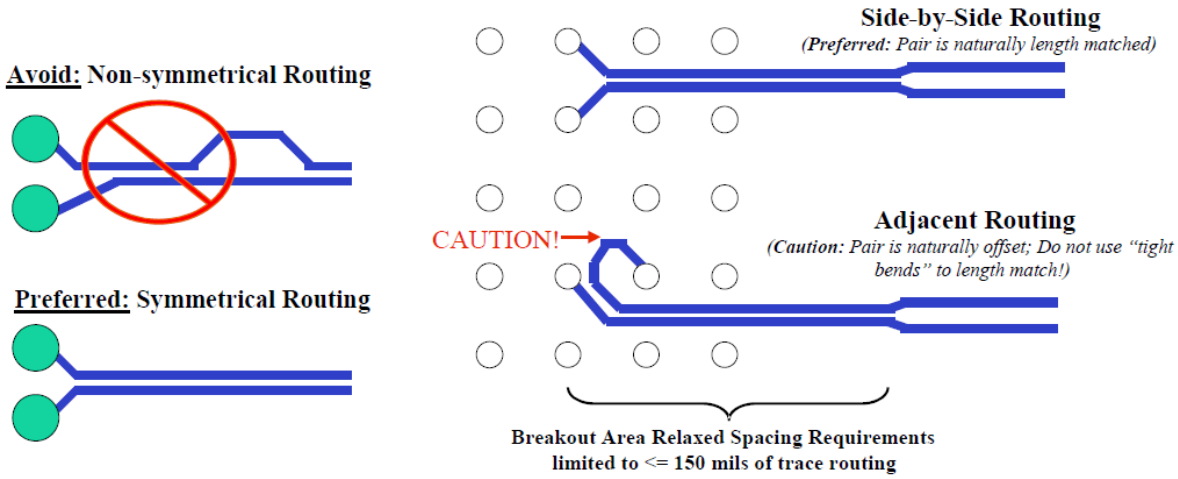


Figure 6-14 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

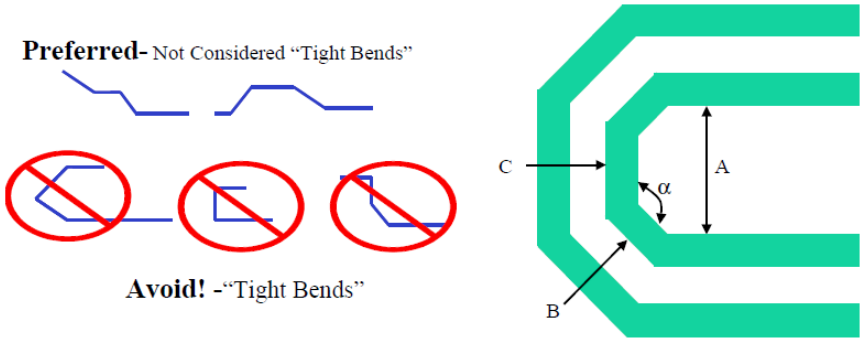


Figure 6-15 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

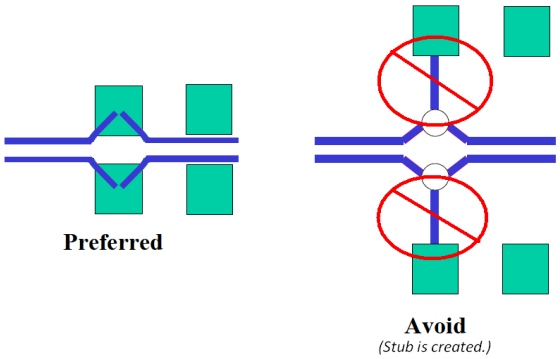


Figure 6-16 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

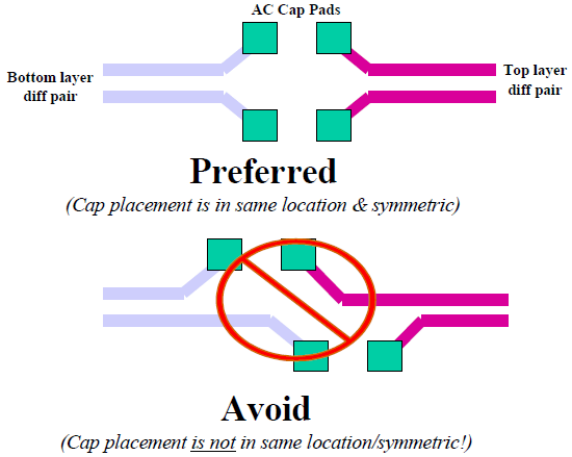


Figure 6-17 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

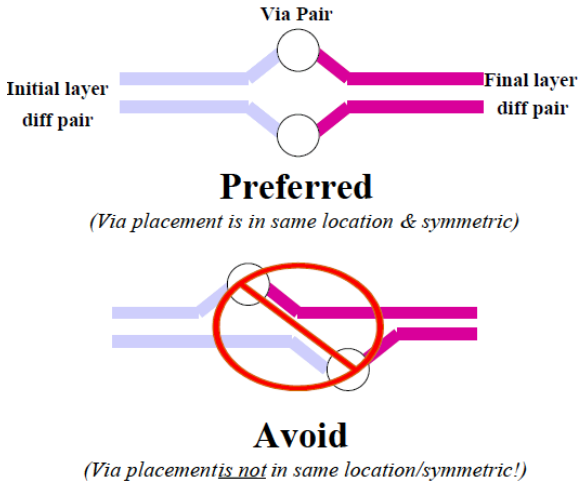


Figure 6-18 Layout Guidance of Stitching Via

6.9 CTS Compliance Test

6.9.1 DisplayPort Compliance Test Report

Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Test Specification	1.4
Lane	4 Lanes
SSC	Disabled
Test Session Details	
DisplayPort Test Controller	UnigrafDPTC
Fixture Type	Other
Infiniium SW Version	05.70.00901
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	3.52.0001
Debug Mode Used	No
Compliance Limits (official)	DisplayPort Compliance Test Specification Version 1.4 Official Test Limit
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (9 JAN 2017 10:16:47), Using Cal Atten (5.7433E+000) Skew: Calibrated (9 JAN 2017 10:17:05), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (9 JAN 2017 10:18:00), Using Cal Atten (5.5352E+000) Skew: Calibrated (9 JAN 2017 10:18:15), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (9 JAN 2017 10:19:03), Using Cal Atten (5.7151E+000) Skew: Calibrated (9 JAN 2017 10:19:16), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (9 JAN 2017 10:20:00), Using Cal Atten (5.5492E+000) Skew: Calibrated (9 JAN 2017 10:20:11), Using Cal Skew
Last Test Date	2017-01-12 16:19:05 UTC +08:00

Figure 6-19 DisplayPort Compliance Test Report

Table 6-2. CTS Testing Trace loss information

DP FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 8.1Gbps	-8.15 dB	-11.52 dB	-14.88 dB	-17.60 dB	-19.94 dB	-22.92 dB	-28.62 dB

6.9.2 USB3 Compliance Test Report

Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
10GTransFunc	C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions\SSGen2_TxComp12p2dB_Embedding.tf4
5GTransFunc	C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions\U7242A_Deembed__USB3_TX_Host_Channel.tf4
AdcMode	AUTO
DC Gain	0
Reference Clock	SSC
Device	Host
Device ID:	Device 1
Test Session Details	
Infiniium SW Version	06.00.00628
Infiniium Model Number	MSOV334A
Infiniium Serial Number	MY55430101
Application SW Version	3.20
Debug Mode Used	No
Compliance Limits (official)	USB 3.1 Specification version 1.0
Last Test Date	2017-05-09 08:35:14 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	13
Total	13

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Deemphasis	-3.449875 dB	32.5 %	-4.100000 dB <= VALUE <= -2.100000 dB
✓	0	1	Preshoot	2.5 dB	35.0 %	1.2 dB <= VALUE <= 3.2 dB
✓	0	1	10G TSSC-Freq-Dev-Min	-4.499636 kppm	50.0 %	-5.300000 kppm <= VALUE <= -3.700000 kppm
✓	0	1	10G TSSC-Freq-Dev-Max	-18.142 ppm	47.0 %	TSSCMin ppm <= VALUE <= TSSCMax ppm
✓	0	1	10G SSC Modulation Rate	30.989320 kHz	33.0 %	30.000000 kHz <= VALUE <= 33.000000 kHz
✓	0	1	10G SSC df/dt	429.5 ppm/us	65.6 %	VALUE <= 1.2500 kppm/us
✓	0	1	10G Random Jitter (CTLE ON)	441 fs	55.9 %	VALUE <= 1.000 ps
✓	0	1	10G Short Channel Template Test	0.000	100.0 %	VALUE = 0.000
✓	0	1	10G Short Channel Extrapolated Eye Height	299.9 mV	328.4 %	VALUE >= 70.0 mV
✓	0	1	10G Short Channel Minimum Eye Width	65.4268 ps	36.3 %	VALUE >= 48.0000 ps
✓	0	1	10G Far End Template Test (CTLE ON)	0.000	100.0 %	VALUE = 0.000
✓	0	1	Extrapolated Eye Height	110.0 mV	57.1 %	VALUE >= 70.0 mV
✓	0	1	Minimum Eye Width	66.3510 ps	38.2 %	VALUE >= 48.0000 ps

Figure 6-20 USB3 Compliance Test Report

6.9.3 Interoperability Test Result

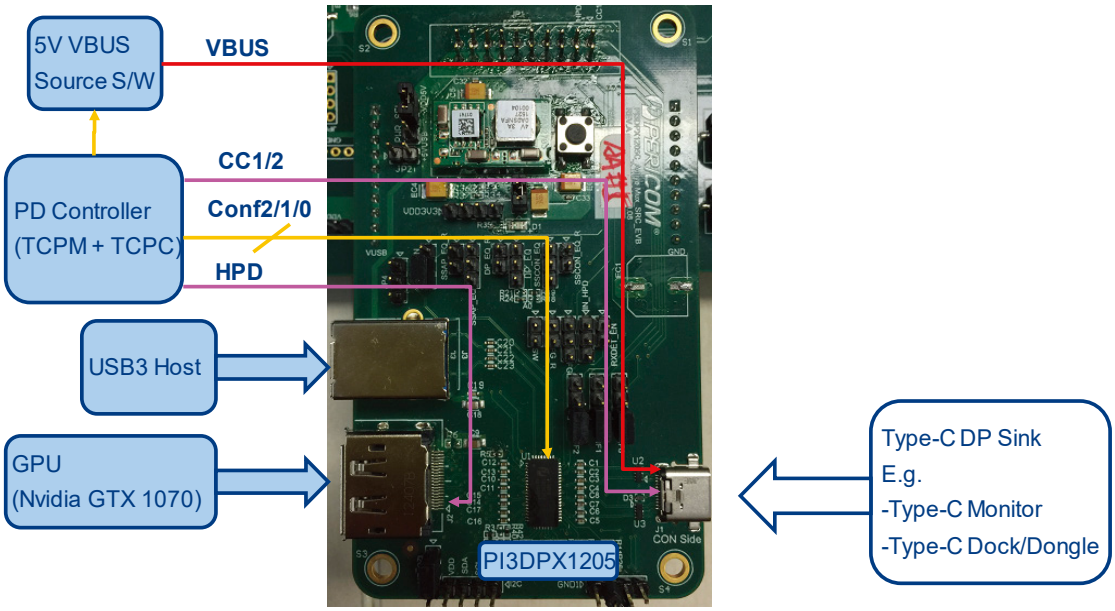


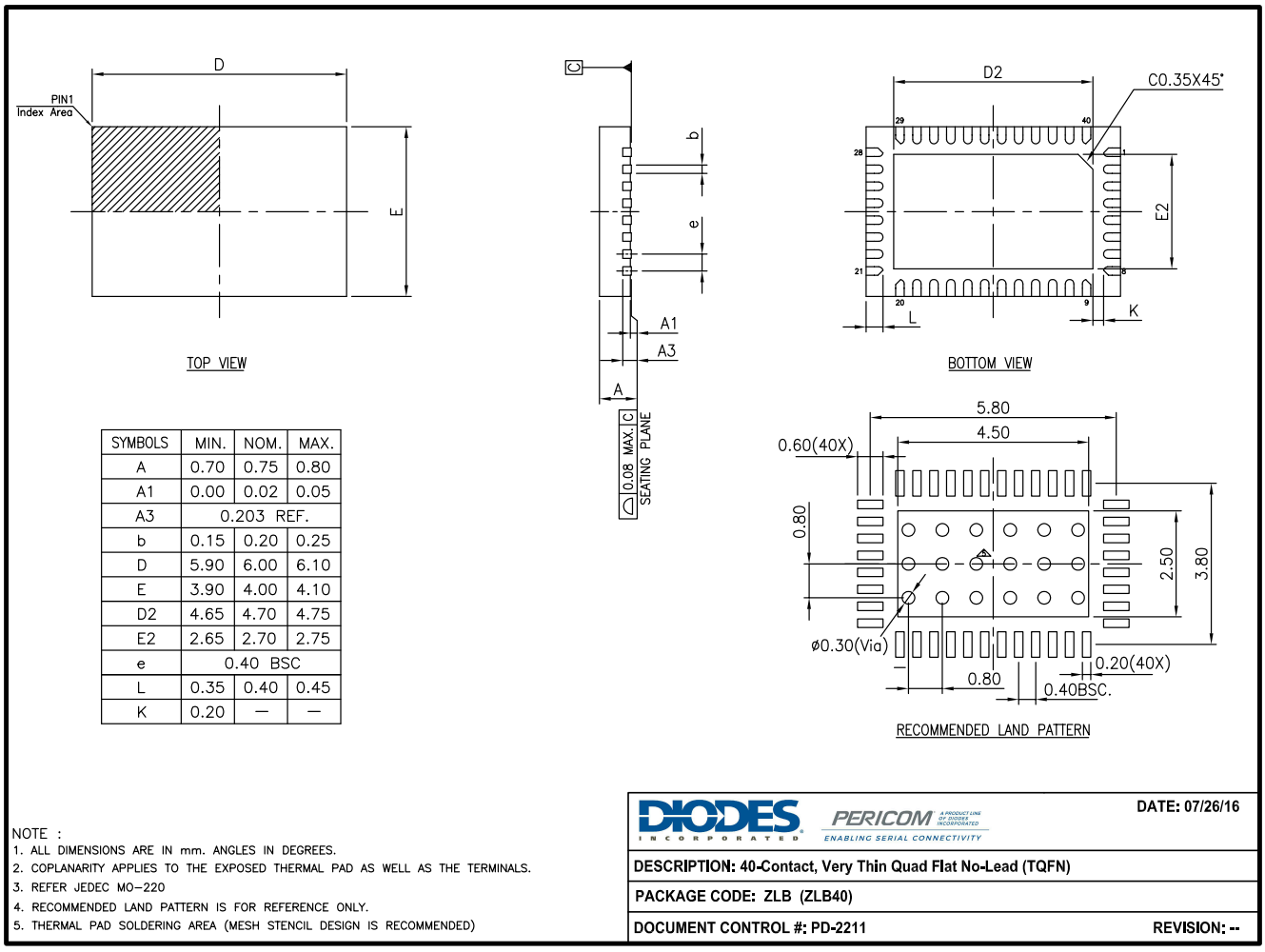
Figure 6-21 Type-C Source Test Board

Table 6-3. Type-C Interoperability Test Result

	Monitor (sink-side device)	Result (Date: Dec 2016)
C-to-DP Cable	Viewsonic VP-2780-4K HDMI2.0/DP1.2a	Pass
C-to-DP Cable	DELL UP2414Qt DP1.2	Pass
C-to-DP Cable	Realtek DP1.3 Montior	Pass
C-to-DP Cable	Mstar HBR3 (=DP1.3) Monitor	Pass
C-to-C Cable	LG 27UD88-W	Pass
Type-C Dock (i.e. Apple Digital AV Adapter, Huawei MateDock, Microsoft Type-C Dock HD-500, E-BOUR Type-C Dock, Dell Dock DisplayPort)	LG 27UD88-W	Pass
C-to-DP Cable/Dongle (i.e. Google, Amphenol, Luxshare, VIA VisionTek, Kanex, CableTime, Aomax, JS Create, ASL, Club)	LG 27UD88-W	Pass

7. Mechanical/Package Information

7.1 Mechanical Outline



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	3.90	4.00	4.10
D2	4.65	4.70	4.75
E2	2.65	2.70	2.75
e		0.40 BSC	
L	0.35	0.40	0.45
K	0.20	—	—

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DATE: 07/26/16

DESCRIPTION: 40-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZLB (ZLB40)

DOCUMENT CONTROL #: PD-2211 REVISION: --

Figure 7-1 PI3DPX1205A(40-pin) Package Mechanical Dimension

7.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an "add mark" operation which places the speed code letter at the end of the complete part number.

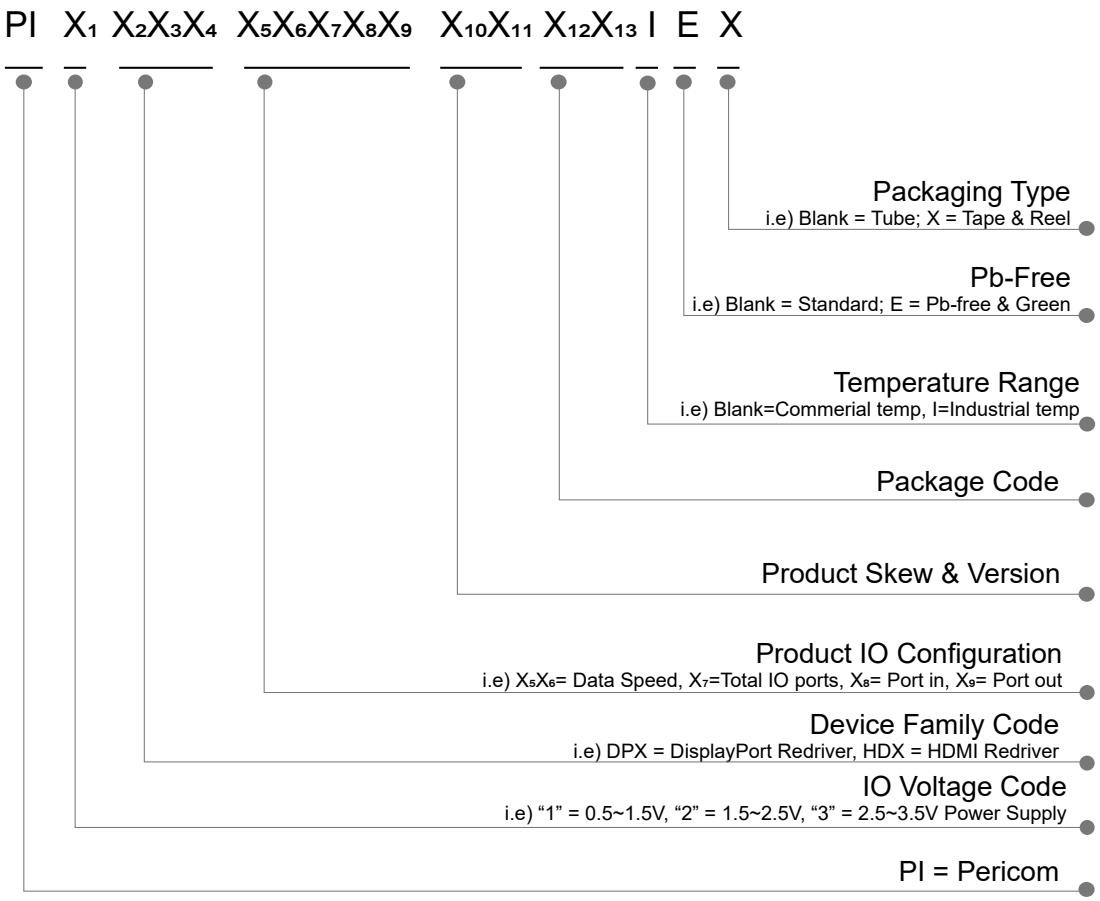


Figure 7-2 Product naming information

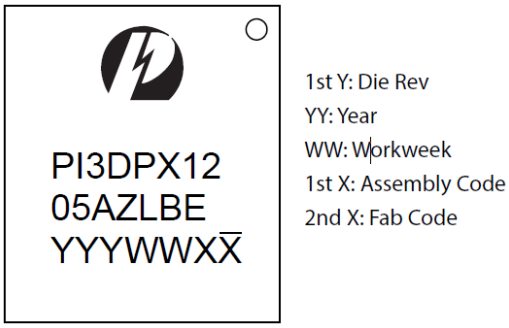


Figure 7-3 Package marking information

7.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6 Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Anti-static High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

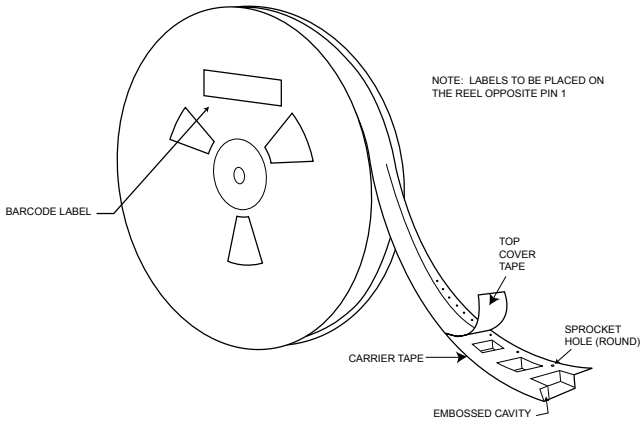


Figure 7-4 Tape & Reel label information

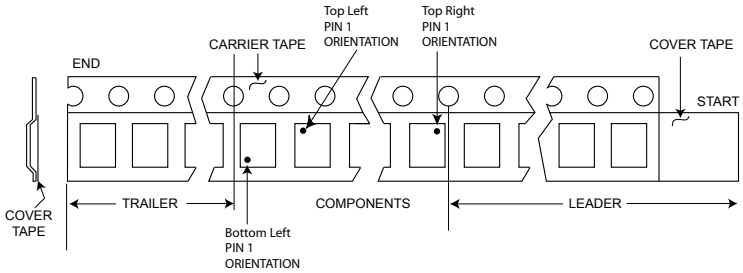


Figure 7-5 Tape leader and trailer pin 1 orientations

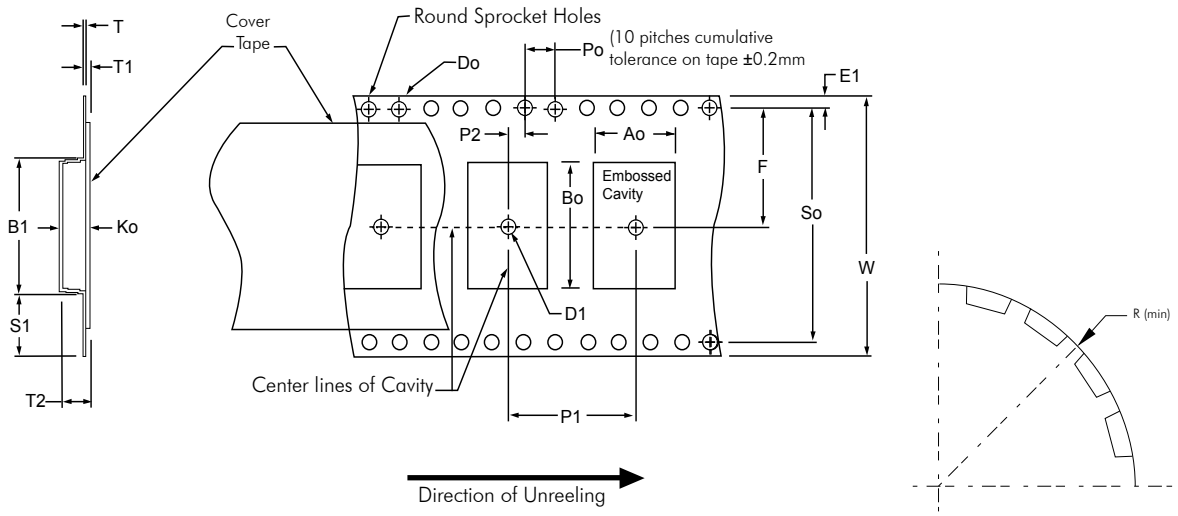


Figure 7-6 Standard embossed carrier tape dimensions

Table 7-1. Constant Dimensions

Tape Size	D_0	D_1 (Min)	E_1	P_0	P_2	R(See Note 2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 7-2. Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

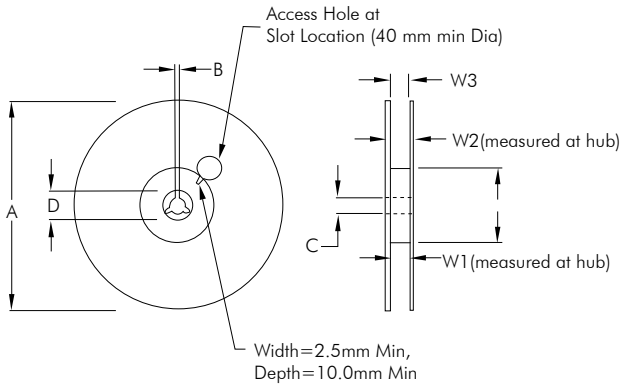


Table 7-3. Reel dimensions by tape size

Tape Size	A	N (Min) See Note A	W1	W2(Max)	W3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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