◇Structure Silicon Monolithic Integrated Circuit
◇Product Name 10bit 8channels・D/A converter (with output buffer)
◇Model Name BU2506FV
◇Application Adjustment/control of industrial or home-use electric equipment, such as DVD, CD-R, CD-R/W, and DVC.
◇Features # The BU2506FV is an integrated semiconductor of CMOS structure with 8 channels of built – in high quality 10 bit D/A converters with output buffer operational amplifiers of Rail to Rail output type
Digital input corresponds to TTL level input.
#Data is inputted by 14 bit 3-wire serial data + reset signal.
[Address 4 bit + Data 10 bit]
It is able to cascading serial use with "Do" terminal.
Highly stable output buffer operational amplifier allow operation in the all voltage range from power supply to ground.
Adopting compact package of 0.65mm pitch 20 pin..

◇Absolute Maximum Rating：(Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	-0.3~6.0	V
Upper reference voltage of D/A converter	VDD	-0.3~6.0	V
Input voltage	VIN	-0.3~6.0	V
Output voltage	VOUT	-0.3~6.0	V
Storage temperature	Tstg	-55~125	℃
Power dissipation	Pd	400 #	mW

Operating at higher than Ta=25℃, 4mW shall be reduced per 1℃.
* 70mm×70mm, thickness1.6mm, less than 3% share of copper foil when implementing glass epoxy board.
* This product is not designed for protection against radioactive rays.

◇Power supply operating voltage range：(Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	4. 5~5. 5	V
Operating temperature	Topr	-30~85	℃

◇Directions
・Described values and data are typical values on design, therefore the values are not guaranteed.
・The application circuit example is supposed to be recommended, however, verify properties sufficiently if this IC is used. When using it by changing external part constant, take enough margin in consideration of dispersion in external part and our LSI including DC and AC characteristic.
・Absolute maximum rating
We are careful enough for quality control about this IC. So, there is no problem under normal operation, excluding that it exceeds the absolute maximum ratings. However, this IC might be destroyed when the absolute maximum rating such as impressed voltages (Vcc, VM) or the operating temperature range (Topr) is exceeded, and whether the destruction is short circuit mode or open circuit mode cannot be specified. Please take into consideration the physical countermeasures for safety, such as fusing, if a particular mode that exceeds the absolute maximum rating is assumed.
・GND line
The ground line is where he lowest potential and transient voltage are connected to the IC.
・Thermal design
Take enough margins taking power dissipation under actual usage into account.
・Short circuit mode between terminals and wrong mounting
Do not mount the IC in the wrong direction and be careful about the reverse connection of the power connector. Moreover, this IC might be destroyed when the dust short the terminals between them or GND.
・Radiation
Strong electromagnetic radiation can cause operation failures.
・Added some ripple and noise to power supply terminals, this IC can't keep the accuracy of the D/A converter.
Therefore, it is recommended that external bypass capacitor should set as close as possible to the terminals between VDD and GND in order to stabilizes the D/A converter.
・The capacitor between output and GND recommend to set under 100pF including parasitic capacitor in order to reduces jitter and noise from layout of the output line.
・LSB-first or MSB-first decoding are selected by REVERSE terminal. Therefore, REVERSE terminal should be set as "open" or "VDD short" at LSB-first mode, "GND short" at MSB-first mode.

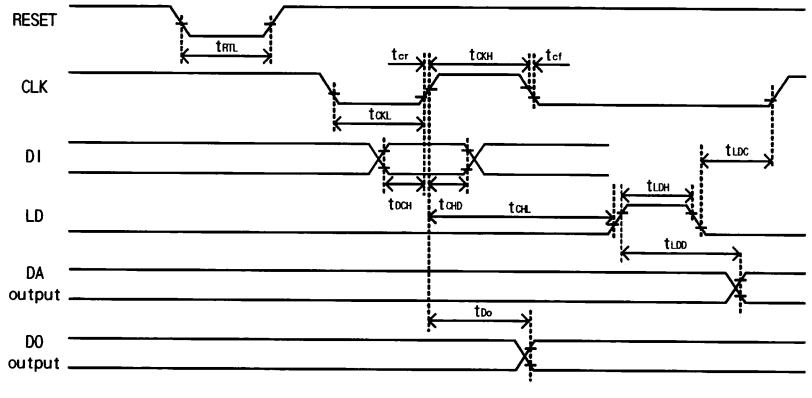
◇Electrical Characteristics (VCC=5V,VrefH=5V,VrefL=0V,Ta=25℃, unless otherwise noted)

Parameter		Symbol	Limits			Unit	Test conditions
			MIN.	TYP.	MAX.		
<<Digital part>>							
Circuit current		ICC	-	0.85	2.8	mA	CLK=10MHz operation、VCC=5V, IAO=0μA
Input leak current		IILK	-5	-	5	μA	VIN=0~VCC
Input low voltage		VIL	-	-	0.8	V	
Input high voltage		VIH	2.0	-	-	V	
Output low voltage		VOL	0	-	0.4	V	IOL=2.5mA
Output high voltage		VOH	4.6	-	5	V	IOH=-2.5mA
<< Analog part >>							
Current dissipation		IrefH	-	4.5	7.5	mA	VrefH =5V, VrefL=0V
			-	3.7	6.2	mA(*1)	Data condition:Maximum Current
D/A converter upper reference voltage range		VrefH	3.0	-	5	V	Reference voltage can not always be set to any value in this range, because it is restricted to the buffer amplifier output voltage range
D/A converter lower reference voltage range		VrefL	0	-	1.5	V	
Buffer amplifier output driver voltage range		VO	0.1	-	4.9	V	IO=±100μA
			0.2	-	4.75		IO=±1.0mA
Buffer amplifier output voltage range		IO	-2	-	2	mA	Upper saturation voltage=0.35V Lower saturation voltage=0.23V
Accuracy	Differential nonlinearity error	SDL	-1.0	-	1.0	LSB	VrefH=4.796V VrefL=0.7V VCC=5.5V (4mV/LSB) Without load (IO=+0mA)
	Nonlinearity error	SL	-3.5	-	3.5		
	Zero code error	SZERO	-25	-	25	mV	
	Full scale error	SFULL	-25	-	25		
Buffer amplifier output impedance		RO	-	5	15	Ω	
Pull-up I/O-cell internal R value		Rup	12.5	25	37.5	kΩ	Vin:0V (Resistance value alters by the applied voltage.)

*1 This is a value when the use of the power-on reset function, and CH1 ~ CH8 are specified for the maximum current setting.

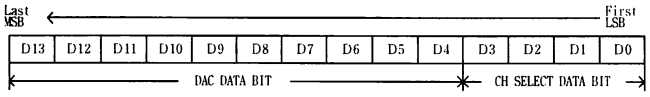
◇Timing characteristic (VCC=5V,VrefH=5V,VrefL=0V,Ta=25℃, unless otherwise noted)

Parameter	Symbol	Limits			Unit	Test conditions
		MIN.	TYP.	MAX.		The threshold voltage is 80%・20% of VCC
Reset "L" pulse width	tRTL	50	-	-	nS	
Clock "L" pulse width	tCKL	50	-	-		
Clock "H" pulse width	tCKH	50	-	-		
Clock rise time Clock fall time	tcr tcf	-	-	50		
Data set up time	tDCH	20	-	-		
Data hold time	tCHD	40	-	-		
LD set up time	tCHL	50	-	-		
LD hold time	tLDC	50	-	-		
LD "H" pulse duration	tLDH	50	-	-		
Data output delay time	tDO	-	-	90		CL=100pF
D/A output setting time	tLDD	-	7	20	μS	CL≦1000pF VO:0.5V⇔4.5V The time until the becomes the final value of 1/2 LSB.



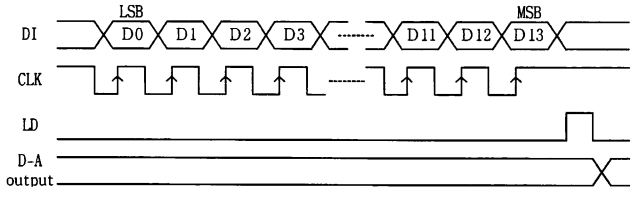
◇Command transmission

○ DIGITAL DATA FORMAT [Reverse=open or VCC short setting. (data : LSBfirst)]



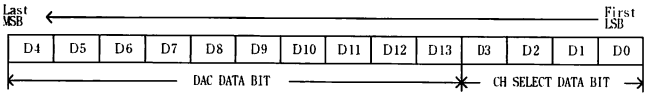
D3	D2	D1	D0	DAC selection
0	0	0	0	Don't Care
0	0	0	1	AO1 selection
0	0	1	0	AO2 selection
0	0	1	1	AO3 selection
0	1	0	0	AO4 selection
0	1	0	1	AO5 selection
0	1	1	0	AO6 selection
0	1	1	1	AO7 selection
1	0	0	0	AO8 selection
1	0	0	1	Don't Care
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

○ TIMING CHART(MODEL)



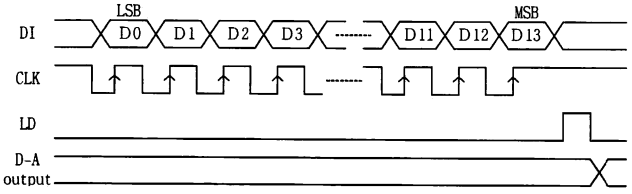
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D/A output (VrefH=VDD, VrefL=VSS)
0	0	0	0	0	0	0	0	0	0	VrefL
0	0	0	0	0	0	0	0	0	1	(VrefH-VrefL)/1024×1+VrefL
0	0	0	0	0	0	0	0	1	0	(VrefH-VrefL)/1024×2+VrefL
0	0	0	0	0	0	0	0	1	1	(VrefH-VrefL)/1024×3+VrefL
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	0	(VrefH-VrefL)/1024×1022+VrefL
1	1	1	1	1	1	1	1	1	1	(VrefH-VrefL)/1024×1023+VrefL

○ DIGITAL DATA FORMAT [Reverse=L setting. (data : MSBfirst)]



D3	D2	D1	D0	DAC selection
0	0	0	0	Don't Care
0	0	0	1	AO1 selection
0	0	1	0	AO2 selection
0	0	1	1	AO3 selection
0	1	0	0	AO4 selection
0	1	0	1	AO5 selection
0	1	1	0	AO6 selection
0	1	1	1	AO7 selection
1	0	0	0	AO8 selection
1	0	0	1	Don't Care
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

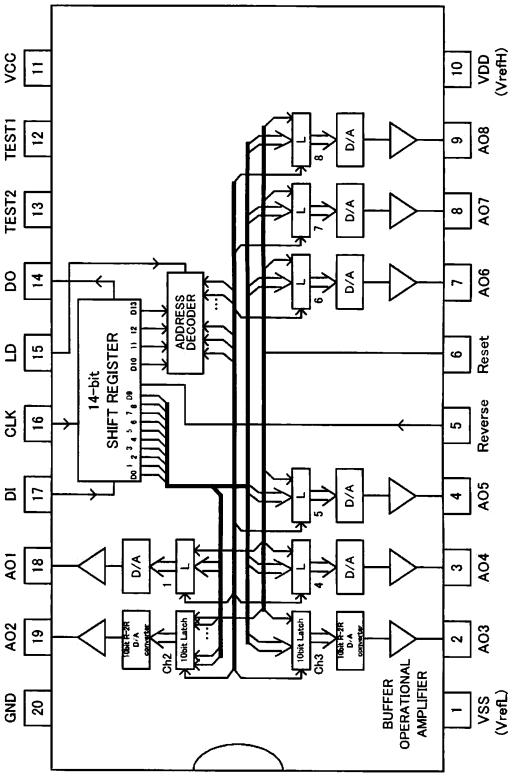
○ TIMING CHART(MODEL)



D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D/A output (VrefH=VDD, VrefL=VSS)
0	0	0	0	0	0	0	0	0	0	VrefL
1	0	0	0	0	0	0	0	0	0	(VrefH-VrefL)/1024×1+VrefL
0	1	0	0	0	0	0	0	0	0	(VrefH-VrefL)/1024×2+VrefL
1	1	0	0	0	0	0	0	0	0	(VrefH-VrefL)/1024×3+VrefL
:	:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1	1	(VrefH-VrefL)/1024×1022+VrefL
1	1	1	1	1	1	1	1	1	1	(VrefH-VrefL)/1024×1023+VrefL

◇Explanation Of Terminals / Block Diagram

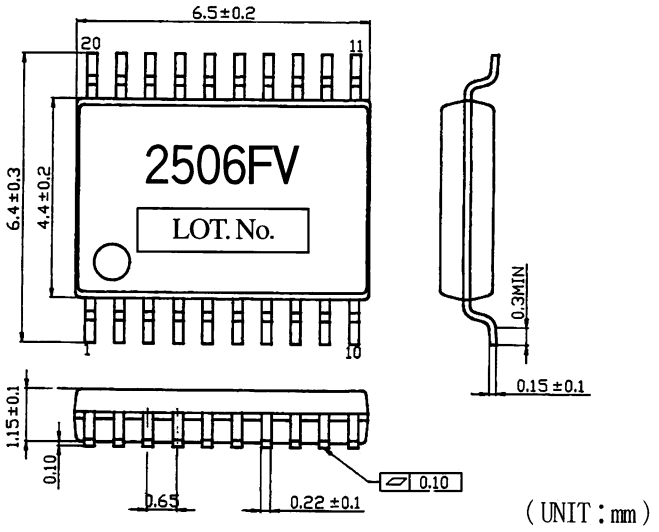
Pin No.	Symbol	Function
1	VSS	D/A converter lower reference voltage input terminal
2	AO3	10bit D/A converter output terminal (CH3)
3	AO4	10bit D/A converter output terminal (CH4)
4	AO5	10bit D/A converter output terminal (CH5)
5	Reverse	It is inverted about the data designation 10bit LSB and MSB.
6	Reset	The analog output of all channels is fixed for "L".
7	AO6	10bit D/A converter output terminal (CH6)
8	AO7	10bit D/A converter output terminal (CH7)
9	AO8	10bit D/A converter output terminal (CH8)
10	VDD	D/A converter upper reference voltage input terminal
11	VCC	Power supply terminal
12	TEST1	Terminal for test
13	TEST2	Terminal for test
14	DO	Terminal to output LSB data of 14-bit shift register
15	LD	When H-level signal is input to this terminal, the value stored in 14-bit shift register is loaded in decoder and D/A converter output register
16	CLK	Shift clock input terminal. Input signal at DI pin is input to 14-bit shift register at rise of shift clock pulse
17	DI	Serial data input terminal to input 14-bit long serial data
18	AO1	10bit D/A converter output terminal (CH1)
19	AO2	10bit D/A converter output terminal (CH2)
20	GND	GND terminal



Please use TEST1 terminal and TEST2 terminal in open condition.

Please refer to directions also when using it.

◇External Dimensions



(UNIT : mm)

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