

General Description

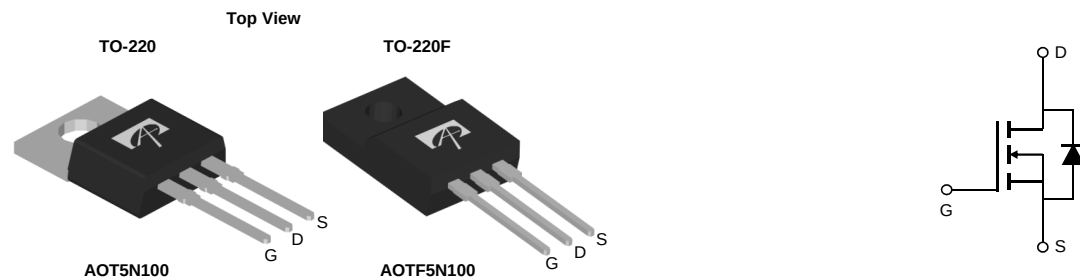
The AOT5N100 & AOTF5N100 are fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability this parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:
 AOT5N100L & AOTF5N100L

Product Summary

V_{DS}	1100@150°C
I_D (at $V_{GS}=10V$)	4A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 4.2Ω

100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	AOT5N100	AOTF5N100	Units
Drain-Source Voltage	V_{DS}	1000		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current	$T_C=25^\circ\text{C}$	4	4*	A
	$T_C=100^\circ\text{C}$	2.5	2.5*	
Pulsed Drain Current ^C	I_{DM}	15		A
Avalanche Current ^C	I_{AR}	2.8		A
Repetitive avalanche energy ^C	E_{AR}	117		mJ
Single pulsed avalanche energy ^G	E_{AS}	235		mJ
Peak diode recovery dv/dt	dv/dt	5		V/ns
Power Dissipation ^B	$T_C=25^\circ\text{C}$	195	42	W
	Derate above 25°C	1.6	0.3	W/°C
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300		°C

Thermal Characteristics

Parameter	Symbol	AOT5N100	AOTF5N100	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	°C/W
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.64	3	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	1000			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		1100		
BV _{DSS} /ΔT _J	Zero Gate Voltage Drain Current	I _D =250μA, V _{GS} =0V		1.04		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =1000V, V _{GS} =0V			1	μA
		V _{DS} =800V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3.3	3.9	4.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =2.5A		3.5	4.2	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =2.5A		5		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.73	1	V
I _S	Maximum Body-Diode Continuous Current				4	A
I _{SM}	Maximum Body-Diode Pulsed Current				15	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	750	950	1150	pF
C _{oss}	Output Capacitance		40	62	85	pF
C _{rss}	Reverse Transfer Capacitance		3.5	6	9	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	2	4.3	6.5	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =800V, I _D =5A	15	19	23	nC
Q _{gs}	Gate Source Charge			4.6		nC
Q _{gd}	Gate Drain Charge			6.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =500V, I _D =5A, R _G =25Ω		27		ns
t _r	Turn-On Rise Time			40		ns
t _{D(off)}	Turn-Off DelayTime			50		ns
t _f	Turn-Off Fall Time			33		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =5A, dI/dt=100A/μs, V _{DS} =100V	350	450	550	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5A, dI/dt=100A/μs, V _{DS} =100V	4.2	5.5	6.8	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=2.8A, V_{DD}=150V, R_G=25 Ω, Starting T_J=25° C

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

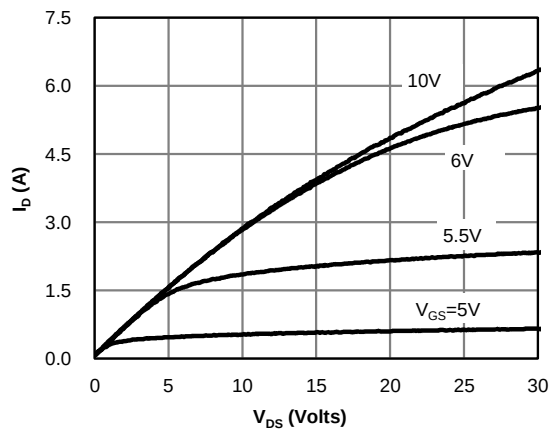


Fig 1: On-Region Characteristics

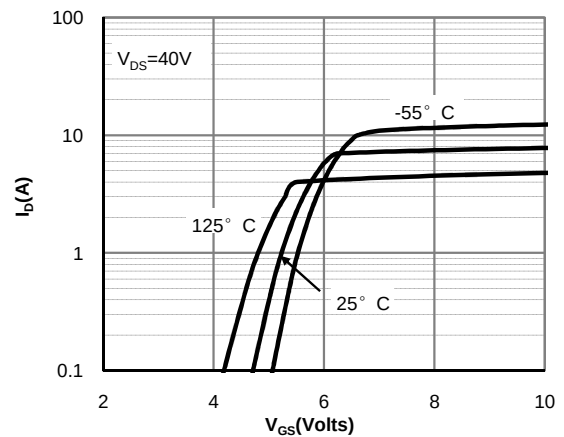


Figure 2: Transfer Characteristics

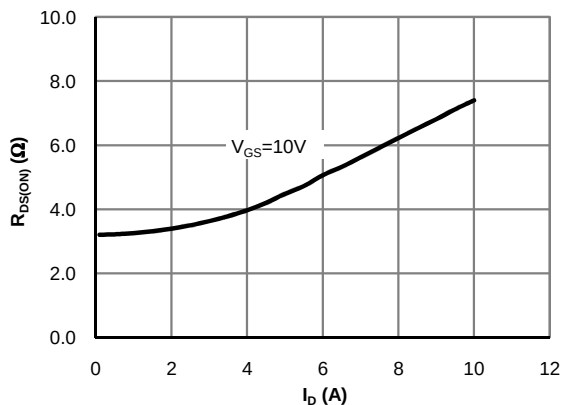


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

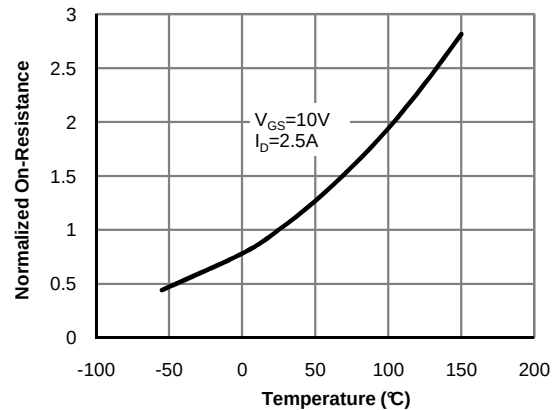


Figure 4: On-Resistance vs. Junction Temperature

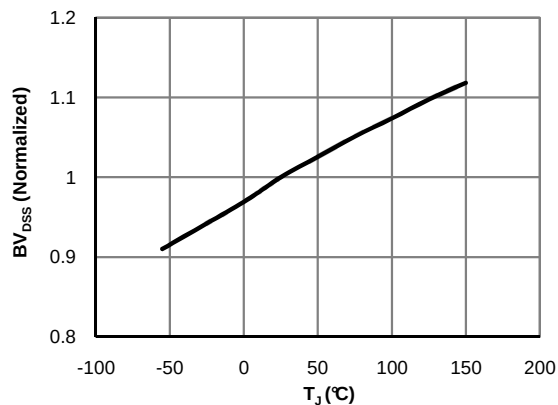


Figure 5: Break Down vs. Junction Temperature

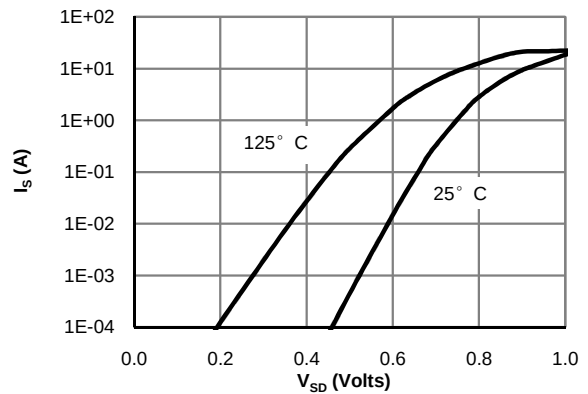


Figure 6: Body-Diode Characteristics (Note E)

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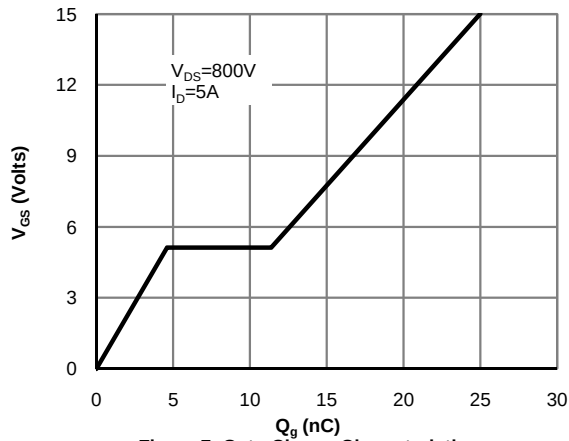


Figure 7: Gate-Charge Characteristics

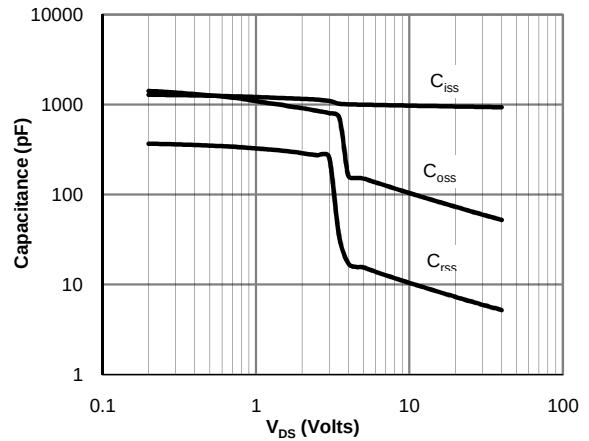


Figure 8: Capacitance Characteristics

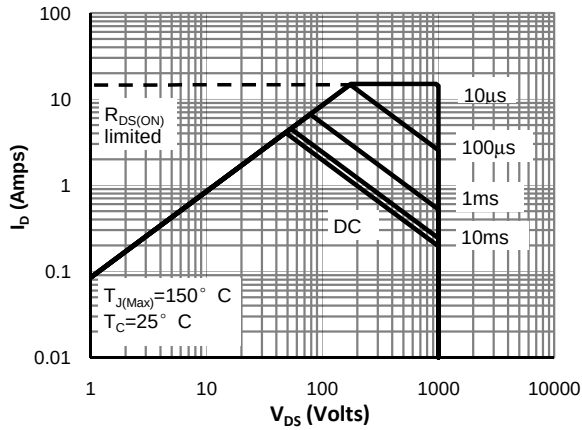


Figure 9: Maximum Forward Biased Safe Operating Area for AOT5N100 (Note F)

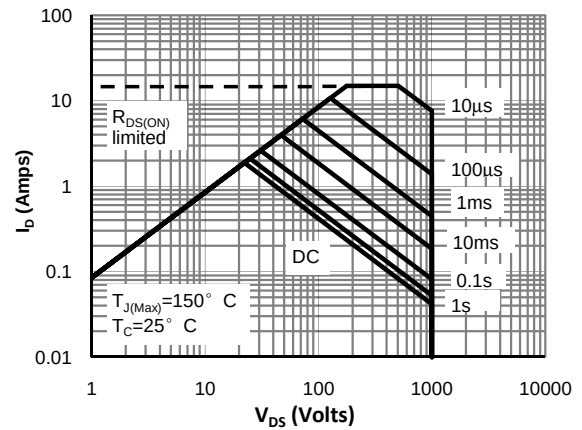


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF5N100 (Note F)

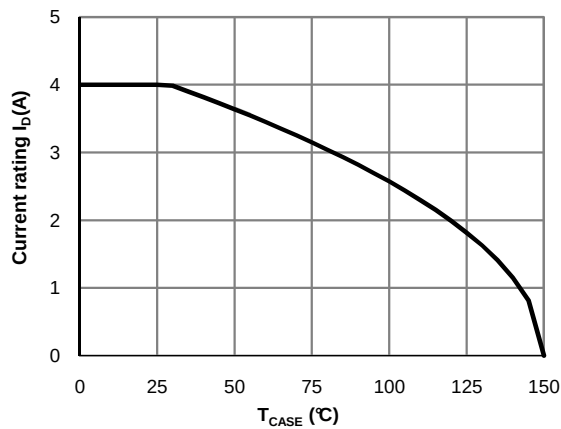


Figure 11: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

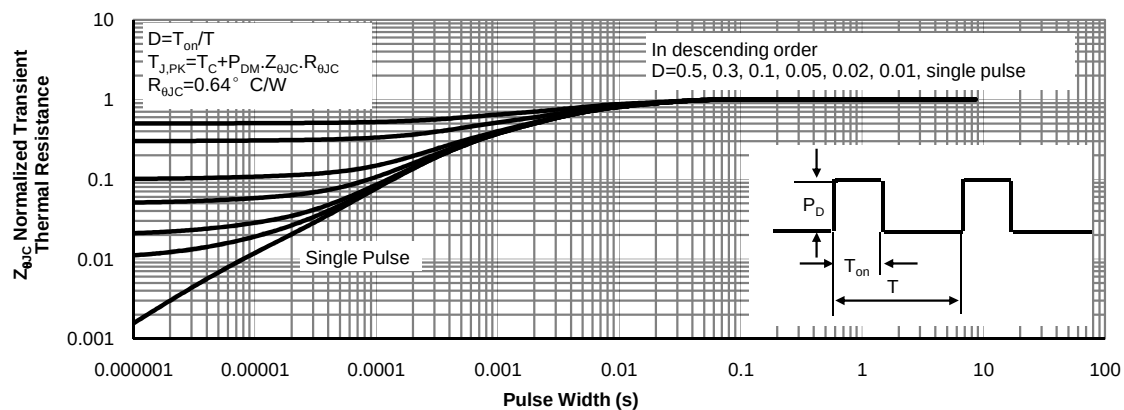


Figure 12: Normalized Maximum Transient Thermal Impedance for AOT5N100 (Note F)

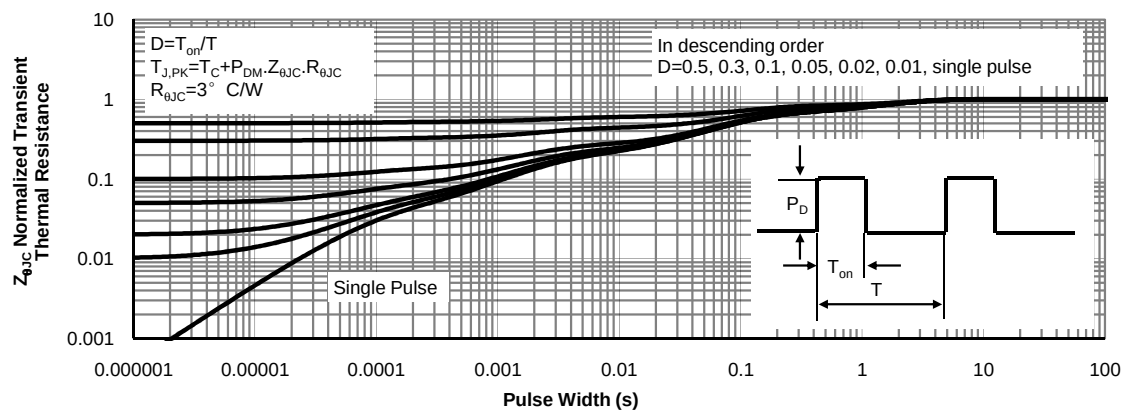
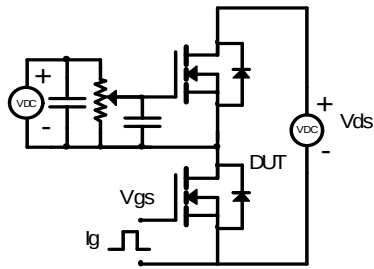
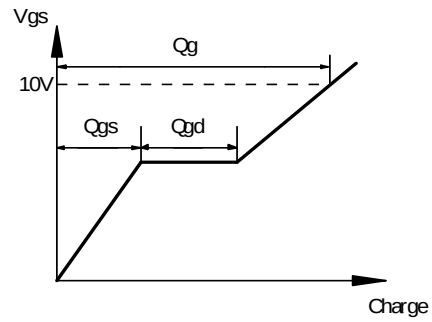
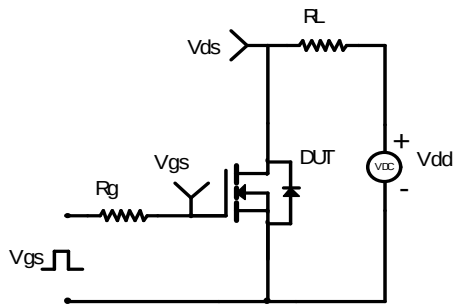
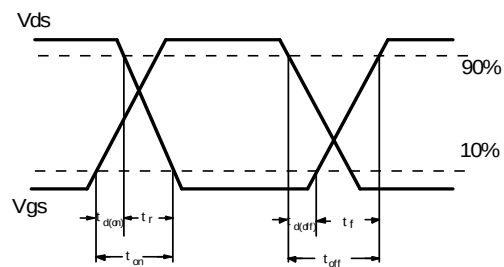


Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF5N100 (Note F)

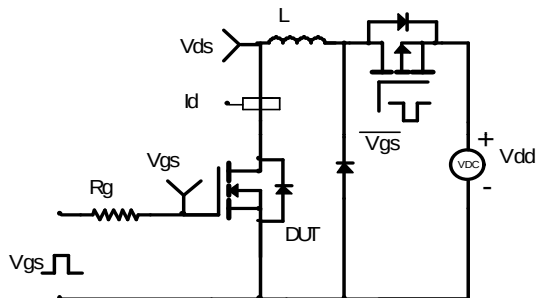
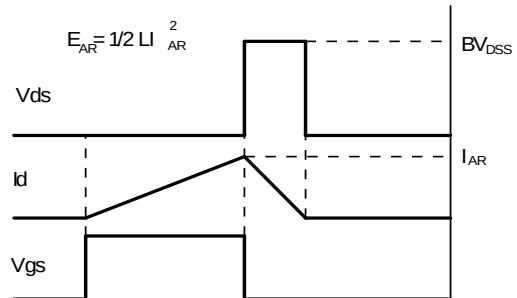
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

