NWK914D

PHY/PMD High Speed Copper Media Transceiver

Preliminary Information

DS4829 - 1.1 December 1997

The NWK914D is a Physical Layer device designed for use in 100BASE-TX applications. The NWK914D has integrated the 100mb/s transceiver, clock and data recovery and NRZI conversion circuitry. It is designed for use in cost effective NIC adapter cards and 100BASE-TX repeater and switch applications.

The device connects through a 5 bit symbol interface directly with any MAC controller that includes the PCS layer, resulting in a simple and cost effective solution. It will also interface with a PCS device such as the NWK935 to form a complete 100BASE-TX Physical Layer for connection to the IEEE 802.3 standard MII interface.

FEATURES

- Compatible with IEEE-802.3 Standards
- Operates over 100 Meters of STP and Category 5 UTP cable
- Five Bit TTL Level Symbol Interface
- Integrated Clock and Data Recovery
- Supports Full-duplex Operation
- Integral 10 Mb/s Buffer for Dual 10 Mb/s & 100 Mb/s Applications
- Adaptive Equalization
- 25MHz to 125MHz Transmit Clock Multiplier
- Programmable TX Output Current
- Base Line Wander Correction

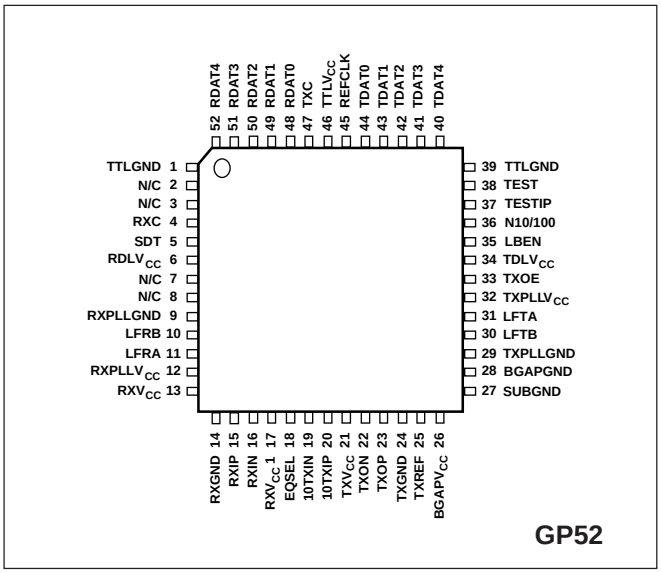


Fig.1 Pin connections - top view

- Single +5V supply
- 52 Pin PQFP package

ORDERING INFORMATION

NWK914D/CG/GP1N

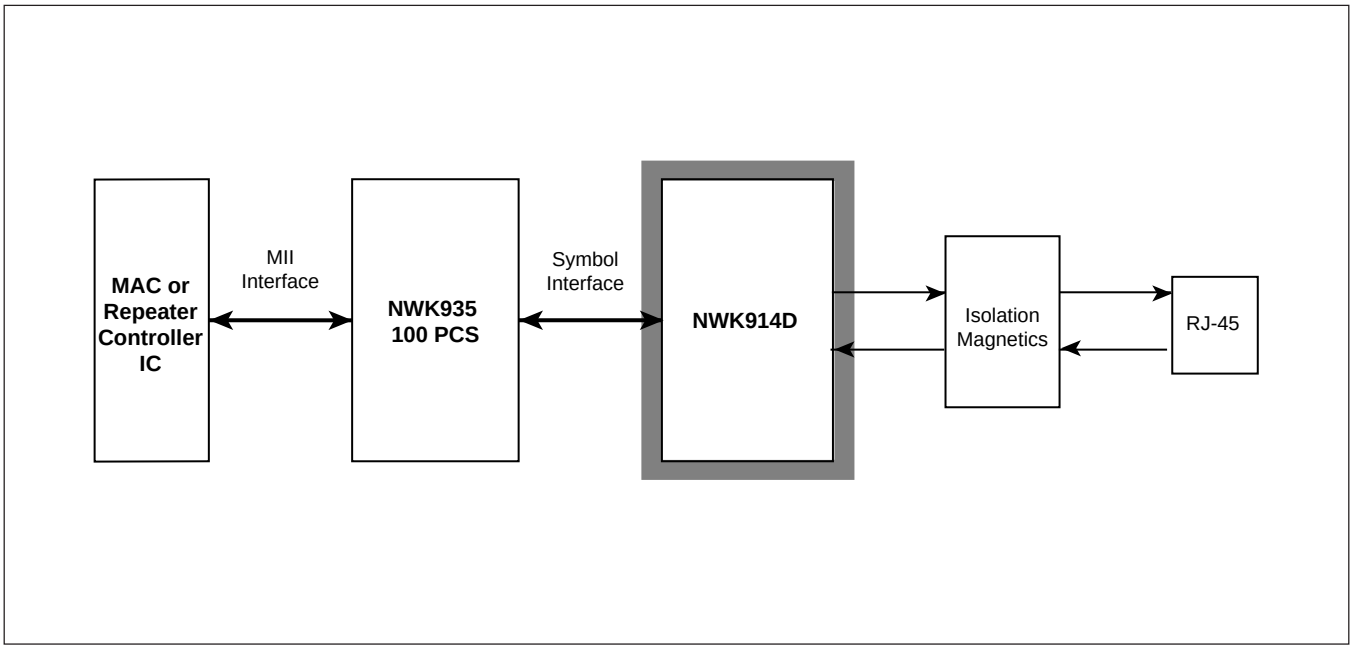


Fig.2 Simplified system diagram

ABSOLUTE MAXIMUM RATINGS

Operation at absolute maximum ratings is not implied. Exposure to stresses outside those listed could cause permanent damage to the device.

DC Supply voltage (V_{CC})	-0.5 to +7V
Storage temperature (tst)	-65 to +150°C
ESD	2kV HBM

RECOMMENDED OPERATING CONDITIONS

DC supply voltages (V_{CC})	+5V ±5%
Operating temperature (T_A)	0°C to +70°C (+25°C typ.)
Power dissipation (P_D)	750mW (typ.)

ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
DC characteristics						
Total V_{CC} supply current	I_{CC}	-	150	-	mA	device only
TTL high level I/P voltage	V_{IH}	2	-	-	V	
TTL low level I/P voltage	V_{IL}	-	-	0.8	V	
TTL high level I/P current	I_{IH}	-	-	20	µA	$V_{IH} = V_{CC}$
TTL low level I/P current	I_{IL}	-	-	–400	µA	$V_{IL} = 0.4V$
EQSEL high level I/P voltage	V_{IH}	4.2	-	-	V	
EQSEL low level I/P voltage	V_{IL}	-	-	0.8	V	
EQSEL floating level I/P	V_{IZ}	-	$V_{CC}/2$	-	V	
EQSEL high level I/P current	I_{IH}	-	-	1400	µA	$V_{IH} = V_{CC}$
EQSEL low level I/P current	I_{IL}	-	-	–1400	µA	$V_{IL} = 0V$
TTL high level O/P voltage	V_{OH}	2.4	-	-	V	$I_{OH} = 20µA$
TTL low level O/P voltage	V_{OL}	-	-	0.5	V	$I_{OL} = 4mA$
TTL high level O/P current	I_{OH}	-	-	–200	µA	
TTL low level O/P current	I_{OL}	-	-	4	mA	
Transmit O/P current pins TXOP, TXON		-	40	-	mA	$R_{REF} = 1300Ω$ 100Mb/s data
Differential RX I/P signal voltage		-	1.4	-	Vp-p	measured on device pins 100Mb/s data, 0mCable
RX I/P common mode voltage		-	$V_{CC}/2$	-	V	RX I/Ps floating
RX I/P impedance			-	24	-	kΩ
Signal detect threshold	V_{TH}	-	50	-	%	wrt normalized output of equalizer
Low voltage shutdown		-	3.8	-	V	
PLL characteristics						
3dB bandwidth	-	50	-	kHz		
Damping factor	-	2	-			
Peaking	-	-	.005	dB		
Overshoot	-	-	5	%		
Static error	-	±0.5	-	ns		
Jitter	-	-	0.5	ns		
VCO characteristics						
Centre frequency		-	125	-	MHz	
Deviation	-	±40	-	MHz		
Gain @125MHz	-	70	-	MHz/V		

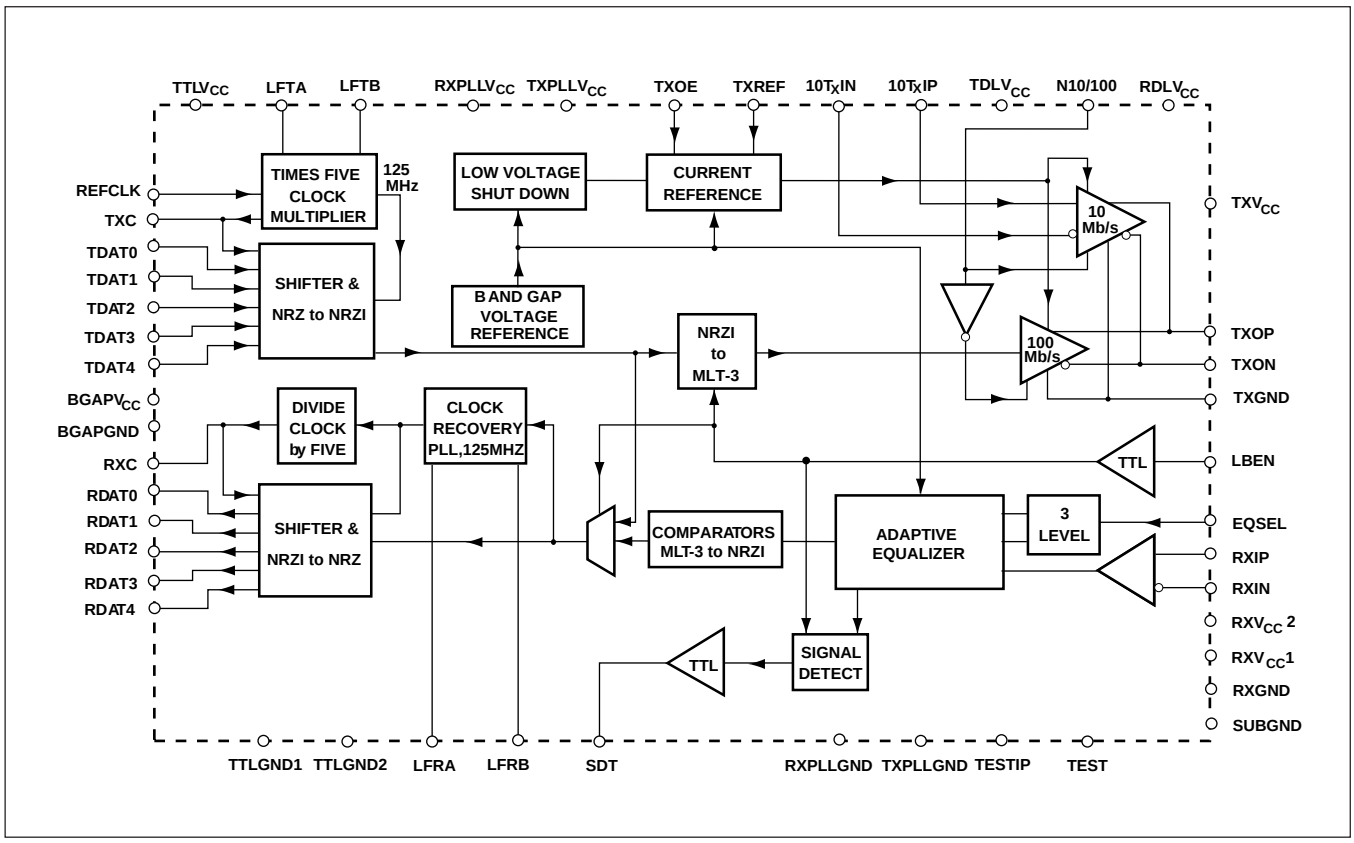


Fig.3 System block diagram

FUNCTIONAL DESCRIPTION

The functional blocks within the device are shown in Fig. 3. These are described below:-

Transmit Section

Times Five Clock Multiplier 25MHz to 125MHz

This circuit consists of a phase lock loop (PLL) that is operating at 125MHz, centre frequency. The 125MHz is divided by 5 to produce a 25MHz clock which is phase compared with a 25MHz crystal clock reference frequency which is input on pin REFCLK. The 25MHz clock (pin TXC) is then sent to the PCS layer to clock in in the 5 bit nibble data. Pins LFTA and LFTB are provided to set the VCO characteristics. The recommended loop filter components are shown in Fig.6.

A control current is derived from the clock multiplier and is used by the receive clock recovery circuit to centre the PLL when no input data is present.

Five Bit Nibble to 125MHz Shifter

Data is input to the transmit side in 5 bit wide parallel form on pins TDAT0 through TDAT4. This NRZ data is clocked in on the positive edge of the 25MHz clock pin TXC. The parallel data is first loaded into a 5 bit wide register prior to being loaded into a 5 bit PISO where it is converted into a serial data stream. The last stage of the shifter incorporates a converter to change the data from NRZ to NRZI.

NRZ to MLT3 Encoder

The serial data from the shifter then passes through an encoder which converts the NRZI binary data into the three level MLT-3 format for transmission by the 'TXO' outputs.

Transmit Line Drivers

There are two on-chip Line Drivers both of which share the output pins TXOP and TXON. The N10/100 pin is used to control which driver is active and allowed to drive the line. When held high the MLT-3 data is output by the 100Mb/s driver. This driver consists of differential current source outputs with programmable sink capability, designed to drive a nominal output impedance of 50Ω.

Output current is set by the value of an external resistor (R_{REF}) between pin 'TXREF' and 'TXGND'.

This resistor defines an internal reference current derived from an on-chip bandgap reference.

Final output current at the 'TXO' outputs is a multiple of this current and is defined as:-

$$I_{TXO}(mA) = 52/R_{REF}(k\Omega)$$

Transition times of the 'TXO' outputs are matched and internally limited to approx. 2.5ns to reduce EMI emissions.

When N10/100 is held low the 10Mb/s driver is selected. This 10Mb/s driver consists of a differential analog buffer designed to take a fully cable conditioned 10Mb/s signal from the filter output of existing 10BASE-T electronics. The 10BASE-T signal is input on pins 10TXIN and 10TXIP. The output current of the buffer is determined by the same external R_{REF} resistor on pin TXREF as used for the 100Mb/s driver.

The unselected driver is switched to a tristated power save mode. A low voltage shutdown circuit turns off both TX drivers when V_{CC} voltage falls to a level below the specified minimum.

When operating in single 100Mb/s applications a 1:1 turn ratio magnetics will be used and therefore to attain the desired line driving current of 40mA out of the secondary a TXO output drive of 40mA is required. Using the above formula it will be found that 1.3Ω is the nearest prefered value to that required to give the 40mA.

In the case of dual 10Mb/s and 100Mb/s applications a 2:1 turn ratio magnetics is recommended. The use of 2:1 magnetics enables a greater efficiency to be gained from the 10Mb/s driver by using a lower output current. At the same time this lower current is also true of the 100Mb/s output where now only a 20mA drive is required. An R_{REF} value of 2.6KΩ is used to set this current. Internal current ratioing within the device will ensure that the correct drive current is chosen depending upon whether the drives are in 10Mb/s or 100Mb/s mode as selected by pin N10/100.

The R_{REF} value can be adjusted to compensate for different magnetics and board layouts. The object is to achieve an output level of 2V p-p measured at the RJ45 socket in compliance with 802.3.

When the TXOE pin is held low the TXdrivers are tri-stated regardless of the mode selected by the N10/100 pin.

Receiver Section

Equalizer

The equalizer circuit is necessary to compensate for signal degradation due to cable losses, however over-equalization must be avoided to prevent excessive overshoots resulting in errors during the reception of MLT-3 data. Three operating modes are therefore provided.

These three operating modes are controlled by the state of tristate input 'EQSEL' and are described below:-

1) Auto Equalization ('EQSEL' floating)

Fully automatic equalization is achieved through the use of a feedback loop driven by a control signal derived from the signal amplitude. This provides adaptive control and prevents over-modulation of the signal when short cable lengths are used.

2) Full Equalization ('EQSEL' low)

In this mode, full equalization is applied to the input signal irrespective of amplitude.

3) No Equalization ('EQSEL high)

The equalization circuit is disabled completely during this mode.

Base Line Wander Correction

MLT-3 codes have significant low frequency components in their spectrum which are not transmitted through the transformers that couple the line to the board. This results in 'Base Line Wander', which can significantly reduce the noise immunity of the receiver.

The purpose ot the correction circuit is to restore these low frequency components through the use of a feedback arrangement. The circuit will also correct any DC offset that may exist on the receive signal.

Signal Detector

A signal detect circuit is provided which continuously monitors the amplitude of the input signal being received on pins RXIP and RXIN. After the input signal reaches the specified level which the equalizer can correctly equalize, SDT is asserted high. Conversely if the signal level falls below a limit for reliable operation then SDT will go low.

Comparators MLT-3 to NRZ Decoder

The equalized MLT-3 data is then passed to a set of window comparators which are used to determine the signal level. The comparator outputs are OR'ed together to reconstitute the NRZI data.

PLL Clock Recovery

This function consists of a 125MHz PLL that is locked to the incoming data stream. The PLL is first centred to the transmit clock multiplier using an internal analog reference signal. Once a valid input signal is present, the PLL will lock to, and thus extract the clock from, the incoming data stream. Pins LFRA and LFRB are provided to set the VCO characteristics. The recommended loop filter components are shown in Fig.6.

125MHz Shifter to Parallel Data

The 125Mb/s serial data stream with an accompanying phase related 125MHz clock is output from the PLL.

This data stream is clocked into the serial to parallel register using the 125MHz clock. This data is then latched prior to being clocked out on pins RDAT0 to RDAT4. A 25MHz clock, derived from the 125MHz PLL by a divide by 5, is used to clock the parallel data and is output to pin RXC.

Loopback Logic

Pin 'LBEN' controls loopback operation. A low level on this pin defines normal operation, a high level defines loopback mode. In loopback mode, the transmit data is internally routed to the receive circuitry, SDT is forced high and the TXOP and TXON outputs are disabled.

Test Pins and No-Connects

Two pins are provided on the product to aid testing in production. These pins TEST(38), and TESTIP(37) must be left unconnected for normal operation in application circuits.

Additionally, there are four No-Connect pins (2,3,7,8) which also mustt be left unconnected for normal operation.

AC CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Waveform Timing	Value Min.	Value Typ.	Value Max.	Units	Conditions
AC characteristics						
100Mb/s TX driver outputs rise/fall times pins TXOP, TXON		-	2.5	-	ns	100Ω differential load measured at RJ45
REFCLK frequency	1	-	25	-	MHz	
REFCLK tolerance	2	-	100	-	ppm	
REFCLK M/S ratio	3	40:60	-	60:40	%	
REFCLK to TXC propagation delay	4	5	-	13	ns	Tx PLL in lock
TDAT0 → 4 to TXC setup time	5	12	-	-	ns	
TDAT0 → 4 to TXC hold time	6	0	-	-	ns	
RDAT0 → 4 valid to RXC +Ve edge	7	10	-	-	ns	
RXC to RDAT0 → 4 invalid	8	10	-	-	ns	
RXC M/S ratio	9	45:55	-	55:45	%	
REFCLK to SDT transition		5	-	15	ns	

NOTE: Conditions for AC Characteristics:
All AC measurementsare made at aV_{th} + 1.5V and with TTL output loaded with 25pf

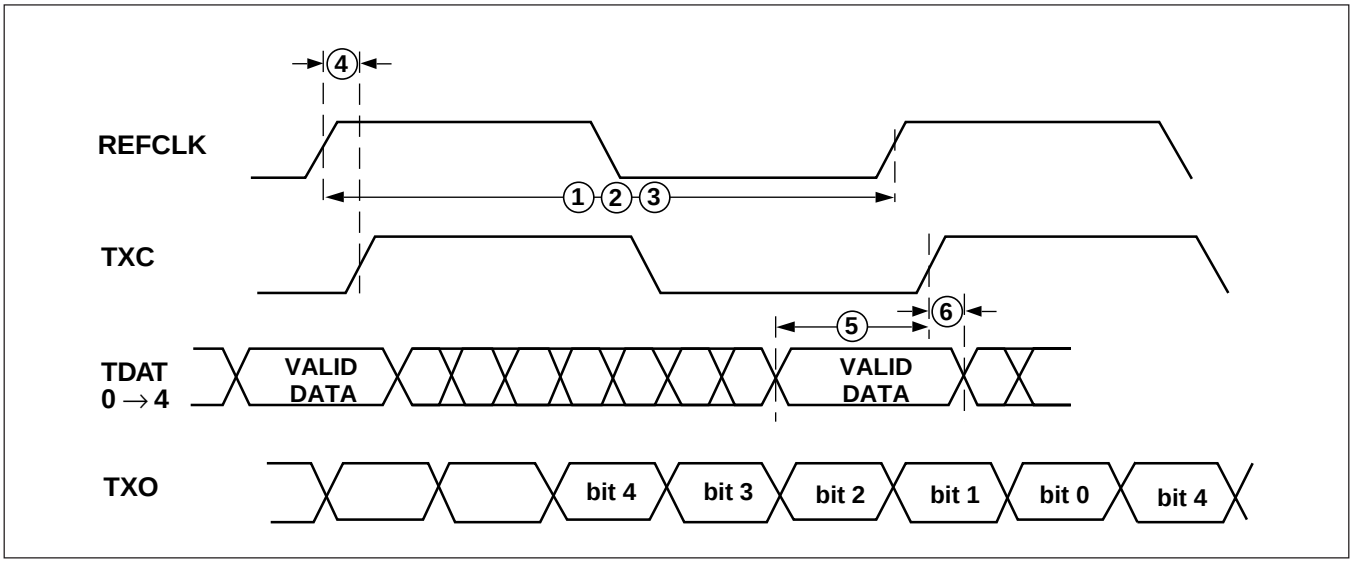


Fig.4 Transmit timing waveform

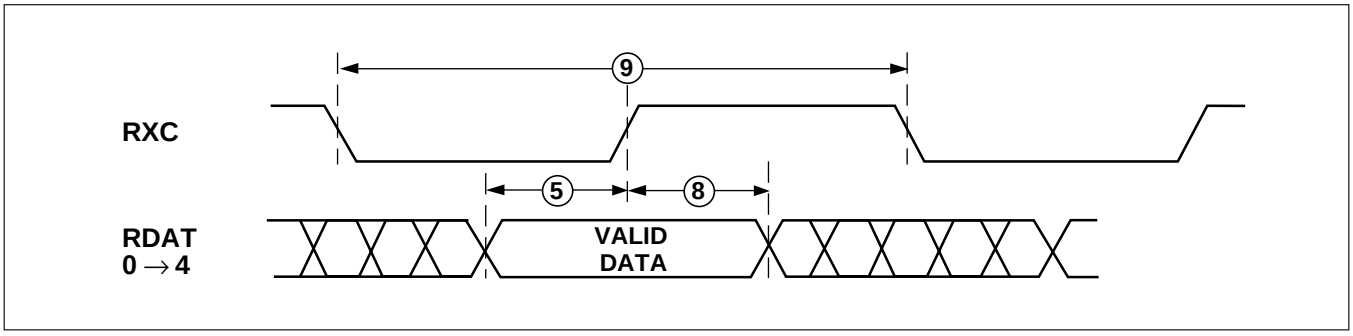


Fig.5 Receive timing waveform

Pin Name	Pin Type	Pin Number	Pin Description
SYMBOL Interface			
RXC	TTLOP	4	25MHz recovered receive clock. This is aligned with and used to clock out the 5 bit parallel receive data to the PCS layer.
SDT	TTLOP	5	Signal detect output. This output is high when an input signal of sufficient amplitude is detected on the RXI inputs.
TDAT4	TTLIP	40	The 100BASE-TX transmit input bit 4
TDAT3	TTLIP	41	The 100BASE-TX transmit input bit 3
TDAT2	TTLIP	42	The 100BASE-TX transmit input bit 2
TDAT1	TTLIP	43	The 100BASE-TX transmit input bit 1
TDAT0	TTLIP	44	The 100BASE-TX transmit input bit 0
TXC	TTLOP	47	25MHz transmit clock. This is aligned with and used to clock in the 5 bit parallel 100BASE-TX transmit data from the PCS layer.
RDAT0	TTLOP	48	The 100BASE-TX receive output bit 0
RDAT1	TTLOP	49	The 100BASE-TX receive output bit 1
RDAT2	TTLOP	50	The 100BASE-TX receive output bit 2
RDAT3	TTLOP	51	The 100BASE-TX receive output bit 3
RDAT4	TTLOP	52	The 100BASE-TX receive output bit 4
Network Interface			
RXIP	analog input	15	+ Differential receive signal input from magnetics
RXIN	analog input	16	– Differential receive signal input from magnetics
TXON	analog output	22	– Differential transmit line driver outputs to magnetics
TXOP	analog output	23	+ Differential transmit line driver outputs to magnetics
10BASE-T Interface			
10TXIN	analog input	19	The filtered 10BASE-T transmit input (–)
10TXIP	analog input	20	The filtered 10BASE-T transmit input (+)
Control Pins			
N10/100	TTLIP	36	10/100 mode selection. A low selects the 10BASE-T mode and enables the data on pins 10TXIP/N to be outut on the TXOP/N pins. A high selects the 100BASE-TX mode, enabling the 100Mb/s drivers.
EQSEL	3 level IP	18	Mode select input for equalizer. Normally this pin is left unconnected (floating) for auto-eq. mode. High selects minimum equalization. Low selects full equalization.
LBEN	TTLIP	35	Loopback enable input. A high on this pin selects the loopback mode and low selects normal operation.
TXOE	TTLIP	33	Transmit output enable. A high on this pin selects normal operation. A low on this pin puts both of the TX drivers in tri-state mode.
TESTIP	test	37	Test pin. This pin must be left unconnected for proper operation.
TEST	test	38	Test pin. This pin must be left unconnected for proper operation.
N/C		2,3,7,8	No connection. This pin must be left unconnected for proper operation.
Component Connections			
REFCLK	TTLIP	45	25MHz clock input. An external 25MHz oscillator is input to this pin.
TXREF	analog input	25	TXOP/N line driver current setting pin. Connects to TXGND through a resistor.
LFRB	analog	10	Differential loop filter pin for receive PLL (see fig.6)
LFRA	analog	11	Differential loop filter pin for receive PLL (see fig.6)
LFTB	analog	30	Differential loop filter pin for transmit clock PLL (see fig.6)
LFTA	analog	31	Differential loop filter pin for transmit clock PLL (see fig.6)
Power			
TTLGND	Power	1,39	GND for TTL logic I/Os
$RDLV_{CC}$	Power	6	+5V supply to receive logic
RXPLLGND	Power	9	GND to receive PLL
$RXPLLV_{CC}$	Power	12	+5V supply to receive PLL
$RXV_{CC}2$	Power	13	+5V supply to adaptive equalizer and QFB circuits
RXGND	Power	14	GND to to adaptive equalizer and QFB circuits
$RXV_{CC}1$	Power	17	+5V supply to MLT-3 to NRZI converter
TXV_{CC}	Power	21	+5V supply to transmit line driver circuits
TXGND	Power	24	GND to transmit line driver circuits
RXV_{CC}	Power	26	+5V supply to on-chip bandgap reference
SUBGND	Power	27	Chip substrate GND connection
BGAPGND	Power	28	GND to on-chip bandgap reference
TXPLLGND	Power	29	GND to to transmit clock-multiplier PLL
$TXPLLV_{CC}$	Power	32	+5V supply to transmit clock-multiplier PLL
$TDLV_{CC}$	Power	34	+5V supply to transmit logic
$TXLV_{CC}$	Power	46	+5V supply to TTL logic I/Os

Table 1: Pin descriptions

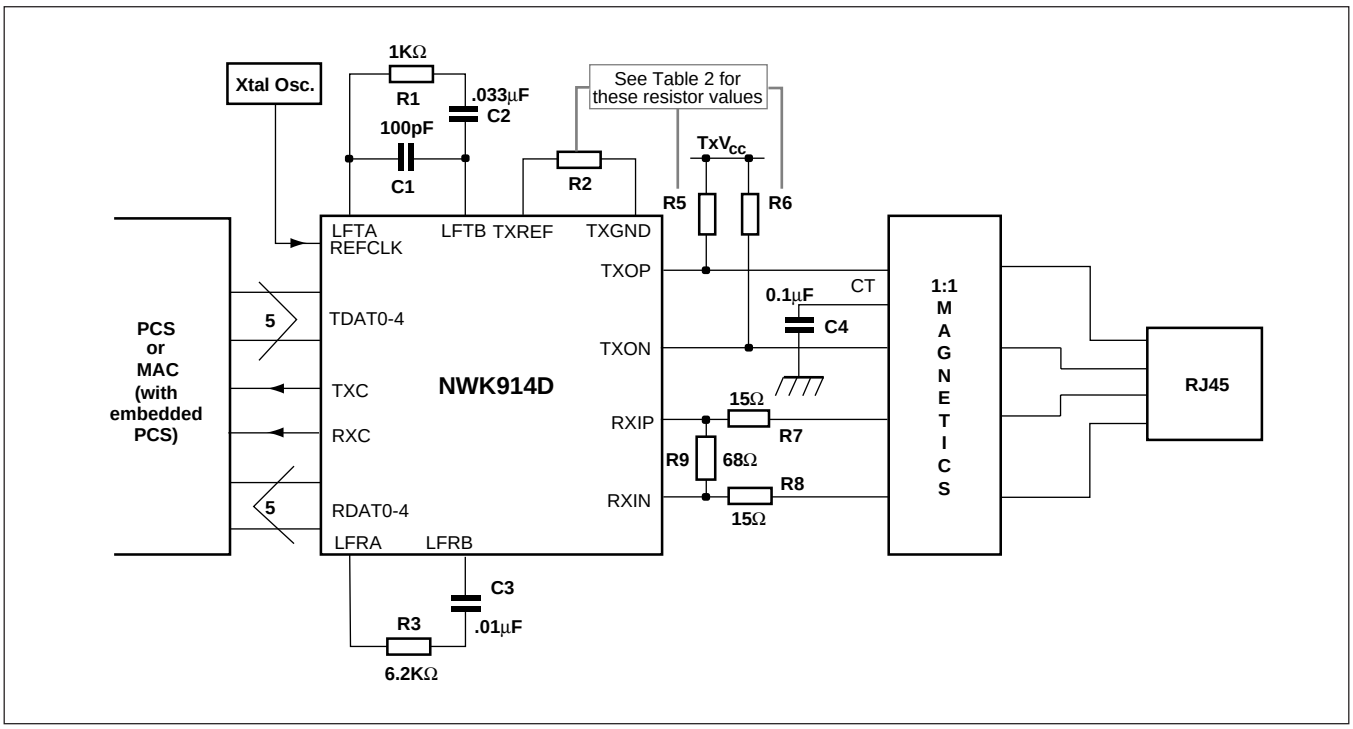


Fig.6 Simplified 100BASE-TX system block diagram showing NWK914D external components

REF.	VALUE	TOL.	FUNC.	NOTES
C1	100pF	20%	loop fltr	
C2	0.033µF	20%	loop fltr	
C3	.01µF	20%	loop fltr	
R1	1KΩ	1%	loop fltr	
R2	1300Ω	1%	tx ref	1:1 magnetics
R3	6.2KΩ	1%	loop fltr	
R5,R6	50Ω	1%	xmit	1:1 magnetics
R7,R8	15Ω	1%	rcv pad	
R9	68Ω	1%	rcv pad	
R2	2.6KΩ	1%	tx ref	2:1 magnetics
R5,R6	200Ω	1%	xmit	2:1 magnetics
CT on transformer connects directly to TX V_{CC} with C4 omitted				2:1 magnetics

Table 2: External components

EXTERNAL REQUIREMENTS

The NWK914D requires a number of external components for the device to function correctly and these are shown in the simplified 100BASE-TX application circuit in Fig.6 and the component value information given in Table 2.

Note that the values of R2, R5 and R6 vary depending upon application. When using 1:1 magnetics, use the values shown in the middle of Table 2 with note "1:1 magnetics". When using 2:1 magnetics use the values shown in the last two lines of Table 2. Please refer to the Transmit Line Driver section on pages 3-4 for more information on these values.

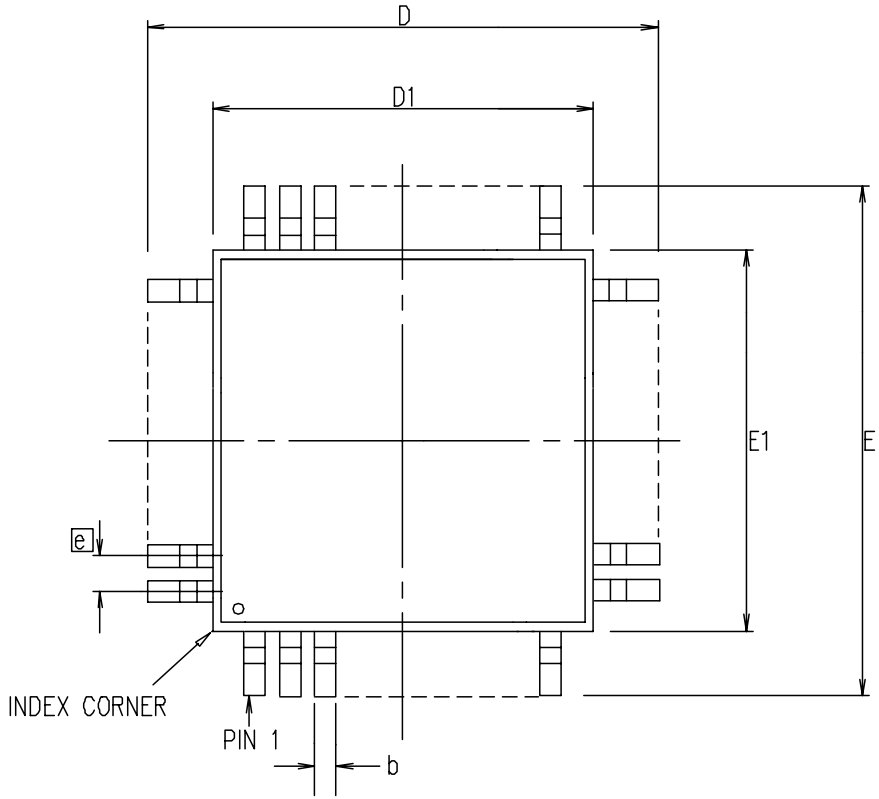
For more detailed Application information please contact your local Sales Office.

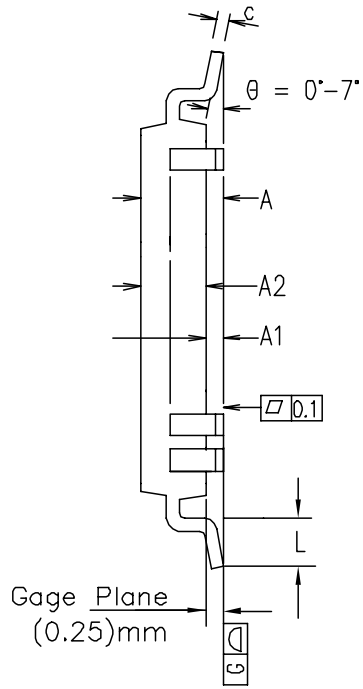
GLOSSARY OF TERMS AND ABREVIATIONS

MAC	Media Access Control
MLT-3	Multi Level Transmit -3 levels
NRZ	Non Return To Zero
NRZI	Non Return to Zero Inverse
PCS	Physical Coding Sublayer
PHY	PHYsical Layer
PLL	Phase Locked Loop
PMD	Physical Media Dependent
UTP	Unshielded Twisted Pair
RX	Receive
STP	Shielded Twisted Pair
TX	Transmit
UTP	Unshielded Twisted Pair
VCO	Voltage Controlled Oscillator

	NWK914B	NWK914S	NWK914D
Base Line Wander Correction	-	improved to 100m	improved to 100m
TXREF resistor with 1:1 magnetics	620Ω	680Ω	1300Ω

Table 3: Differences between NWK914B, NWK914S and NWK914D





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	–	2.45		–	0.096
A1	0.00	0.25		0.000	0.010
A2	1.80	2.20		0.071	0.087
D	13.20 BSC			0.520 BSC	
D1	10.00 BSC			0.394 BSC	
E	13.20 BSC			0.520 BSC	
E1	10.00 BSC			0.394 BSC	
L	0.73	1.03		0.029	0.041
e	0.65 BSC.			0.026 BSC.	
b	0.22	0.40		0.009	0.016
c	0.11	0.23		0.004	0.009
	Pin features				
N	52				
ND	13				
NE	13				
NOTE	SQUARE				

Conforms to JEDEC MS-022 AC Iss. B

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.010 mm max.

ORIGINATING SITE: SWINDON

ISSUE	1	2	3	4	
ACN	202049	204614	205254	207058	
DATE	20FEB97	22MAY98	25SEP98	30JUN99	
APPD.					

MITEL SEMICONDUCTOR

Title: Package Outline Drawing for 52L MQFP (GP) (10x10x2.0) mm, Body+3.2 mm

Drawing Number

GPD00300

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