140Mb/s Bi-directional Level Translator for Push-Pull Applications

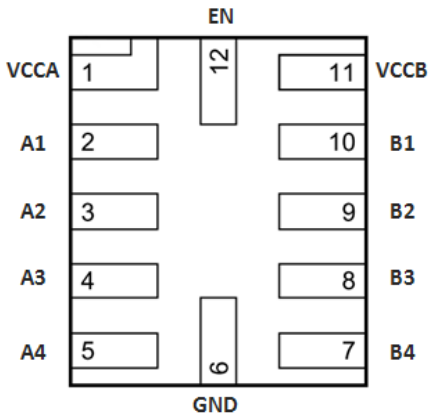
Features

- 0.85V to 2.7V on A Port and 1.35V to 3.6V on B Port
- VCCA may be greater than, equal to, or less than VCCB
- High-Speed with 140 Mb/s Guaranteed Date Rate
- 100 pF Capacitive Drive Capability
- Low Bit-to-Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non-preferential Power-Up Sequencing
- Power-Off Protection
- Package: UQFN1.7x2.0-12L

Applications

- Mobile Phones, PDAs
- Other Portable Devices

Pin Configuration



UQFN2.0*1.7-12L (Top View)

Description

The PI4ULS3V304 is a 4-bit configurable dual-supply autosensing bidirectional level translator that does not require a direction control pin. The B and A ports are designed to track two different power supply rails, VCCB and VCCA respectively.

The PI4ULS3V304 offers the feature that the values of the VCCB and VCCA supplies are independent. Design flexibility is maximized because VCCA can be set to a value either greater than or less than the VCCB supply.

The PI4ULS3V304 has high output current capability, which allows the translator to drive high capacitive loads such as most high frequency EMI filters. Another feature of the PI4ULS3V304 is that each An and Bn channel can function as either an input or an output.

An Output Enable (EN) input is available to reduce the power consumption. The EN pin can be used to disable both I/O ports by putting them in 3-state which significantly reduces the supply current.

The PI4ULS3V304 is 2 kV System-Level ESD Capable.

Pin Description

Pin No.	Pin Name	Type	Description
1	V_{CCA}	Power	A-port supply voltage.0.85V ⩽ VCCA ⩽ 2.7 V
2	A1	I/O	Input/output A. Referenced to VCCA.
3	A2	I/O	Input/output A. Referenced to VCCA
4	A3	I/O	Input/output A. Referenced to VCCA.
5	A4	I/O	Input/output A. Referenced to VCCA
6	GND	GND	Ground.
7	B4	I/O	Input/output B. Referenced to VCCB
8	B3	I/O	Input/output B. Referenced to VCCB
9	B2	I/O	Input/output B. Referenced to VCCB
10	B1	I/O	Input/output B. Referenced to VCCB
11	V_{CCB}	Power	B-port supply voltage.1.35 V ⩽ VCCB ⩽ 3.6 V
12	EN	Input	Output enable (active High). Pull EN low to place all outputs in 3-state mode.

Block Diagram

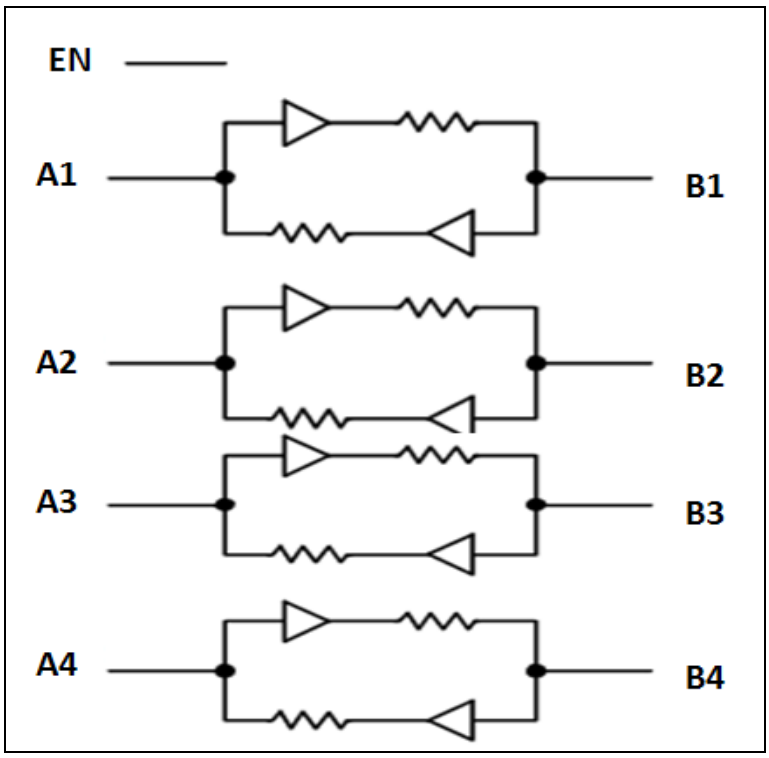


Figure 1: Block Diagram

Maximum Ratings

Storage Temperature ..... -65°C to +150°C
DC Supply Voltage port B..... -0.5V to +4.6V
DC Supply Voltage port A ..... -0.5V to+3.6V
Vi(A) referenced DC Input / Output Voltage..... -0.5V to +3.6V
Vi(B) referenced DC Input / Output Voltage..... -0.5V to+4.6V
Enable Control Pin DC Input Voltage..... -0.5V to+3.6V
DC Input Diode Current(V_I<GND)..... -50mA
DC Output Diode Current(V_O<GND)..... -50mA
DC Supply Current through V_{CCB} ..... ±100mA
DC Supply Current through V_{CCA} ..... ±100mA
DC Ground Current through Ground Pin ..... ±100mA

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{CCA}	A-side Positive DC Supply Voltage		0.85	-	2.7	V
V_{CCB}	B-side Positive DC Supply Voltage		1.35	-	3.6	V
V_I	Enable Control Pin Voltage		GND	-	2.7	V
V_{IO}	Bus Input/Output Pin Voltage	I/O A	GND	-	2.7	V
		I/O B	GND	-	3.6	V
T_A	Operating Temperature Range		-40	-	+85	℃
At/Av	Input Transition Rise or Rate, V_I, V_{IO} from 30% to 70% of V_{CC}; V_{CC}= 3.3 V ± 0.3 V		0	-	10	ns

DC Electrical Characteristics

Sym	Parameter	Test Conditions[*1]	V_{CCB}[*2] (V)	V_{CCA}[*3] (V)	-40 ℃ to +85 ℃			Unit
					Min	Typ[*4]	Max	
V_{IHB}	B port Input HIGH Voltage	-	1.35-3.6	0.85-2.7	2/3*V_{CCB}	-	-	V
V_{ILB}	B port Input LOW Voltage	-	1.35-3.6	0.85-2.7	-	-	1/3* V_{CCB}	V
V_{IHA}	A port Input HIGH Voltage	-	1.35-3.6	0.85-2.7	2/3*V_{CCA}	-	-	V
V_{ILA}	A port Input LOW Voltage	-	1.35-3.6	0.85-2.7	-	-	1/3 * V_{CCA}	V
V_{IH}	Control Pin Input HIGH Voltage	T_A = +25 ℃	1.35-3.6	0.85-2.7	2/3*V_{CCA}	-	-	V
V_{IL}	Control Pin Input LOW Voltage	T_A = +25 ℃	1.35-3.6	0.85-2.7	-	-	1/3 * V_{CCA}	V
V_{OHB}	B port Output HIGH Voltage	B port source current = 20 μA	1.35-3.6	0.85-2.7	0.9*V_{CCB}	-	-	V
V_{OLB}	B port Output LOW Voltage	B port sink current = 20 μA	1.35-3.6	0.85-2.7	-	-	0.2	V
V_{OHA}	A port Output HIGH Voltage	A port source current= 20 μA	1.35-3.6	0.85-2.7	0.9*V_{CCA}	-	-	V
V_{OLA}	A port Output LOW Voltage	A port sink current = 20 μA	1.35-3.6	0.85-2.7	-	-	0.2	V
I_{QVB}	V_{CCB} Supply Current	EN = V_{CCA},I_O = 0A, (I/O_B= 0V or V_{CCB}, I/O_A= float) or (I/O_B = float, I/O_A = 0V or V_{CCA})	1.35-3.6	0.85-2.7	-	0.2	1.5	μA
I_{QVA}	V_{CCA} Supply Current		1.35-3.6	0.85-2.7	-	0.1	1	μA
I_{TS-B}	B port Tristate Output Mode Supply Current	T_A=+25 ℃, EN=0V (I/O_B = 0V or V_{CCB}, I/O_A = float) or (I/O_B = float, I/O_A = 0V or V_{CCA})	1.35-3.6	0.85-2.7	-	0.2	1.5	μA
I_{TS-A}	A port Tristate Output Mode Supply Current		1.35-3.6	0.85-2.7	-	0.1	1	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	T_A= +25 ℃, EN= 0V	1.35-3.6	0.85-2.7	-	-	±1	μA
I_I	Control Pin Input Current	T_A = +25 ℃	1.35-3.6	0.85-2.7	-	-	±1	μA
I_{OFF}	Power Off Leakage Current	I/O_B = 0 to 3.6V, I/O_A = 0 to 2.5V	0	0	-	-	2	μA
			1.35-3.6	0	-	-	2	
			0	0.85-2.7	-	-	2	

Note:

1. Normal test conditions are V_I = 0V, $C_{IOB} \leq$ 15pF and $C_{IOA} \leq$ 15pF, unless otherwise specified.
2. V_{CCB} is the supply voltage associated with the I/O B port, and B range from +1.35 V to 3.6 V under normal operating conditions.
3. V_{CCA} is the supply voltage associated with the I/O A port, and A range from +0.85 V to 2.7V under normal operating conditions.
4. Typical values are for V_{CCB} = +2.8V, V_{CCA} = +1.8V and T_A = +25 ℃. All units are production tested at T_A = +25 ℃. Limits over the operating temperature range are guaranteed by design.
5. When VCCA <1.0V, VIH is 0.75*V_{CCA} (Min), VIL is 0.25*V_{CCA} (Max)

Timing Characteristics

Sym	Parameter	Test Conditions[*1]	V_{CCB}[*2] (V)	V_{CCA}[*3](V)	-40 ℃ to +85 ℃			Unit
					Min	Typ[*4]	Max	
t_{R-B}	B port Rise Time	C_{IOB} = 15 pF	1.35-2.5	0.85-2.7	-	3	8	ns
			2.5-3.6	0.85-2.7	-	0.8	4	
t_{F-B}	B port Fall Time	C_{IOB} = 15 pF	1.35-2.5	0.85-2.7	-	0.6	3	ns
			2.5-3.6	0.85-2.7	-	0.5	3	
t_{R-A}	A port Rise Time	C_{IOA} = 15 pF	1.35-3.6	0.85-1.8	-	4	12	ns
			1.35-3.6	1.8-2.7	-	0.7	4	
t_{F-A}	A port Fall Time	C_{IOA} = 15 pF	1.35-3.6	0.85-1.8	-	0.8	4	ns
			1.35-3.6	1.8-2.7	-	0.5	3	
Z_{OB}	B port One-Shot Output Impedance	*5	1.5 2.5 3.6	0.9-2.5	- - -	37 20 15	- - -	Ω
Z_{OA}	A port One-Shot Output Impedance	*5	1.5-3.3	0.9 1.8 2.5	- - -	52 17 15	- - -	Ω
t_{PD_A-B}	Propagation Delay (Driving B port)	C_{IOB} = 15 pF	1.35-3.6	0.85-2.7	-	9.8	35	ns
			2.5-3.6	1.8-2.7	-	2.3	10	
		C_{IOB} = 30 pF	1.35-3.6	0.85-2.7	-	10	35	
			2.5-3.6	1.8-2.7	-	2.5	10	
		C_{IOB} = 50 pF	1.35-3.6	0.85-2.7	-	10.4	37	
			2.5-3.6	1.8-2.7	-	2.7	11	
		C_{IOB} = 100 pF	1.35-3.6	0.85-2.7	-	10.9	40	
			2.5-3.6	1.8-2.7	-	3.3	13	
t_{PD_B-A}	Propagation Delay (Driving A port)	C_{IOA} = 15 pF	1.35-3.6	0.85-2.7	-	9.4	35	ns
			2.5-3.6	1.8-2.7	-	1.6	10	
		C_{IOA} = 30 pF	1.35-3.6	0.85-2.7	-	9.6	35	
			2.5-3.6	1.8-2.7	-	1.8	10	
		C_{IOA} = 50 pF	1.35-3.6	0.85-2.7	-	10	37	
			2.5-3.6	1.8-2.7	-	2	11	
		C_{IOA} = 100 pF	1.35-3.6	0.85-2.7	-	11.2	40	
			2.5-3.6	1.8-2.7	-	2.6	13	
t_{SK}	Channel-to-Channel	C_{IOB} = 15pF, C_{IOA} = 15pF[*5]	1.35-3.6	0.85-2.7	-	-	0.15	ns
t_{EN-B} (t_{PZH})	B port Output Enable Time	C_{IOB} = 15pF, I/O_A = V_{CCA}	1.35-3.6	0.85-2.7	-	120	250	ns
			2.5-3.6	1.8-2.7	-	40	160	
t_{EN-B} (t_{PZL})		C_{IOB} = 15pF, I/O_A = 0V	1.35-3.6	0.85-2.7	-	80	200	
			2.5-3.6	1.8-2.7	-	40	160	
t_{EN-A} (t_{PZH})	A port Output Enable Time	C_{IOA} = 15pF, I/O_B = V_{CCB}	1.35-3.6	0.85-2.7	-	120	250	ns
			2.5-3.6	1.8-2.7	-	40	160	
t_{EN-A} (t_{PZL})		C_{IOA} = 15 pF, I/O_B = 0 V	1.35-3.6	0.85-2.7	-	50	200	
			2.5-3.6	1.8-2.7	-	30	160	
t_{DIS-B} (t_{PHZ})	B port Output Disable Time	C_{IOB} = 15pF, I/O_A = V_{CCA}	1.35-3.6	0.85-2.7	-	200	400	ns
			2.5-3.6	1.8-2.7	-	200	400	
t_{DIS-B} (t_{PLZ})		C_{IOB} = 15pF, I/O_A = 0V	1.35-3.6	0.85-2.7	-	60	175	
			2.5-3.6	1.8-2.7	-	60	175	
t_{DIS-A} (t_{PHZ})	A port Output Disable Time	C_{IOB} = 15pF, I/O_A = V_{CCA}	1.35-3.6	0.85-2.7	-	180	400	ns
			2.5-3.6	1.8-2.7	-	100	400	
t_{DIS-A} (t_{PLZ})		C_{IOB} = 15pF, I/O_A = 0V	1.35-3.6	0.85-2.7	-	50	175	
			2.5-3.6	1.8-2.7	-	50	175	

To be continued.

Continuously.

Sym	Parameter	Test Conditions[*1]	V_{CCB}[*2] (V)	V_{CCA}[*3](V)	-40 ℃ to +85 ℃			Unit
					Min	Typ[*4]	Max	
M_{IDR}	Maximum Data Rate	C_{IO} = 15pF	1.35-3.6	0.85-2.7	50	-	-	mbps
			2.5-3.6	1.8-2.7	140	-	-	
		C_{IO} = 30pF	1.35-3.6	0.85-2.7	40	-	-	
			2.5-3.6	1.8-2.7	120	-	-	
		C_{IO} = 50pF	1.35-3.6	0.85-2.7	30	-	-	
			2.5-3.6	1.8-2.7	100	-	-	
		C_{IO} = 100pF	1.35-3.6	0.85-2.7	20	-	-	
			2.5-3.6	1.8-2.7	60	-	-	

Notes:
1. Normal test conditions are V_I = 0 V, $C_{IOB} \leq$ 15pF and $C_{IOA} \leq$ 15pF, unless otherwise specified.
2. V_{CCB} is the supply voltage associated with the I/O B port, and B ranges from +1.35 V to 3.6 V under normal operating conditions.
3. V_{CCA} is the supply voltage associated with the I/O A port, and A ranges from +0.85 V to 2.7V under normal operating conditions.
4. Typical values are tested at T_A = +25 ℃. Limits over the operating temperature range are guaranteed by design.
5. Guaranteed by design

Power Consumption (T_A=+25 ℃)

Sym[*1]	Parameter	Test Conditions	V_{CCB}[*2] (V)	V_{CCA}[*3](V)	Typ	Unit
C_{PD_VCCA}	A = Input port, B = Output Port	C_{Load} = 0, f = 1MHz, EN = V_{CCA} (outputs enabled)	1.35-3.6	0.85-2.7	40	pF
	B = Input port, A = Output Port					
C_{PD_VCCB}	A = Input port, B = Output Port	C_{Load} = 0, f = 1MHz, EN = V_{CCA} (outputs enabled)	1.35-3.6	0.85-2.7	40	pF
	B = Input port, A = Output Port					
C_{PD_VCCA}	A = Input port, B = Output Port	C_{Load} = 0, f = 1MHz, EN = GND(outputs disabled)	1.35-3.6	0.85-2.7	1	pF
	B = Input port, A = Output Port					
C_{PD_VCCB}	A = Input port, B = Output Port	C_{Load} = 0, f = 1MHz, EN = GND(outputs disabled)	1.35-3.6	0.85-2.7	1	pF
	B = Input port, A = Output Port					

Notes:

1. C_{PD_VCCA} and C_{PD_VCCB} are defined as the value of the IC's equivalent capacitance from which the operating current can be calculated for the A and B power supplies, respectively. $I_{CC} = I_{CC}$ (dynamic) + I_{CC} (static) ≈ I_{CC}(operating) ≈CPD x V_{CC} x f_{IN} x NSW where $I_{CC} = I_{CC_}V_{CCB}$+ I_{CC} V_{CCA} and NSW = total number of outputs switching.
2. V_{CCB} is the supply voltage associated with the I/O B port, and V_{CCB} ranges from +1.35V to 3.6V under normal operating conditions.
3. V_{CCA} is the supply voltage associated with the I/O A port, and V_{CCA} range from +0.0.85 V to 2.7V under normal operating conditions.
4. Typical values are at T_A = +25 ℃.

Test Circuits

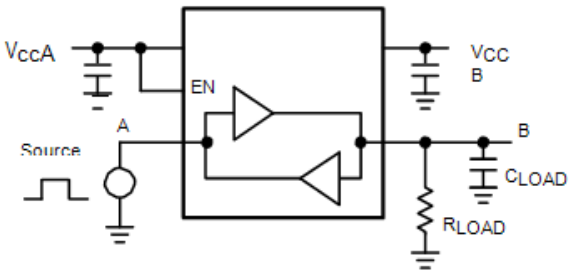


Figure 2. Driving A Test Circuit

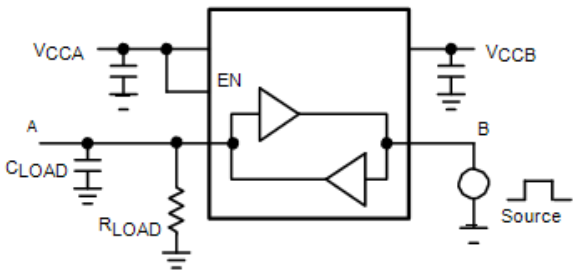


Figure 3. Driving B Test Circuit

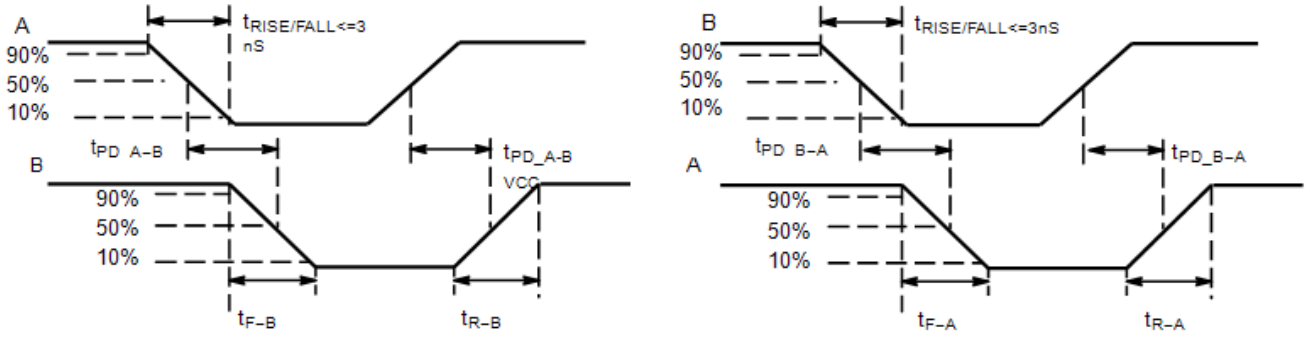
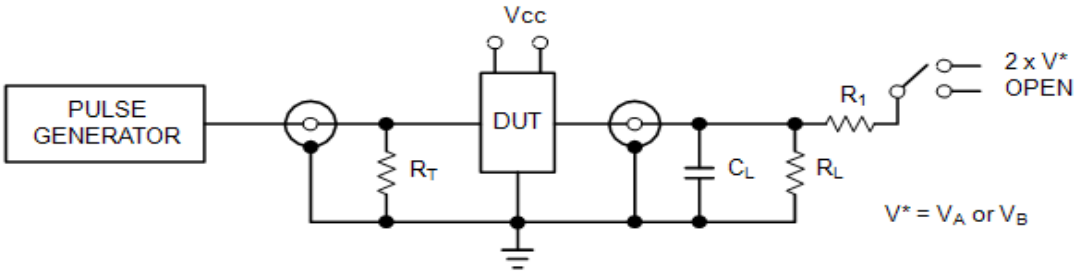


Figure 4. Definition of Timing Specification Parameters



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V*

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)
V* = V_A or V_B for A or B measurements,
respectively.

Figure 5. Test Circuit for Enable/Disable Time Measurement

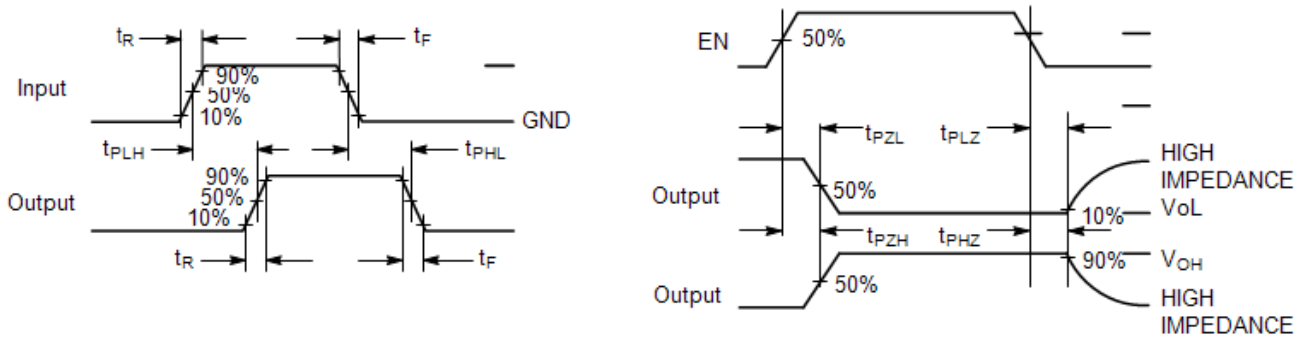


Figure 6. Timing Definitions for Propagation Delays and Enable/Disable Measurement

Functional Description

The PI4ULS3V304 is a 4-bit configurable dual-supply autosensing bidirectional level translator that does not require a direction control pin. The B and A ports are designed to track two different power supply rails, VCCB and VCCA respectively.

The PI4ULS3V304 offers the feature that the values of the VCCB and V_{CCA} supplies are independent. Design flexibility is maximized because VCCA can be set to a value either greater than or less than the VCCB supply.

The PI4ULS3V304 has high output current capability, which allows the translator to drive high capacitive loads such as most high frequency EMI filters. Another feature of the PI4ULS3V304 is that each An and Bn channel can function as either an input or an output.

An Output Enable (EN) input is available to reduce the power consumption. The EN pin can be used to disable both I/O ports by putting them in 3-state which significantly reduces the supply current.

Application Information

Level Translator Architecture

The PI4ULS3V304 auto-sense translator provides bi-directional logic voltage level shifting to transfer data in multiple supply voltage systems. These level translators have two supply voltages, V_{CCA} and V_{CCB}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the I/O V_{CCA} to the I/O V_{CCB} ports, input signals referenced to the V_{CCA} supply are translated to output signals with a logic level matched to VCCB. In a similar manner, the I/O V_{CCB} to I/O V_{CCA} translation shifts input signals with a logic level compatible to V_{CCB} to an output signal matched to V_{CCA}. The PI4ULS3V304 translator consists of bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. One-shot circuits are used to detect the rising or falling input signals. In addition, the one-shots decrease the rise and fall times of the output signal for high-to-low and low-to-high transitions.

Input Driver Requirements

Auto-sense translators such as the PI4ULS3V304 have a wide bandwidth, but a relatively small DC output current rating. The high bandwidth of the bi-directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. The I/O ports have a modest DC current output specification so that the output driver can be over driven when data is sent in the opposite direction. For proper operation, the input driver to the auto-sense translator should be capable of driving 3mA of peak output current. The bi-directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage. Enable Input (EN) The PI4ULS3V304 translator has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CCB} and I/O V_{CCA} pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_{CCA} supply and has Over-Voltage Tolerant (OVT) protection.

Uni-Directional versus Bi-Directional Translation

The PI4ULS3V304 translator can function as a non-inverting uni-directional translator. One advantage of using the translator as a uni-directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni-directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

The values of the V_{CCA} and V_{CCB} supplies can be set to anywhere in range 0.85-2.7V and 1.35-3.6V. Design flexibility is maximized because V_{CCA} may be either greater than or less than the V_{CCB} supply. In contrast, the majority of the competitive auto sense translators has a restriction that the value of the V_{CCA} supply must be equal to less than (V_{CCB} - 0.4) V. The sequencing of the power supplies will not damage the device during power-up operation. In addition, the I/O V_{CCB} and I/O V_{CCA} pins are in the high impedance state if either supply voltage is equal to 0V. For optimal performance, 0.01 to 0.1µF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces. The PI4ULS3V304 translators have a power down feature that provides design flexibility. The output ports are disabled when either power supply is off (V_{CCA} or V_{CCB} = 0V). This feature causes all of the I/O pins to be in the power saving high impedance state.

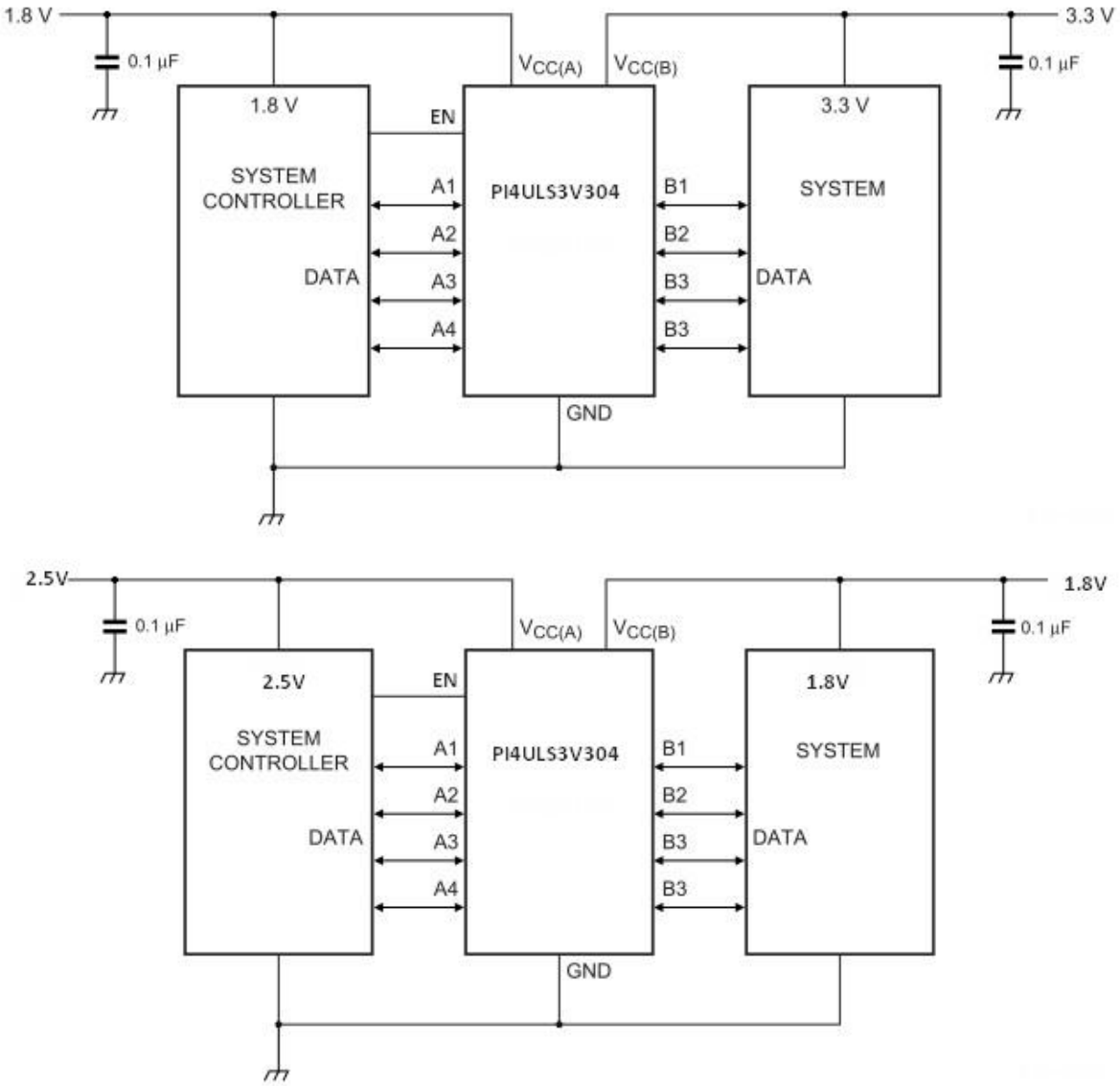
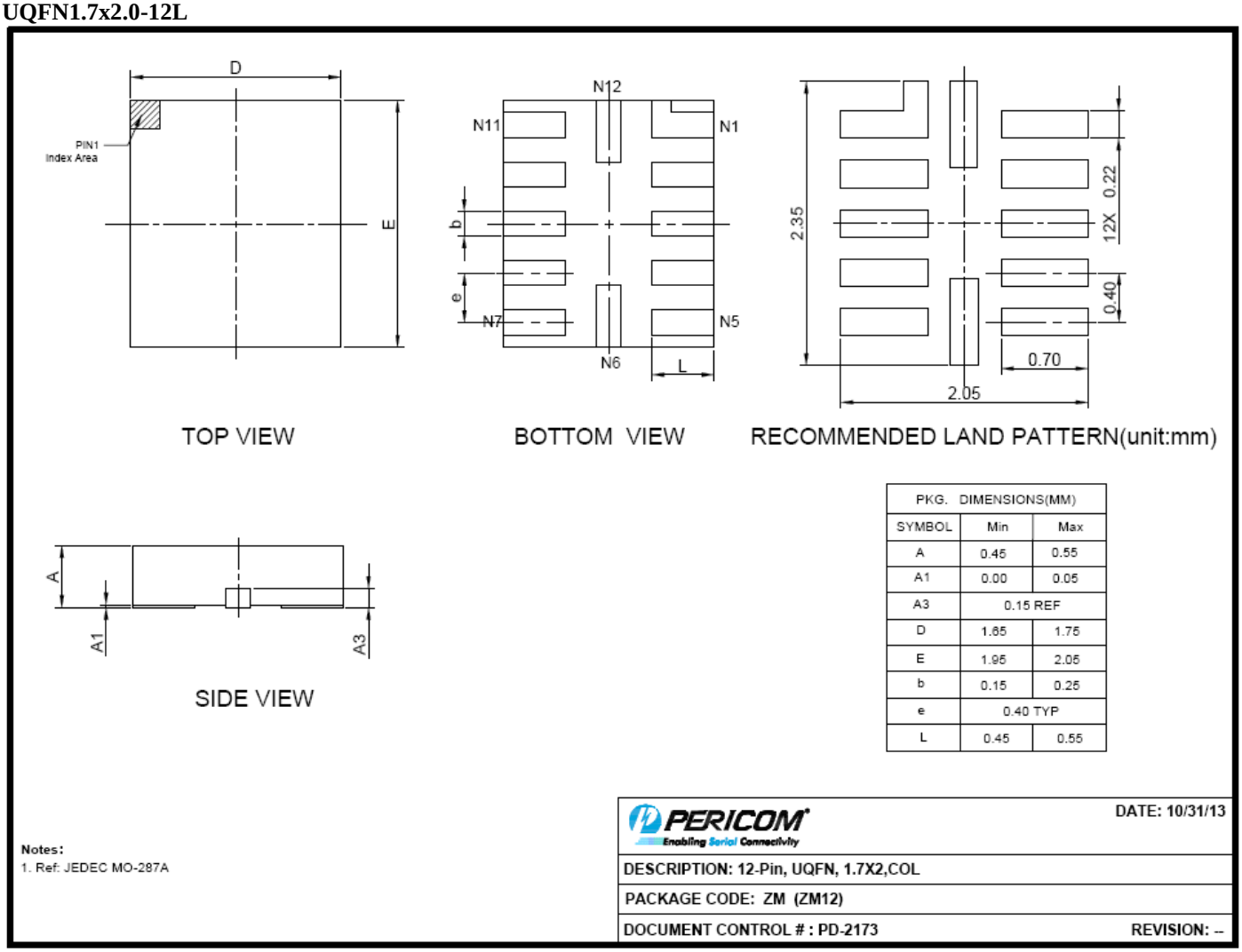


Figure 7. Typical Application

Mechanical Information

UQFN1.7x2.0-12L



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF	
D	1.65	1.75
E	1.95	2.05
b	0.15	0.25
e	0.40 TYP	
L	0.45	0.55

Notes:
1. Ref: JEDEC MO-287A

PERICOM Enabling Serial Connectivity — DATE: 10/31/13

DESCRIPTION: 12-Pin, UQFN, 1.7X2,COL

PACKAGE CODE: ZM (ZM12)

DOCUMENT CONTROL # : PD-2173 REVISION: --

Ordering Information

Part No.	Package Code	Package
PI4ULS3V304ZME	ZM	Lead free and Green 12-pin UQFN1.7x2.0

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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