LM6121/LM6221/LM6321 High Speed Buffer

Check for Samples: LM6121, LM6221, LM6321

FEATURES

- **High Slew Rate: 800 V/µs**
- **Wide Bandwidth: 50 MHz**
- **Slew rate and Bandwidth 100% Tested**
- **Peak Output Current: ±300 mA**
- **High Input Impedance: 5 MΩ**
- **LH0002H Pin Compatible**
- **No Oscillations with Capacitive Loads**
- **5V to ±15V Operation Specified**
- **Current and Thermal Limiting**
- **Fully Specified to Drive 50Ω Lines**

APPLICATIONS

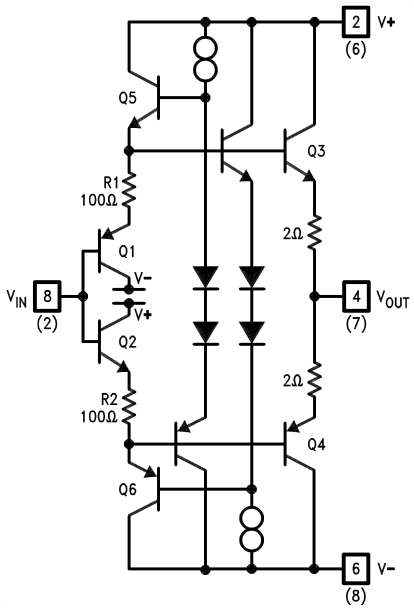
- **Line Driving**
- **Radar**
- **Sonar**

DESCRIPTION

These high speed unity gain buffers slew at 800 V/µs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

SIMPLIFIED SCHEMATIC



Numbers in ( ) are for 8-pin N DIP.

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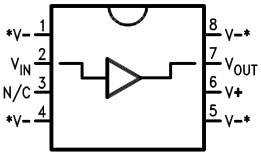
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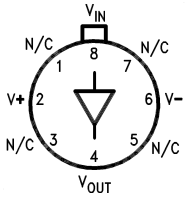
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM



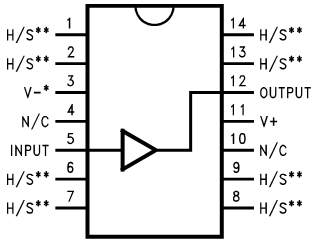
*Heat-sinking pins. See Application section on heat sinking requirements.

Plastic DIP



Note: Pin 6 connected to case.

Metal Can - Top View C



*Pin 3 must be connected to the negative supply.
**Heat-sinking pins. See Application section on heat-sinking requirements. These pins are at V^- potential.

Plastic SOIC

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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage	36V (±18)
Input to Output Voltage (2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Power Dissipation	(4)
ESD Tolerance (5)	±2000V
Junction Temperature ($T_{J(MAX)}$)	+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) During current limit or thermal limit, the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to ±20 mA.
(3) The LM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.
(4) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/\theta_{JA}$.
(5) The test circuit consists of the human body model of 120 pF in series with 1500Ω.

Operating Ratings

Operating Temperature Range	
LM6121H/883	−55°C to +125°C
LM6221	−40°C to +85°C
LM6321	0°C to +70°C
Operating Supply Range	4.75 to ±16V
Thermal Resistance (θ_{JA}), (1)	
H Package	150°C/W
N Package	47°C/W
M Package	69°C/W
Thermal Resistance (θ_{JC}), H Package	17°C/W

(1) The thermal resistance θ_{JA} of the device in the N package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 4, 5 and 8) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal resistance θ_{JA} of the N package is 84°C/W. The thermal resistance θ_{JA} of the device in the M package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 2, 6, 7, 8, 9, 13, 14) are connected to 1 square inch of 2 oz. copper.

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DC ELECTRICAL CHARACTERISTICS

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, R_L ≥ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for T_A = T_J = T_{MIN} to T_{MAX}; all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6121	LM6221	LM6321	Units
				Limit(1) (2)	Limit(1)	Limit(1)	
A_{V1}	Voltage Gain 1	R_L = 1 kΩ, V_{IN} = ±10V	0.990	0.980	0.980	0.970	V/V
				0.970	**0.950**	**0.950**	Min
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.900	0.860	0.860	0.850	V/V
				0.800	**0.820**	**0.820**	Min
A_{V3}	Voltage Gain 3 (3)	R_L = 50Ω, V^+ = 5V	0.840	0.780	0.780	0.750	V/V
		V_{IN} = 2 V_{pp} **(1.5 V_{pp})**		**0.750**	**0.700**	**0.700**	Min
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	30	30	50	mV
				50	**60**	**100**	Max
I_B	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	4	4	5	µA
				7	**7**	**7**	Max
R_{IN}	Input Resistance	R_L = 50Ω	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3	5	5	5	Ω
				10	**10**	**6**	Max
I_{S1}	Supply Current 1	R_L = ∞	15	18	18	20	mA Max
				20	**20**	**22**	
I_{S2}	Supply Current 2	R_L = ∞, V^+ = 5V	14	16	16	18	
				18	**18**	**20**	
V_{O1}	Output Swing 1	R_L = 1k	13.5	13.3	13.3	13.2	±V
				13	**13**	**13**	Min
V_{O2}	Output Swing 2	R_L = 100Ω	12.7	11.5	11.5	11	±V
				10	**10**	**10**	Min
V_{O3}	Output Swing 3	R_L = 50Ω	12	11	11	10	±V
				9	**9**	**9**	Min
V_{O4}	Output Swing 4	R_L = 50Ω, V^+ = 5V (3)	1.8	1.6	1.6	1.6	V_{PP}
				1.3	**1.4**	**1.5**	Min
PSSR	Power Supply Rejection Ratio	$V^±$ = ±5V to ±15V	70	60	60	60	dB
				55	**50**	**50**	Min

(1) Limits are specified by testing or correlation.
(2) For specification limits over the full Military Temperature Range, see RETS6121X.
(3) The input is biased to 2.5V and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V 3 test at −55°C where it is reduced to 1.5 V_{PP}.

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AC ELECTRICAL CHARACTERISTICS

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, R_L ≥ 100 kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typ	LM6121	LM6221	LM6321	Units
				Limit(1)	Limit(1)	Limit(1)	
SR_1	Slew Rate 1	V_{IN} = ±11V, R_L = 1 kΩ	1200	550	550	550	V/µs Min
SR_2	Slew Rate 2	V_{IN} = ±11V, R_L = 50Ω(2)	800	550	550	550	
SR_3	Slew Rate 3	V_{IN} = 2 V_{PP}, R_L = 50ΩV^+ = 5V (3)	50	550	550	550	
BW	−3 dB Bandwidth	V_{IN} = ±100 mV_{PP}, R_L = 50Ω, C_L ≤ 10 pF	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	R_L = 50Ω, C_L ≤ 10 pF V_O = 100 mV_{PP}	7.0				ns
t_{pd}	Propagation Delay Time	R_L = 50Ω, C_L ≤ 10 pF, V_O = 100 mV_{PP}	4.0				ns
O_S	Overshoot	R_L = 50Ω, C_L ≤ 10 pF, V_O = 100 mV_{PP}	10				%

(1) Limits are specified by testing or correlation.

(2) Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/µs.

(3) The input is biased to 2.5V and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V 3 test at −55°C where it is reduced to 1.5 V_{PP}.

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TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless otherwise specified

Frequency Response

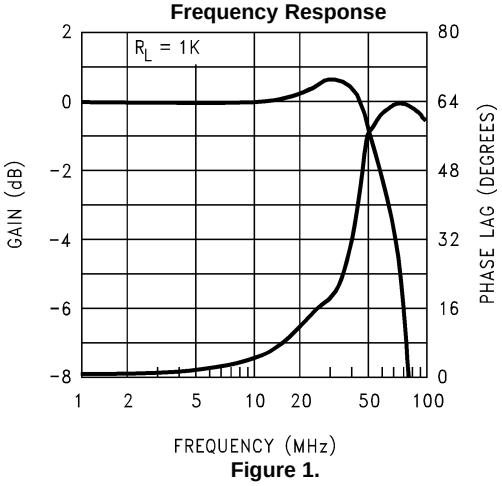


Figure 1.

Frequency Response

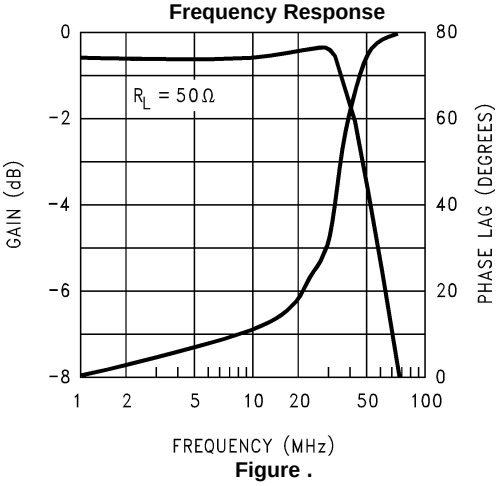


Figure .

Slew Rate vs Temperature

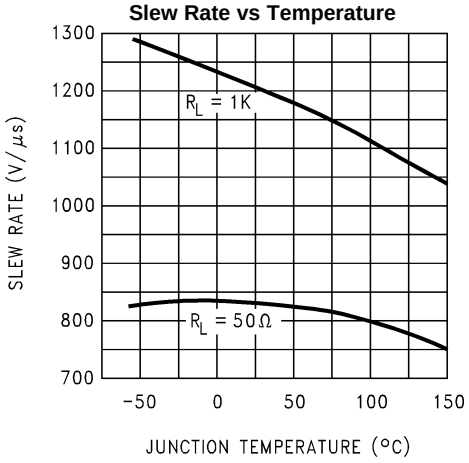


Figure 2.

Overshoot vs Capacitive Load

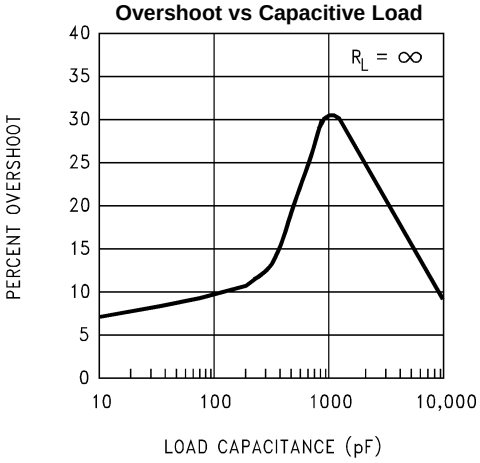


Figure 3.

Large Signal Response
R_L = 1 kΩ

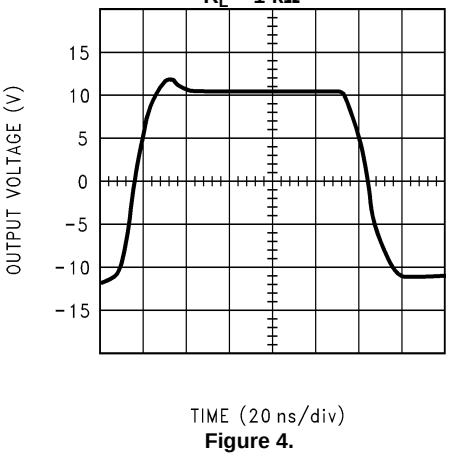


Figure 4.

Large Signal Response
R_L = 50Ω

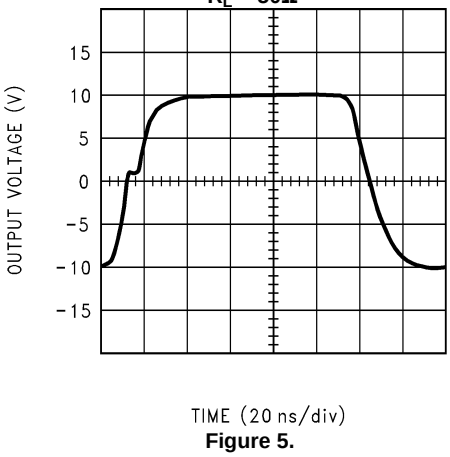


Figure 5.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C, unless otherwise specified

Supply Current

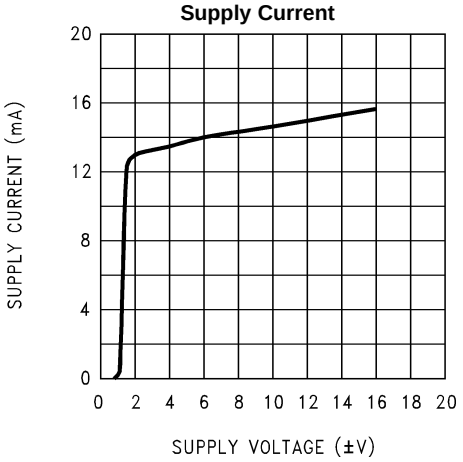


Figure 6.

−3 dB Bandwidth

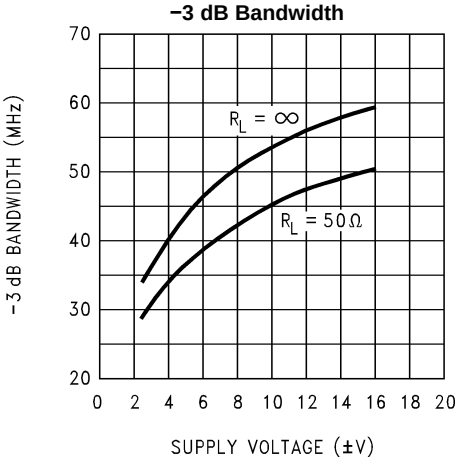


Figure 7.

Slew Rate

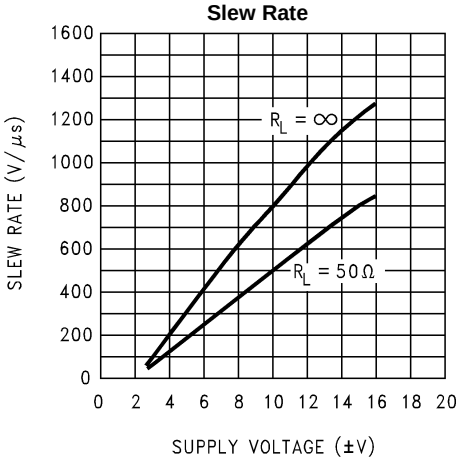


Figure 8.

Slew Rate

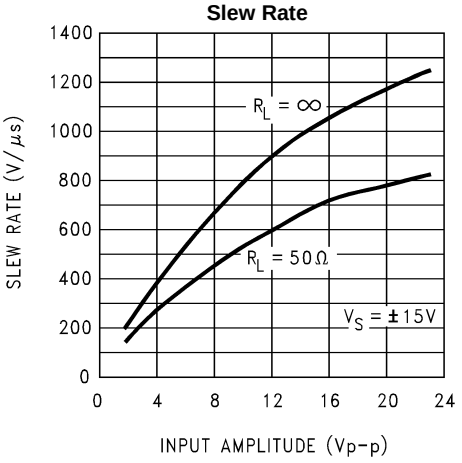


Figure 9.

Power Bandwidth

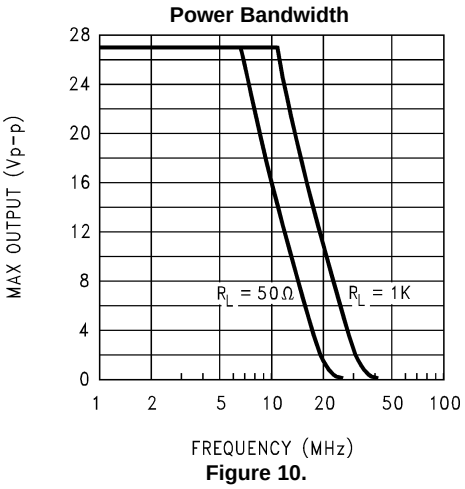


Figure 10.

Input Return Gain (S11)

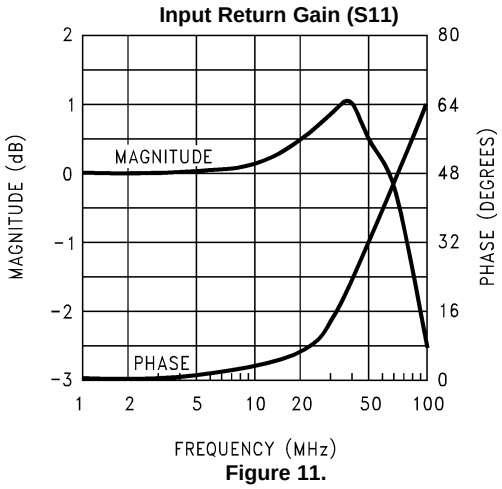


Figure 11.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C, unless otherwise specified

Forward Transmission Gain (S12)

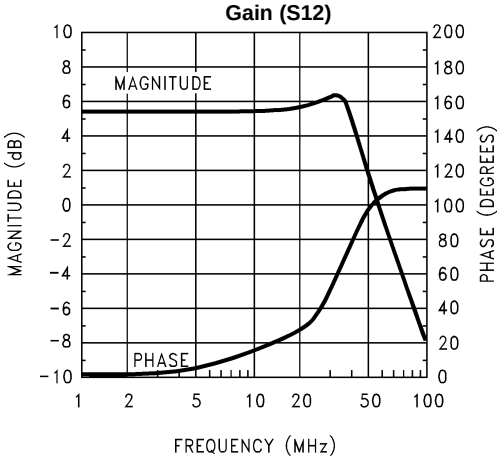


Figure 12.

Current Limit

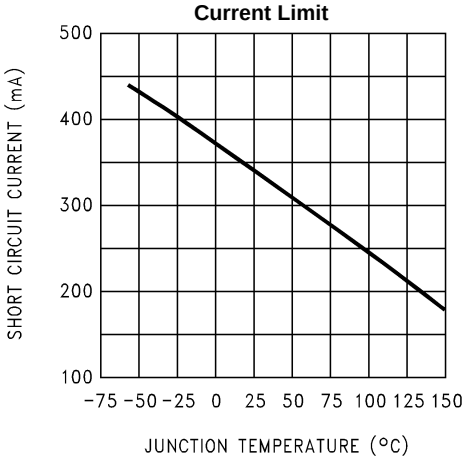


Figure 13.

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Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6121 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/µs into a 50Ω load produces a di/dt of 18 A/µs. Multiplying this by a wiring inductance of 50 nH (which corresponds to approximately 1½″ of 22 gauge wire) result in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 µF ceramic in parallel with one or two 2.2 µF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6121 is stable to any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high frequency buffer, the LM6121 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

The LM6121 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6121 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. Furthermore, this will defeat the short-circuit and over-temperature protection circuitry. Exceeding ±7V input with a shorted output will destroy the device.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see Figure 14). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6121 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.

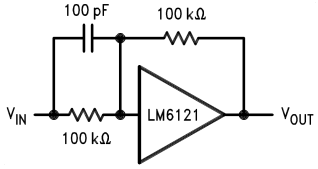


Figure 14. LM6121 with Overvoltage Protection

HEATSINK REQUIREMENTS

A heatsink may be required with the LM6321 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

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To determine if a heatsink is required, the maximum power dissipated by the buffer, P(max), must be calculated. The formula for calculating the maximum allowable power dissipation in any application is $P_D = (T_J(max) - T_A)/\theta_{JA}$. For the simple case of a buffer driving a resistive load as in Figure 15, the maximum DC power dissipation occurs when the output is at half the supply. Assuming equal supplies, the formula is $P_D = I_S (2V^+) + V^{+2}/4\ R_L$.

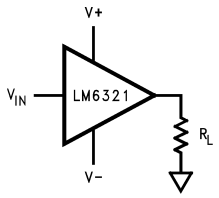


Figure 15.

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(max)$. This is calculated by using the formula:

$$T_R(max) = T_J(max) - T_A(max) \quad (1)$$

Where:

$T_J(max)$ is the maximum allowable junction temperature

$T_A(max)$ is the maximum ambient temperature

Using the calculated values for $T_R(max)$ and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

$$\theta_{(J-A)} = T_R(max)/P(max) \quad (2)$$

The heatsink for the LM6321 is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are:

Part	Package	Pins
LM6321N	8-Pin DIP	1, 4, 5, 8
LM6321M	14-Pin SO	1, 2, 3, 6, 7, 8, 9, 13, 14

Figure 17 shows copper patterns which may be used to dissipate heat from the LM6321.

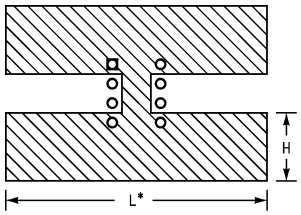
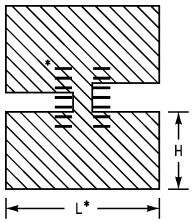


Figure 16. 8-Pin DIP



*For best results, use L = 2H

Figure 17. 14-Pin SOIC, Copper Heatsink Patterns

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The table below shows some values of junction-to-ambient thermal resistance (θ_{JA}) for values of L and W for 2 oz. copper.

Package	L (in.)	H (in.)	θ_{JA} (°C/W)
8-Pin DIP	2	0.5	47
14-Pin SO	1	0.5	69
	2	1	57

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

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