



**Document Title**

256K x 8 Hight Speed SRAM with 3.3V

**Revision History**

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	September 12,2001	

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# 256K x 8 HIGH-SPEED CMOS STATIC RAM

## FEATURES

- High-speed access times:
  - 8, 10, 12 and 15 ns
- High-performance, lower-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- $\overline{CE}$  power-down
- CMOS power: 540 mW @ 10 ns  
36 mW standby mode
- TTL compatible inputs and outputs
- Single 3.3V  $\pm$  10% power supply
- Packages available:
  - 36-pin 400mil SOJ
  - 44-pin TSOP-2

## DESCRIPTION

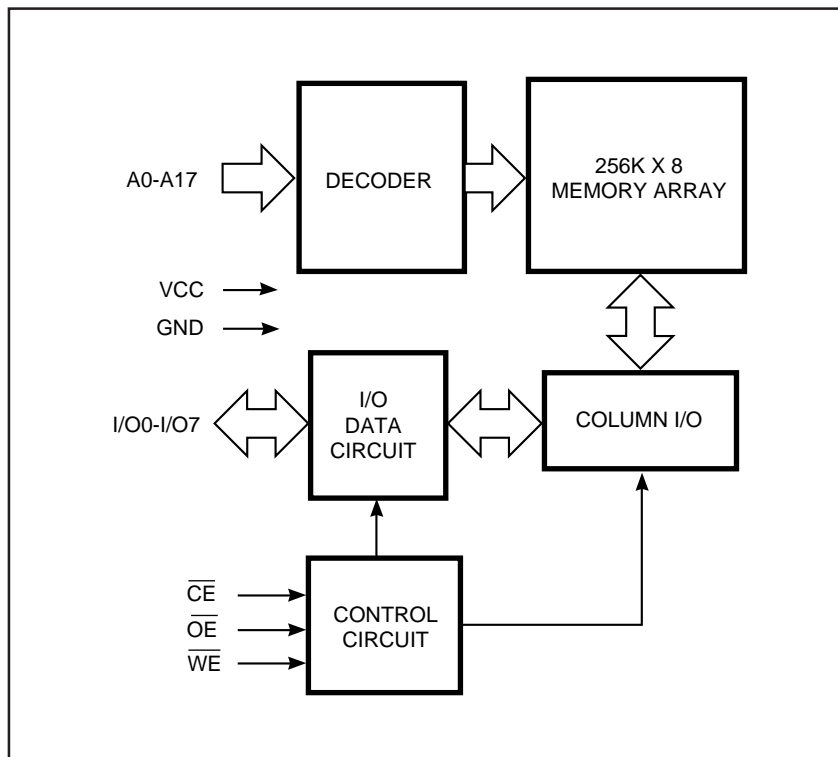
The *ICSI* IC61LV2568 is a very high-speed, low power, 262,144-word by 8-bit CMOS static RAM. The IC61LV2568 is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 36 mW (max.) with CMOS input levels.

The IC61LV2568 operates from a single 3.3V power supply and all inputs are TTL-compatible.

The IC61LV2568 is available in 36-pin, 400mil SOJ and 44-pin TSOP-2 package.

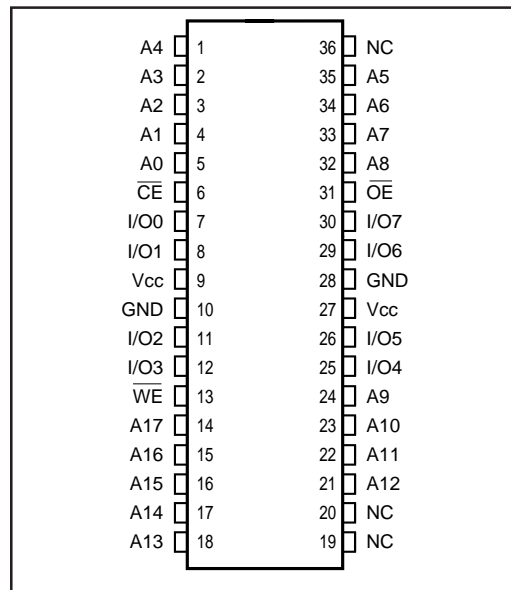
## FUNCTIONAL BLOCK DIAGRAM



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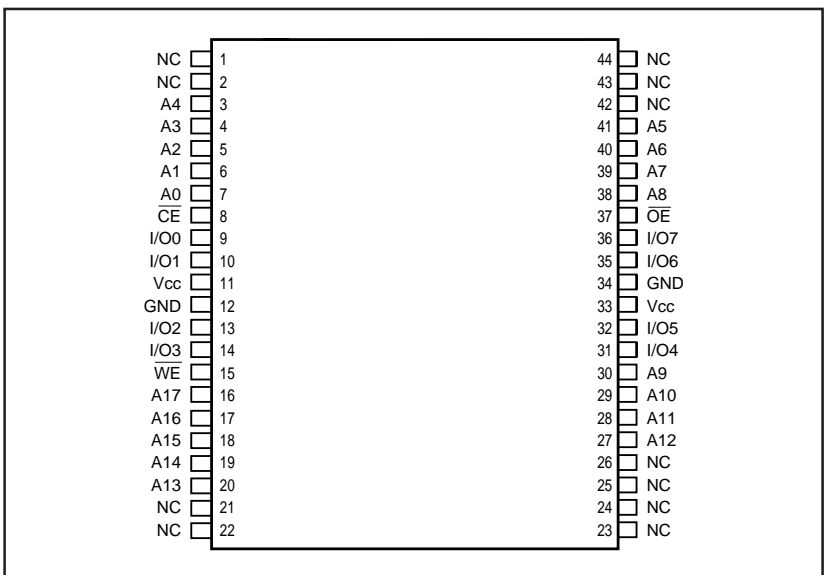
**PIN CONFIGURATION**

**36-Pin SOJ**



**PIN CONFIGURATION**

**44-Pin TSOP-2**



**PIN DESCRIPTIONS**

A0-A17	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground
NC	No Connection

**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	IsB1, IsB2
Output Disabled	H	L	H	High-Z	Icc
Read	H	L	L	DOUT	Icc
Write	L	L	X	DIN	Icc

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
Vcc	Power Supply Voltage Relative to GND	-0.5 to +4.6	V
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V
TBIAS	Temperature Under Bias	Com. -10 to +85 Ind. -45 to +90	°C
TSTG	Storage Temperature	-65 to +150	°C
Pd	Power Dissipation	1	W
IOUT	DC Output Current	±20	mA

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE**

Range	Ambient Temperature	V <sub>cc</sub>
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>cc</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>cc</sub> = Min., I <sub>OL</sub> = 8.0 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>cc</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>cc</sub>	Com. Ind.	-1 5	1 5 μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>cc</sub> , Outputs Disabled	Com. Ind.	-1 -5	1 5 μA

**Notes:**

- V<sub>IL</sub> (min.) = -0.3V (DC); V<sub>IL</sub> (min.) = -2.0V (pulse width ≤ 2.0 ns).  
V<sub>IH</sub> (max.) = V<sub>cc</sub> + 0.3V (DC); V<sub>IH</sub> (max.) = V<sub>cc</sub> + 2.0V (pulse width ≤ 2.0 ns).
- The V<sub>cc</sub> operating range for 8 ns is 3.3V +10%, -5%.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Sym.	Parameter	Test Conditions	-8 ns		-10 ns		-12 ns		-15 ns		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>CC</sub>	V <sub>cc</sub> Dynamic Operating Supply Current	V <sub>cc</sub> = Max., $\overline{CE}$ = V <sub>IL</sub> I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	170	—	150	—	140	—	130	mA
			Ind.	—	180	—	160	—	150	—	140	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>cc</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE}$ ≥ V <sub>IH</sub> , f = 0	Com.	—	30	—	30	—	30	—	30	mA
			Ind.	—	40	—	40	—	40	—	40	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>cc</sub> = Max., $\overline{CE}$ ≤ V <sub>cc</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>cc</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	—	10	—	10	—	10	—	10	mA
			Ind.	—	15	—	15	—	15	—	15	

**Notes:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>cc</sub> = 3.3V.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	8	—	10	—	12	—	15	—	ns
t <sub>AA</sub>	Address Access Time	—	8	—	10	—	12	—	15	ns
t <sub>OHA</sub>	Output Hold Time	3	—	3	—	3	—	3	—	ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time	—	8	—	10	—	12	—	15	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	3	—	4	—	5	—	6	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	0	3	0	4	0	5	0	6	ns
t <sub>LZCE<sup>(2)</sup></sub>	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE}$ to High-Z Output	0	3	0	4	0	5	0	6	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 200$  mV from steady-state voltage. Not 100% tested.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

**Notes:**

1. The V<sub>cc</sub> operating range for 8 ns is 3.3V +10%, -5%.

**AC TEST LOADS**

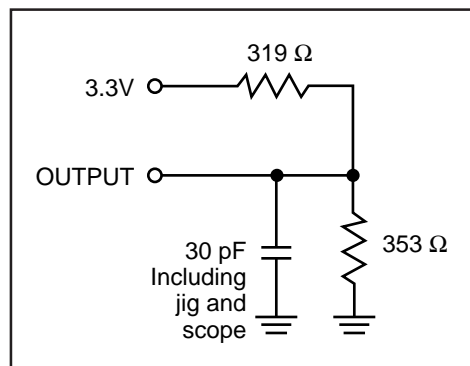


Figure 1.

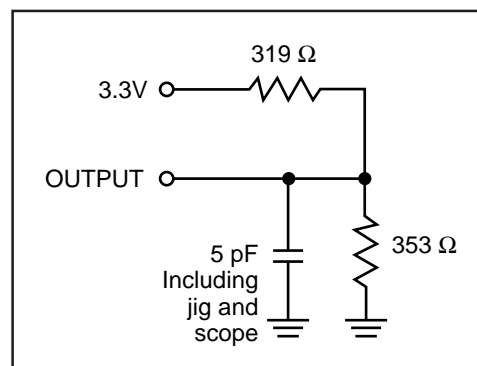
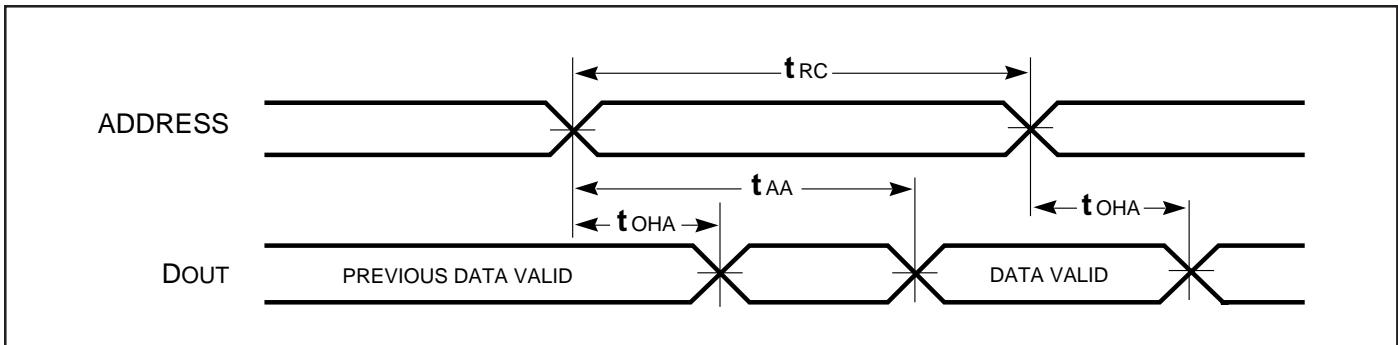


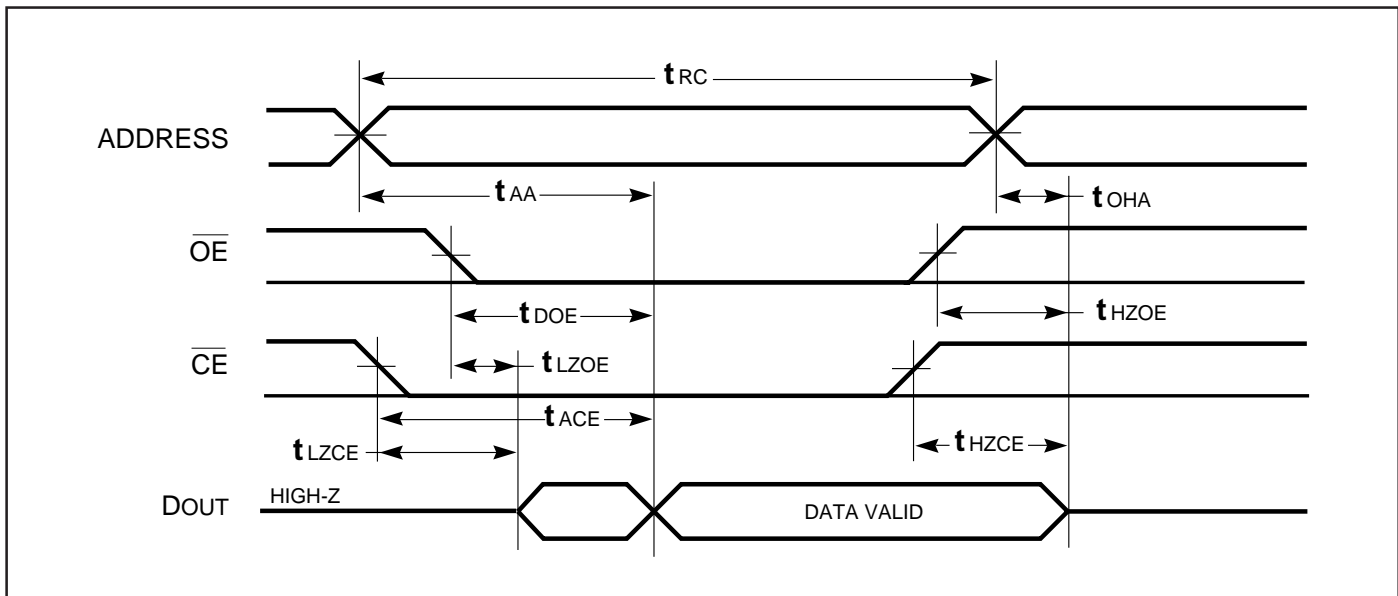
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

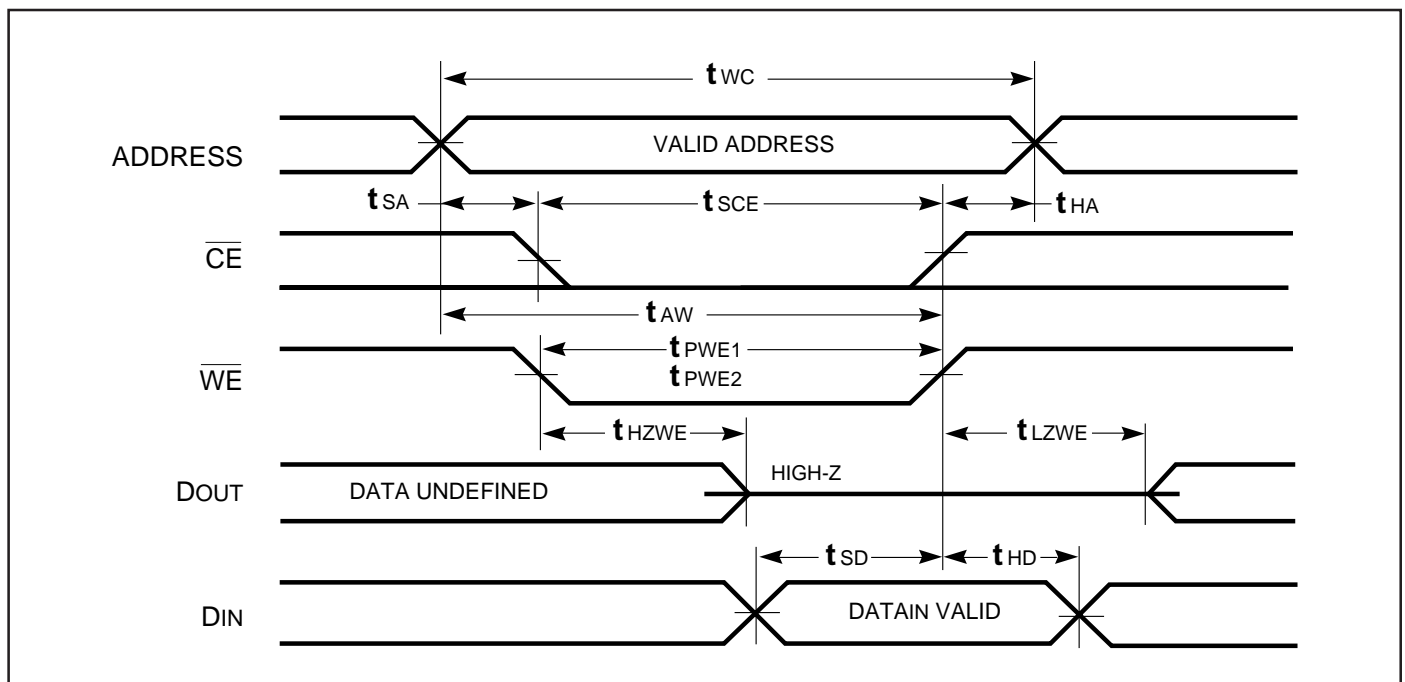
Symbol	Parameter	-8 ns		-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	8	—	10	—	12	—	15	—	ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	7	—	8	—	9	—	10	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	7	—	8	—	9	—	10	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	0	—	ns
t <sub>PWE<sup>(4)</sup></sub>	$\overline{WE}$ Pulse Width	7	—	8	—	9	—	10	—	ns
t <sub>SD</sub>	Data Setup to Write End	4.5	—	5	—	6	—	7	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t <sub>HZWE<sup>(3)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	3	—	4	—	5	—	6	ns
t <sub>LZWE<sup>(3)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	ns

**Notes:**

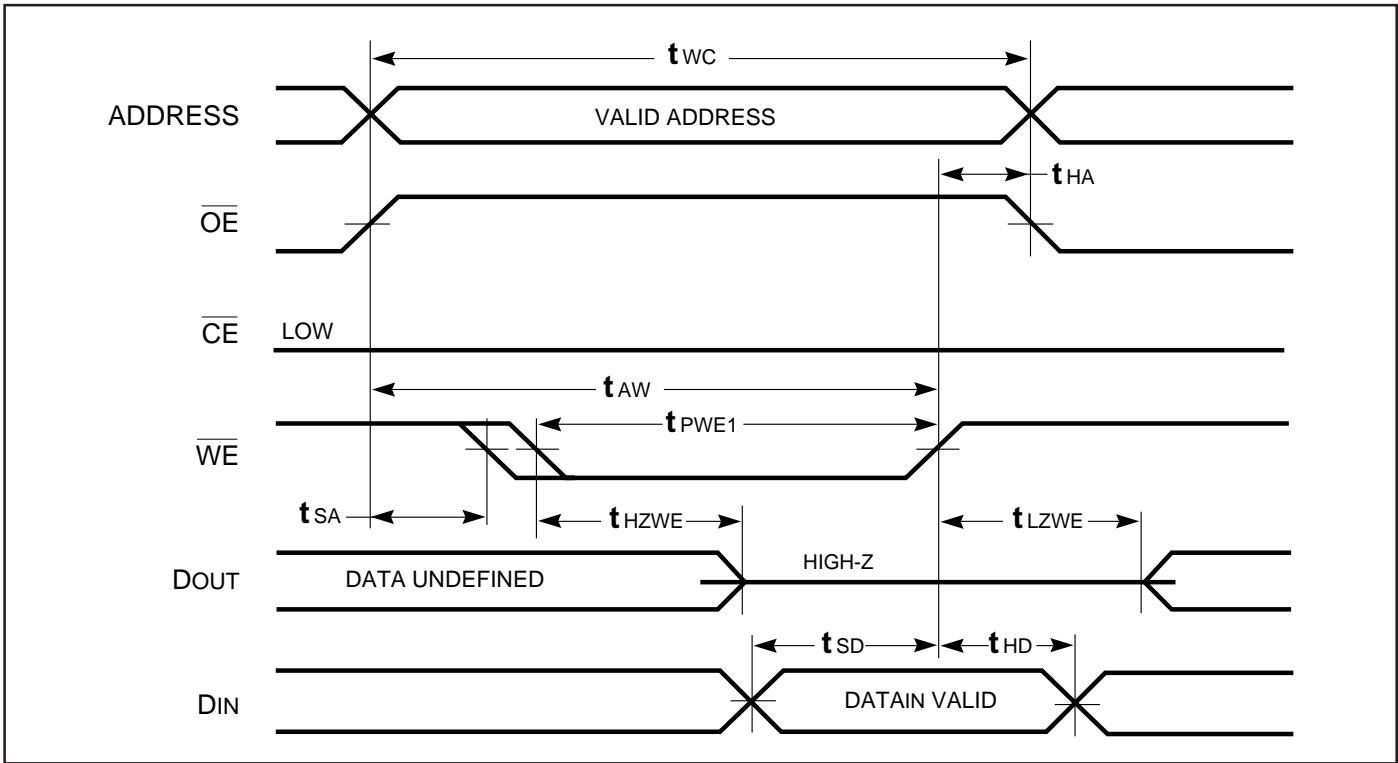
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
4. Tested with  $\overline{OE}$  Hith.

**AC WAVEFORMS**

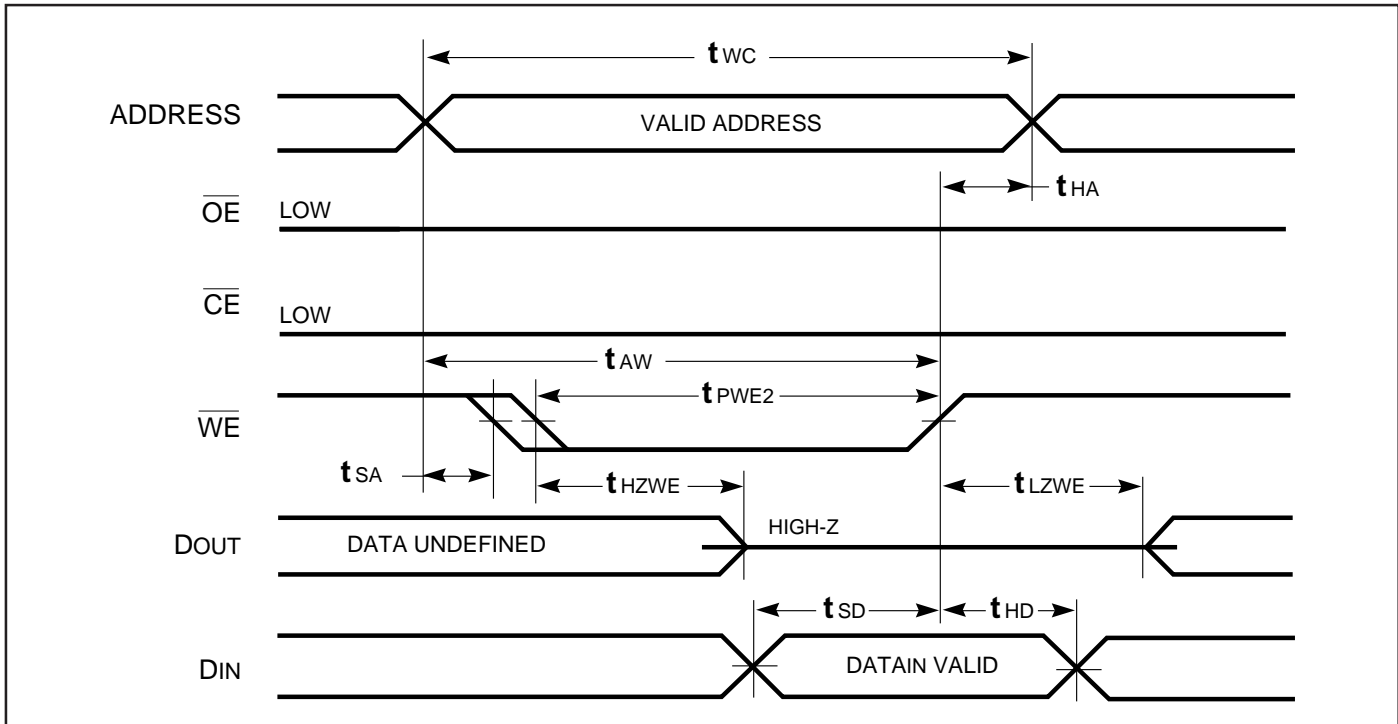
**WRITE CYCLE NO. 1** <sup>(1,2)</sup>( $\overline{CE}$  Controlled,  $\overline{OE}$  is HIGH or LOW)



**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled,  $\overline{OE}$  is HIGH During Write Cycle) <sup>(1,2)</sup>



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled,  $\overline{OE}$  is LOW During Write Cycle) <sup>(1)</sup>



**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} > V_{IH}$ .



**ORDERING INFORMATION****Commercial Range: 0°C to +70°C**

Speed(ns)	OrderPartNo.	Package
8	IC61LV2568-8T	400mil T SOP-2
	IC61LV2568-8K	400mil SOJ
10	IC61LV2568-10T	400mil T SOP-2
	IC61LV2568-10K	400mil SOJ
12	IC61LV2568-12T	400mil T SOP-2
	IC61LV2568-12K	400mil SOJ
15	IC61LV2568-15T	400mil T SOP-2
	IC61LV2568-15K	400mil SOJ

**ORDERING INFORMATION****Industrial Range: -40°C to +85°C**

Speed(ns)	OrderPartNo.	Package
8	IC61LV2568-8TI	400mil T SOP-2
	IC61LV2568-8KI	400mil SOJ
10	IC61LV2568-10TI	400mil T SOP-2
	IC61LV2568-10KI	400mil SOJ
12	IC61LV2568-12TI	400mil T SOP-2
	IC61LV2568-12KI	400mil SOJ
15	IC61LV2568-15TI	400mil T SOP-2
	IC61LV2568-15KI	400mil SOJ

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