MULTI-RATE SONET/SDH CLOCK RECOVERY UNIT S3076

FEATURES

- SiGe BiCMOS technology
- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for:
  OC-48 (2488.32 Mbps) (with FEC)
  Fibre Channel (2125 Mbps) (with FEC)
  OC-24 (1244.16 Mbps) (with FEC)
  Gigabit Ethernet (1250 Mbps) (with FEC)
  Fibre Channel (1062.5 Mbps) (with FEC)
  OC-12 (622.08 Mbps) (with FEC)
  OC-3 (155.52 Mbps) (with FEC) NRZ data
- Selectable reference frequencies
  19.44 MHz or 155.52 MHz
  (or equivalent Fibre Channel/
  Gigabit Ethernet frequencies)
- Lock detect—monitors frequency of incoming data
- Low-jitter serial interface
- +3.3 V supply
- Compact 48 pin TQFP TEP package
- Typical power 620 mW
- Available in Die form also

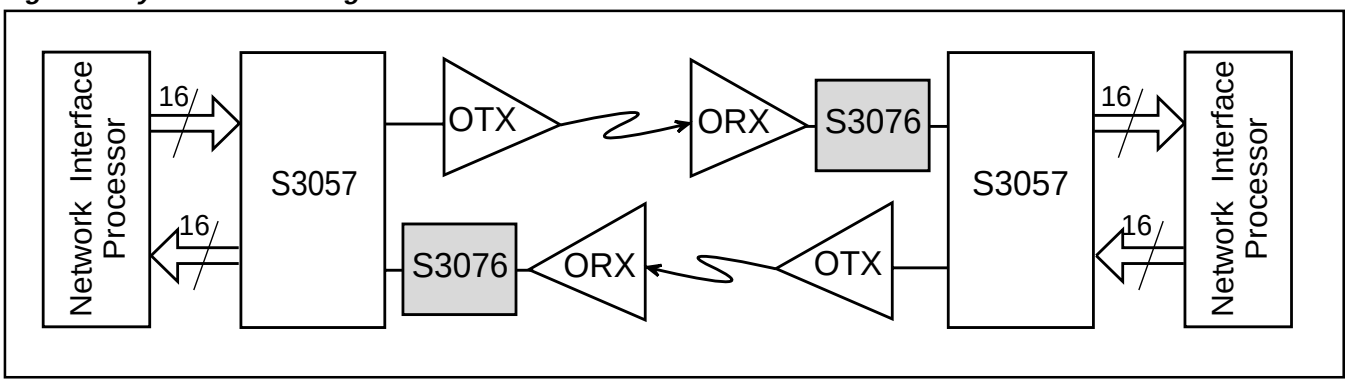
GENERAL DESCRIPTION

The function of the S3076 clock recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3076 is implemented using AMCC's proven Phase Locked Loop (PLL) technology. Figure 1 shows a typical network application.

The S3076 receives an OC-48, OC-24, OC-12, OC-3, Fibre Channel or Gigabit Ethernet scrambled NRZ signal with FEC capability up to 8 bytes per 255-byte block and recovers the clock from the data. The chip outputs a differential bit clock and retimed data.

The S3076 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

Figure 1. System Block Diagram



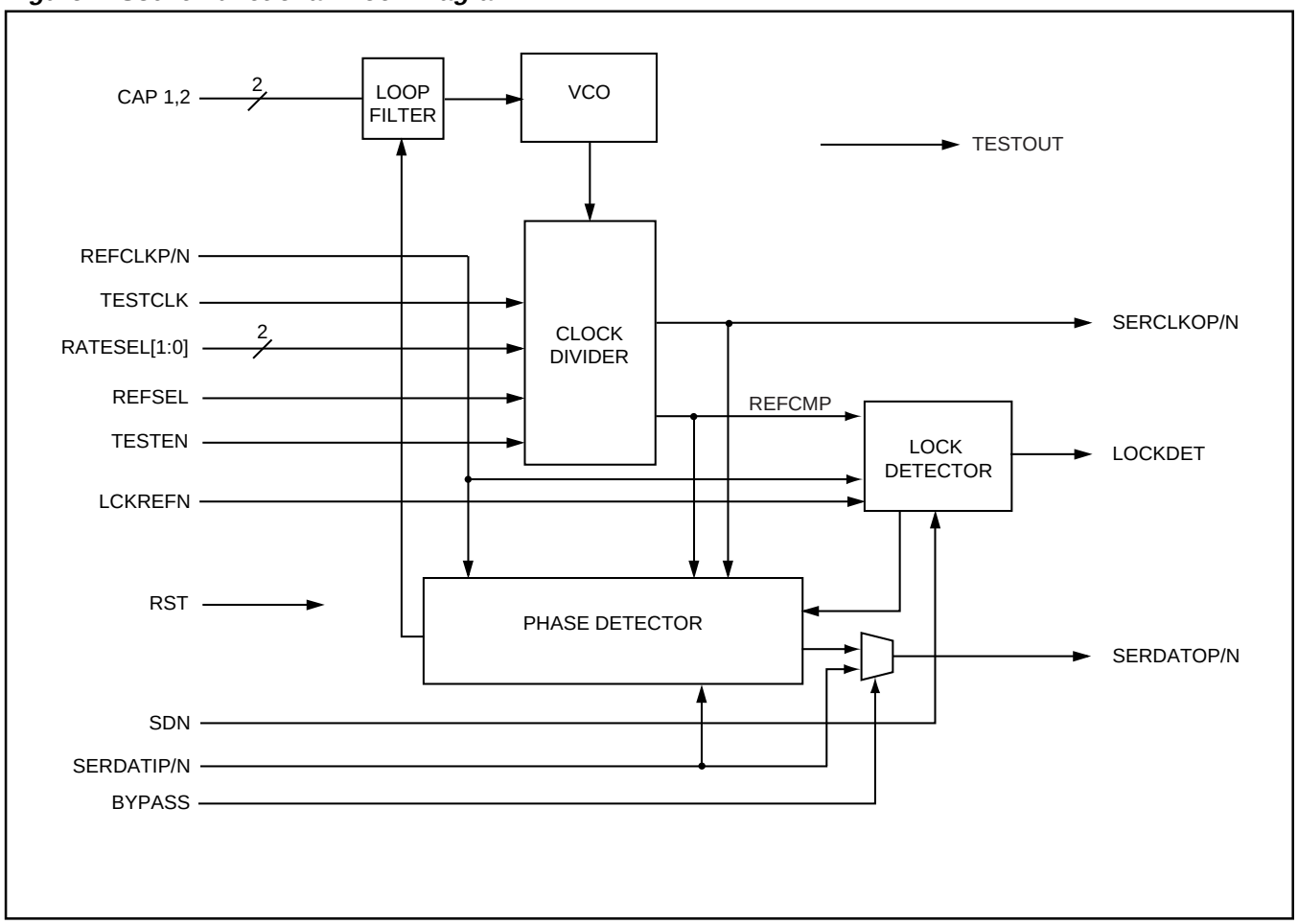
S3076 OVERVIEW

The S3076 supports clock recovery for the OC-48, Fibre Channel (2125 Mbps), OC-24, Gigabit Ethernet, Fibre Channel (1062.5 Mbps), OC-12 or OC-3 data rate with FEC capabilty up to 8 bytes per 255-byte block. Differential serial data is input to the chip at the specified rate, and clock recovery is performed on the incoming data stream. An external oscillator is required to minimize the PLL lock time, and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3076.

Suggested Interface Devices

Sumitomo	OC-48 Optical Receiver
AMCC S3057	OC-48 Transceiver

Figure 2. S3076 Functional Block Diagram



S3076 FUNCTIONAL DESCRIPTION

The S3076 clock recovery device performs the clock recovery function for SONET OC-48, Fibre Channel (2125 Mbps), OC-24, Gigabit Ethernet, Fibre Channel (1062.5 Mbps), OC-12 or OC-3 serial data links with FEC capabilty up to 8 bytes per 255-byte block. The chip extracts the clock from the serial data inputs and provides retimed clock and data outputs. A 155.52/19.44 MHz (156.25/19.53 MHz for Gigabit Ethernet and 132.81/16.60 MHz for Fibre Channel) reference clock is required for phase locked loop start up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate. The input data rate is selected by the RATESEL inputs. (See Table 1.)

Clock Recovery

Clock recovery, as shown in the block diagram in Figure 2, generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by a value greater than that stated in Table 7 with respect to REFCLKP/N, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of SDN will also cause an out of lock condition.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 3.

Lock Detect

The S3076 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than that stated in Table 7, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within that stated in Table 7, the PLL will be declared in lock and the lock detect output will go active. The assertion of SDN will also cause an out of lock condition.

Table 1. Data Rate Select

RATESEL0	RATESEL1	Operating Mode	REFCLK Frequency
0	0	OC-3	155.52/19.44
0	1	OC-12	155.52/19.44
1	0	OC-24	155.52/19.44
1	1	OC-48	155.52/19.44
1	0	Gigabit Ethernet	156.25/19.53
1	0	Fibre Channel (1062.5 Mbps)	132.81/16.60
1	1	Fibre Channel (2125 Mbps)	132.81/16.60

Table 2. Reference Frequency Select

REFSEL	Reference Frequency for Data Rates with FEC Capability of X bytes per 255–Byte Block (For OC-3/12/24/48 Rates Only)						
	X = 0	X = 3	X = 4	X = 5	X = 6	X = 7	X = 8
0	19.44 MHz	19.99 MHz	20.15 MHz	20.31 MHz	20.48 MHz	20.65 MHz	20.83 MHz
1	155.52 MHz	159.91MHz	161.21 MHz	162.53 MHz	163.87 MHz	165.26 MHz	166.63 MHz

SONET JITTER CHARACTERISTICS

Performance

The S3076 PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used as specified.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 3.

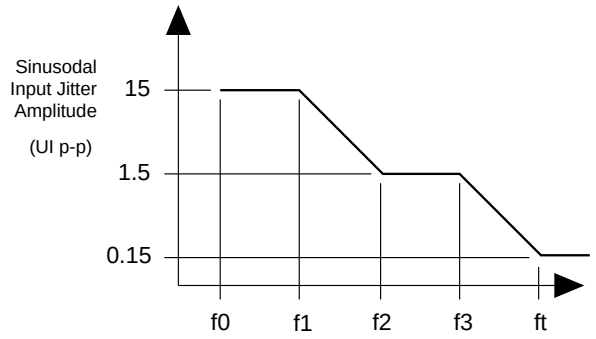
Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 4. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 be applied.

Jitter Generation

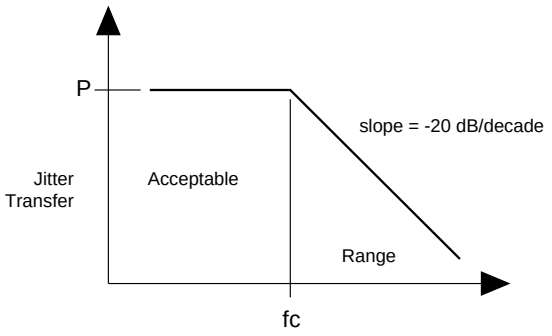
The jitter of the serial clock and serial data outputs shall not exceed the value specified in Table 7. when a serial data input with no jitter is presented to the serial data inputs. (See Table 7.)

Figure 3. Input Jitter Tolerance Specification



OC/STS Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
48	10	600	6000	100	1000
24[3]					
12	10	30	300	25	250
3	10	30	300	6.5	65

Figure 4. Jitter Transfer Specification



OC/STS Level[1,2]	fc (kHz)	P (dB)
48	2000	0.1
24[3]		
12	500	0.1
3	130	0.1

1. Bellcore Specifications: GR-253- CORE, Issue 2, December 1995.
2. ITU-T Recommendations: G.958.
3. Not specified in GR-253 or G.958.

FIBRE CHANNEL JITTER CHARACTERISTICS

Performance

The S3076 PLL complies with the jitter specifications proposed for Fibre Channel equipment defined by the fibre channel methodology for Jitter specification.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. Fibre Channel input jitter tolerance requirements are shown in Table 3.

Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed the value specified in Table 4 when a serial data input with no jitter is presented to the serial data inputs.

Table 3. Input Jitter Tolerance Specification at node α_R

Parameters	Description	Min	Max	Units
t_{FDJ}	Frequency Dependent Jitter Tolerance (637 kHz to ≥ 5 MHz)	0.10	–	UI p-p
t_{DJ}	Deterministic Jitter Tolerance (637 kHz – 531 MHz)	0.38	–	UI p-p
t_{RJ}	Random Jitter (637 kHz – 531 MHz)	0.22	–	UI p-p
t_{TJ}	Total Jitter	0.70	–	UI p-p

Table 4. Total Jitter Generation Specification at node α_T

Parameters	Description	Min	Max	Units
DJ	Deterministic Jitter		0.08	UI p-p
TJ	Total Jitter		0.23	UI p-p

Figure 5. Fibre Channel System Node Definition

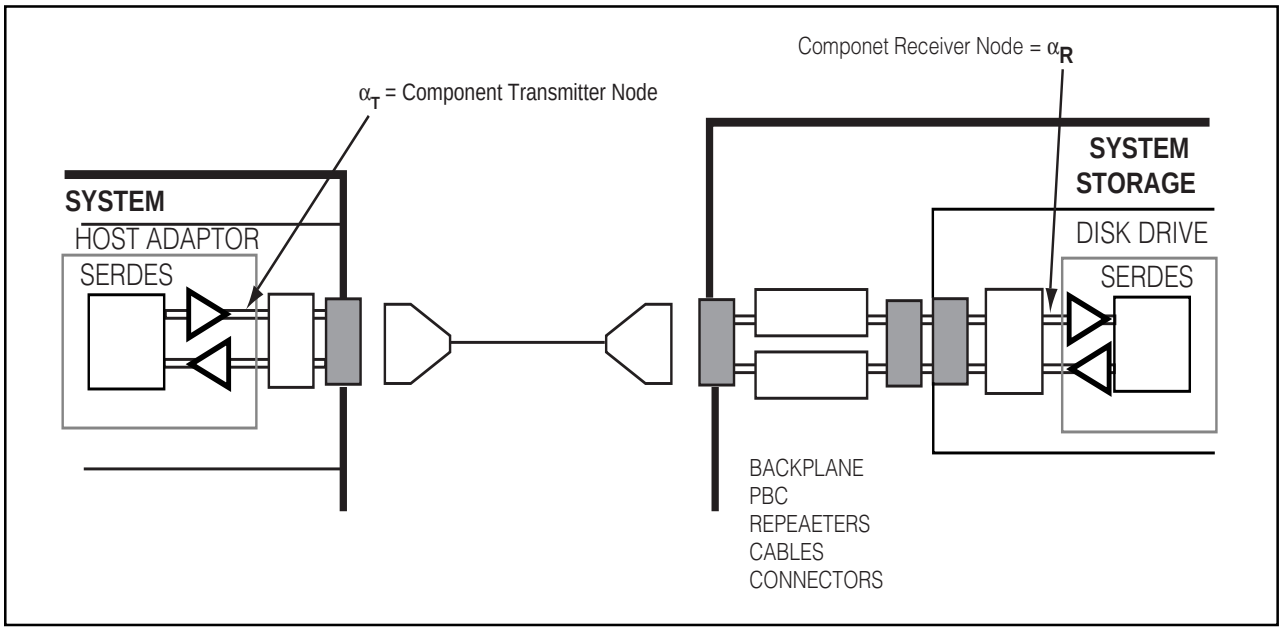


Table 5. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
SERDATIP SERDATIN	Diff. CML	I	3 2	Serial Data In. Clock is recovered from the transitions on these inputs. Internally biased and terminated. (See Figure 10.)
BYPASS	LVTTL	I	46	Active High. Used to bypass the PLL. It allows transmission of data input without clock recovery.
SDN	Single Ended LVPECL	I	45	Signal Detect. Active Low. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, and the PLL will be forced to lock to the REFCLK inputs. When SDN is active, data on the SERDATIP/N pins will be processed normally.
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	6 7	Reference Clock. 155.52/19.44 MHz (or equivalent Fibre Channel or Gigabit Ethernet frequency) input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data, during reset or when SDN is inactive. Internally biased.
CAP1 CAP2		I	40 39	Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. (See Figure 14.)
LCKREFN	LVTTL	I	17	Lock to Reference. Active Low. When active, the serial clock output will be forced to lock to the local reference clock input [REFCLK].
RATESEL0 RATESEL1	LVTTL	I	20 19	Rate Select. Selects the operating mode (See Table 1.)
TESTCLK	LVTTL	I	15	Test Clock. Test input signal used for production test. Connect to Ground for normal operation. This input is internally pulled High.
REFSEL	LVTTL	I	18	Selects the reference frequency (See Table 2.)
RST	LVTTL	I	16	Reset Input. Active High. Resets lock detect circuit and VCO divide-by-N circuit for production test.
TESTEN	LVTTL	I	47	Test Enable. Active High. Bypasses the VCO for production test. Connect to Ground for normal operation. This input is internally pulled High.
SERDATOP SERDATON	Diff. CML	O	28 27	Serial Data Out. This signal is the delayed version of the incoming data stream (SERDATIP/N) updated on the falling edge of Serial Clock Out (SERCLKOP/N).
SERCLKOP SERCLKON	Diff. CML	O	34 33	Serial Clock Out. This signal is phase aligned with Serial Data Out (SERDATO). (See Figure 8.)
LOCKDET	LVTTL	O	10	Lock Detect. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.

Table 5. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
TESTOUT		O	23	Test Output. Leave open for normal operation.
AVCC	+3.3 V	I	37 42	Analog power supply.
AGND	GND	I	38, 41, 43	Analog GND connection.
VCC	+3.3 V	I	1, 5, 9, 21, 24, 26, 29, 32, 35, 48	Power Supply.
GND	GND	I	4, 8, 11, 12, 13, 14, 22, 25, 30, 31, 36, 44	Ground connection.

Pad Assignment

Pad #	Pad Center	Pin Name	Pad #	Pad Center	Pin Name
1	(756.900, 72.425)	VCC	14	(3751.375, 868.900)	GND
2	(861.900, 72.425)	TESTOUT	15	(3751.375, 973.900)	LOCKDET
3	(966.900, 72.425)	GND	16	(3751.375, 1078.900)	VCC
4	(1806.900, 72.425)	VCC	17	(3751.375, 1603.900)	GND
5	(1911.900, 72.425)	RATESEL0	18	(3751.375, 1708.900)	REFCLKN
6	(2016.900, 72.425)	RATESEL1	19	(3751.375, 1813.900)	REFCLKP
7	(2121.900, 72.425)	REFSEL	20	(3751.375, 1918.900)	VCC
8	(2226.900, 72.425)	LCKREFN	21	(3751.375, 2758.900)	GND
9	(2331.900, 72.425)	RST	22	(3751.375, 2863.900)	SERDATIP
10	(2436.900, 72.425)	TESTCLK	23	(3751.375, 2968.900)	SERDATIN
11	(2541.900, 72.425)	GND	24	(3751.375, 3073.900)	VCC
12	(3171.900, 72.425)	GND	25	(3171.900, 3871.375)	VCC
13	(3751.375, 756.900)	GND	26	(3066.900, 3871.375)	TESTEN

Table 5. Pin Assignment and Descriptions (Continued)

Pad Assignment (Continued)					
Pad #	**Pad Center**	**Pin Name**	**Pad #**	**Pad Center**	**Pin Name**
27	(2961.900, 3871.375)	BYPASS	40	(651.900, 3871.375)	AVCC
28	(2856.900, 3871.375)	SDN	41	(72.425, 3287.900)	GND
29	(2751.900, 3871.375)	GND	42	(72.425, 3182.900)	VCC
30	(2436.925, 3871.375)	AGND	43	(72.425, 3077.900)	SERCLKOP
31	(2226.900, 3871.375)	AVCC	44	(72.425, 2972.900)	SERCLKON
32	(2121.900, 3871.375)	AVCC	45	(72.425, 2867.900)	VCC
33	(2016.900, 3871.375)	AGND	46	(72.425, 2762.900)	GND
34	(1911.900, 3871.375)	AGND	47	(72.425, 1610.400)	GND
35	(1386.900, 3871.375)	CAP1	48	(72.425, 1505.400)	VCC
36	(1281.900, 3871.375)	CAP2	49	(72.425, 1400.400)	SERDATOP
37	(966.900, 3871.375)	AGND	50	(72.425, 1295.400)	SERDATON
38	(861.900, 3871.375)	AGND	51	(72.425, 1190.400)	VCC
39	(756.900, 3871.375)	AVCC	52	(72.425, 1085.400)	GND

Figure 6. S3076 48 Pin TQFP/TEP Pinout

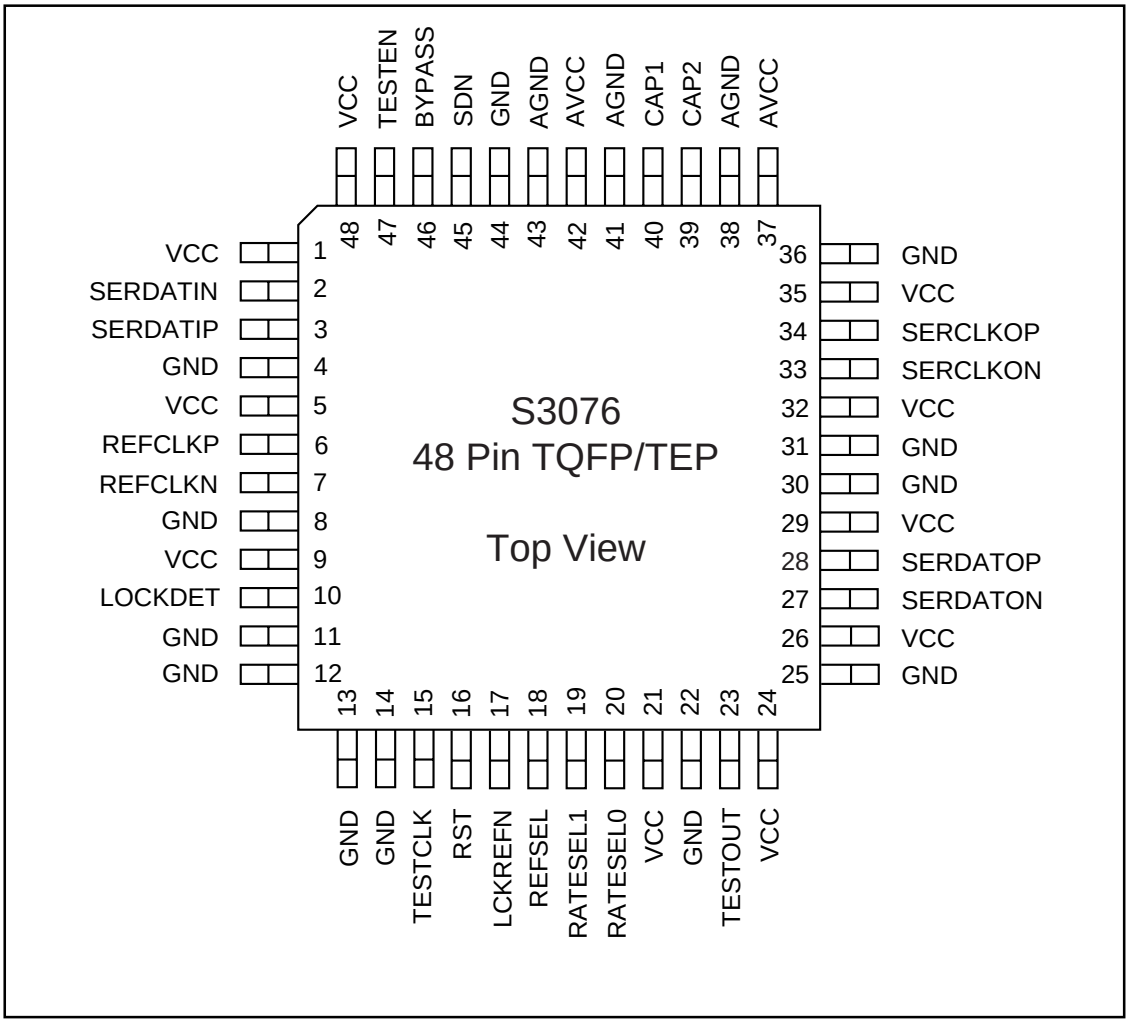
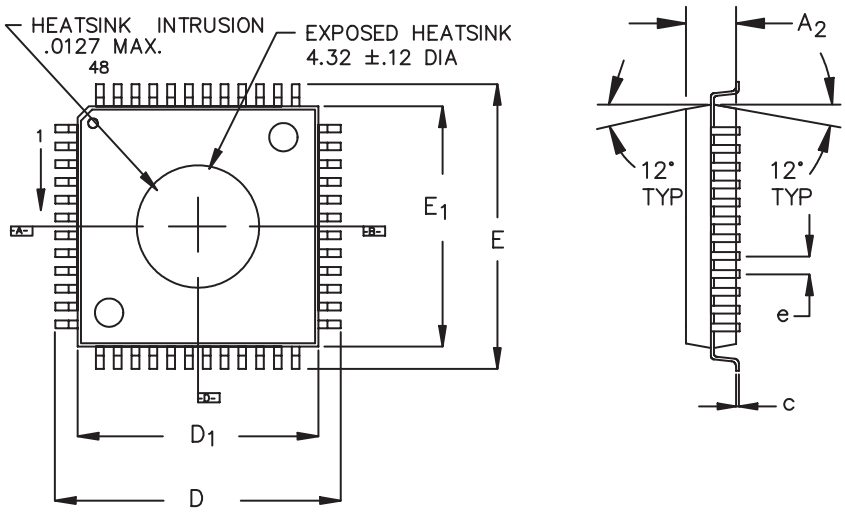
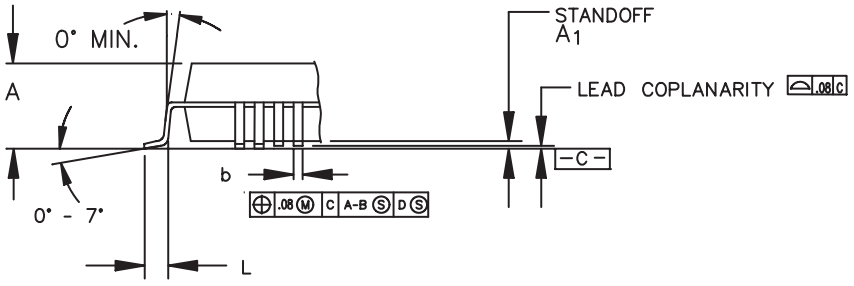


Figure 7. 48 Pin TQFP/TEP Package



TOP VIEW



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	8.80	6.90	8.80	6.90	0.75	0.50 BSC.	0.17	
NOM			1.40	9.00	7.00	9.00	7.00	0.60		0.22	1.27
MAX	1.60	0.15	1.45	9.20	7.10	9.20	7.10	0.50		0.27	

Die Width – 156.7 mils	Die Length – 161.5 mils

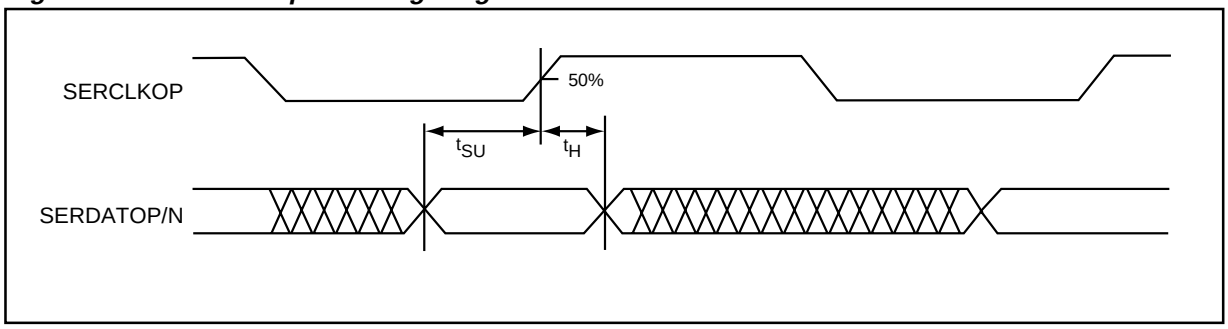
Table 6. Thermal Management

Device	Package Max Power	Θja
S3076	850 mW	50° C/W

Table 7. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
VCO Operating Frequency	2.125	2.488	2.67	GHz	
Data Output Jitter with VCO locked to SERDATIP/N OC-48 OC-24 OC-12 OC-3		 0.0038 0.002 0.002	 0.005 0.005 0.005	 UI (rms) UI (rms) UI (rms)	 rms jitter Not specified in GR-253 rms jitter rms jitter
Reference Clock Frequency Tolerance	-100		+100	ppm	
Acquisition Lock Time (OC-48) 19.44 MHz REFCLK 155.52 MHz REFCLK			 1800 250	µsec	Minimum transition density of 20%. Guaranteed but not tested. With device already powered up and valid ref. clk.
Reference Clock Input Duty Cycle	40		60	% of UI	
Reference Clock Rise & Fall Times			1.5	ns	20% to 80% of amplitude.
CML Output Rise & Fall Times		60	120	ps	20% to 80%, 50 Ω load, 1 pF cap.
Frequency difference at which the PLL goes out of lock (REFCLK compared to the divided down VCO clock)	450	600	770	ppm	
Frequency difference at which the receive PLL goes into lock (REFCLK compared to the divided down VCO clock)	220	300	390	ppm	
t_{SU} OC-48/Fibre Channel (2125 Mbps) OC-24/Fibre Channel (1062.5 Mbps) OC-12 OC-3	 100 250 500 2500			ps	See Figure 8.
t_H OC-48/Fibre Channel (2125 Mbps) OC-24/Fibre Channel (1062.5 Mbps) OC-12 OC-3	 100 250 500 2500			ps	See Figure 8.

Figure 8. Receiver Output Timing Diagram



Note: Output propagation delay time of high speed CML outputs is the time in pico seconds from the cross-over point of the reference signal to the cross-over point of the output.

Table 8. Jitter Tolerance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Jitter Tolerance STS-48	0.4	0.5		UI	1 MHz < f < 5 MHz Data Pattern = 2^7-1 PRBS
Jitter Tolerance STS-24					
Jitter Tolerance STS-12	0.4	0.6		UI	250 kHz < f < 5 MHz Data Pattern = 2^7-1 PRBS
Jitter Tolerance STS-3	0.4	0.8		UI	65 kHz < f < 1 MHz Data Pattern = 2^7-1 PRBS

Table 9. Gigabit Ethernet Jitter Specifications

Parameter	Min	Typ	Max	Units	Conditions
t_J Total Input Jitter Tolerance	599			ps	As specified in IEEE 802.3z.
t_{DJ} Deterministic Input Jitter Tolerance	370			ps	As specified in IEEE 802.3z.

Table 10. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias (Industrial)	-40		+85	˚C
Voltage on V_{CC} with respect to GND	3.135	3.3	3.465	V
Voltage on any LVTTL Input Pin	0		V_{CC}	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
I_{CC} Supply Current[1]		187	245	mA

1. Outputs open.

Table 11. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		+150	˚C
Voltage on V_{CC} with respect to GND	-0.5		3.465	V
Voltage on any LVTTL Input Pin	-0.5		V_{CC}	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
LVTTL Output Sink Current			8	mA
LVTTL Output Source Current			8	mA

Electrostatic Discharge (ESD) Ratings

The S3076 is rated to the following voltages based on the human body model:

1. All pins are rated 1500 Volts except pin # 24(VCC), 37(AVCC), 38(AGND), 41(AGND), 42(AVCC), and 43(AGND). Pins 24, 37, 38, 41, 42, and 43 are rated at 100 volts.

Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, "Protection of Electrical and Electronic Parts, Assemblies and Equipment." Contact your local FAE or sales representative for applicable ESD application notes.

Table 12. CML Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1900	mV	See Figure 9.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		950	mV	See Figure 9.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 13. CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OL} (Data)	CML Output Low Voltage	V_{CC} -1.0		V_{CC} -0.65	V	100 Ω line-to-line.
V_{OH} (Data)	CML Output High Voltage	V_{CC} -0.35		V_{CC} -0.2	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$ (Data)	CML Serial Output Differential Voltage Swing	800		1600	mV	100 Ω line-to-line. See Figure 9.
$\Delta V_{OUTSINGLE}$ (Data)	CML Serial Output Single-ended Voltage Swing	400		800	mV	100 Ω line-to-line at 2.5 Gbps. See Figure 9.
V_{OL} (Clock)	CML Output Low Voltage	V_{CC} -1.5		V_{CC} -0.85	V	100 Ω line-to-line.
V_{OH} (Clock)	CML Output High Voltage	V_{CC} -0.5		V_{CC} -0.25	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$ (Clock)	CML Serial Output Differential Voltage Swing	800		1800	mV	100 Ω line-to-line. See Figure 9.
$\Delta V_{OUTSINGLE}$ (Clock)	CML Serial Output Single-ended Voltage Swing	400		900	mV	100 Ω line-to-line at 2.5 GHz. See Figure 9.

Table 14. LVTTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage	2.0		3.465	V	TTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	TTL V_{CC} = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.4			V	V_{IH} = Min V_{IL} = Max I_{OH} = -100 µA
V_{OL}	Output Low Voltage			0.5	V	V_{IH} = Min V_{IL} = Max I_{OL} = 1.0 mA

Note: All parameters are specified with respect to the source termination and ground with V_{TTL} = Max. = 3.465 V.

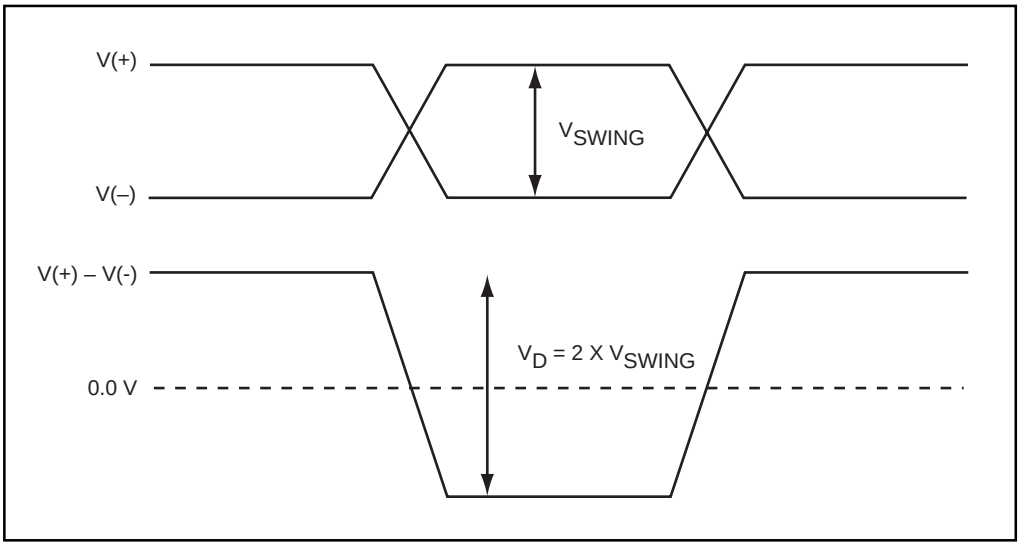
Table 15. Single Ended LVPECL Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} -2.00		V_{CC} -1.4	V	
V_{IH}	Input High Voltage	V_{CC} -1.2		V_{CC} -0.5	V	
I_{IL}	Input Low Current	-100		0	µA	
I_{IH}	Input High Current	+50		350	µA	

Table 16. Internally Biased Differential LVPECL Input AC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	V_{CC} -2.00		V_{CC} -1.4	V	
V_{IH}	Input High Voltage	V_{CC} -1.2		V_{CC} -0.5	V	
I_{IL}	Input Low Current	-300		0	µA	$V_{IL} = V_{CC}$ -2
I_{IH}	Input High Current	-50		100	µA	$V_{IH} = V_{CC}$ -0.5
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 9.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 9.

Figure 9. Differential Voltage Measurement



Note: V(+) – V(-) is the algebraic difference of the input signals.

Figure 10. +5 V Differential PECL Driver to S3076 Differential CML Input AC Coupled Termination

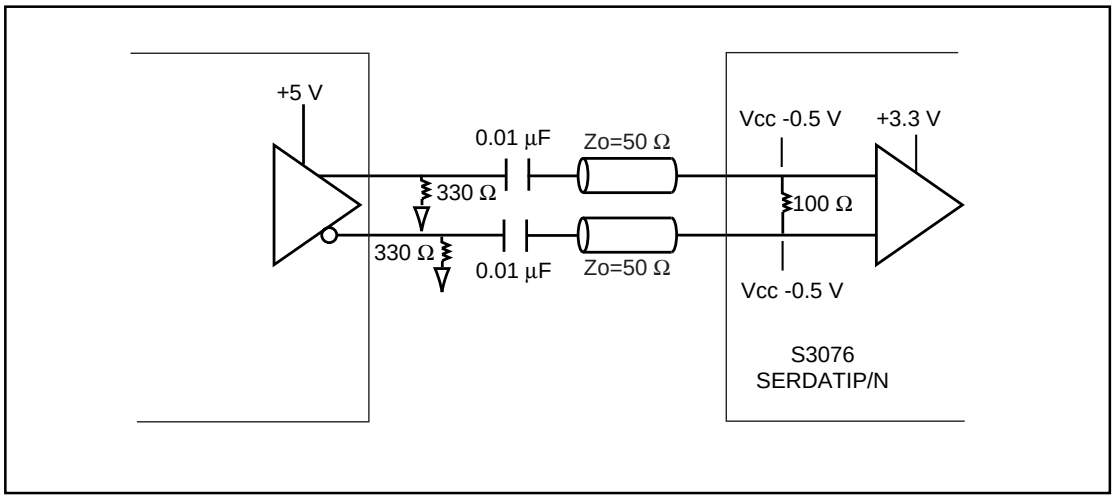


Figure 11. S3076 Differential CML Output to S3057/S3067 Terminations

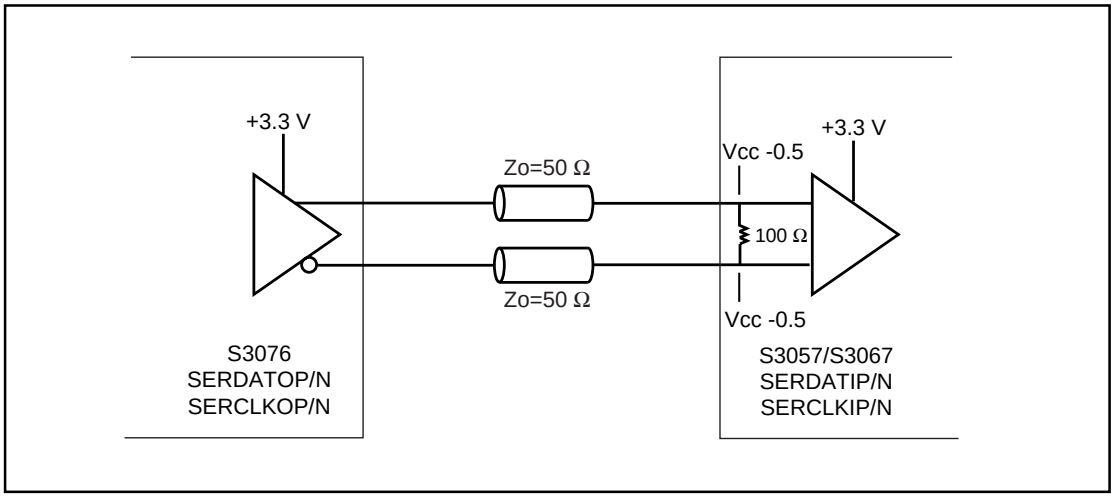


Figure 12. +5 V Differential PECL Driver to S3076 Reference Clock Input AC Coupled Termination

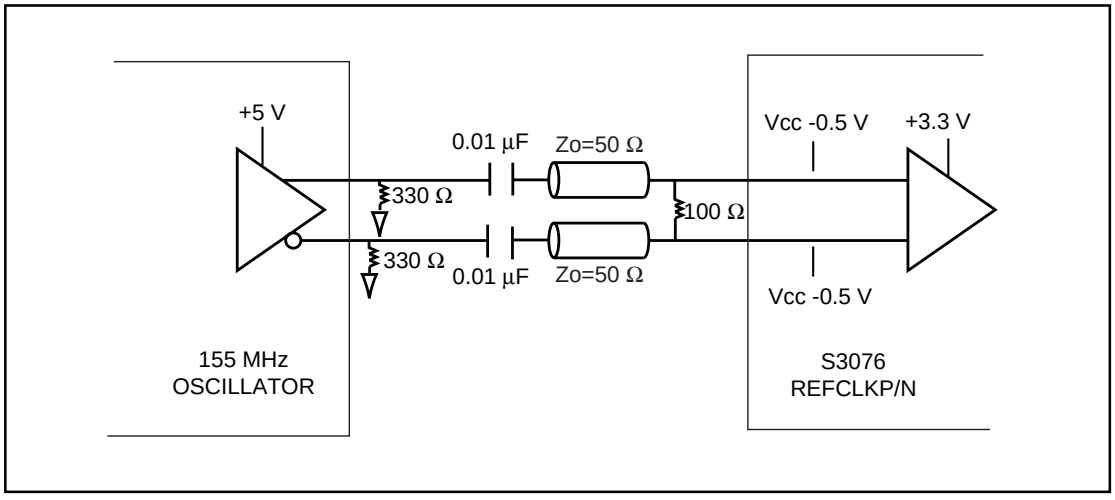


Figure 13. +3 V Differential LVPECL Driver to S3076 Reference Clock Input DC Coupled Termination

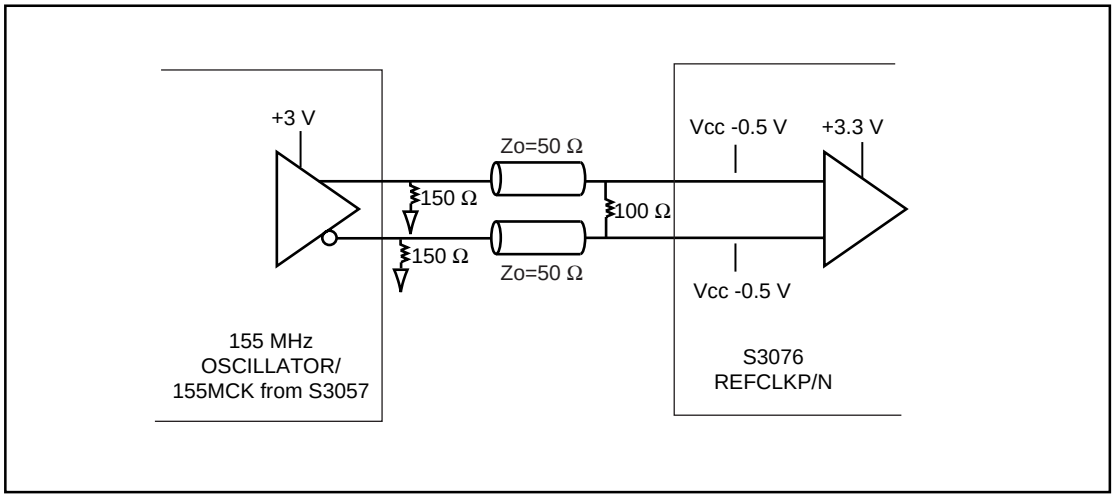
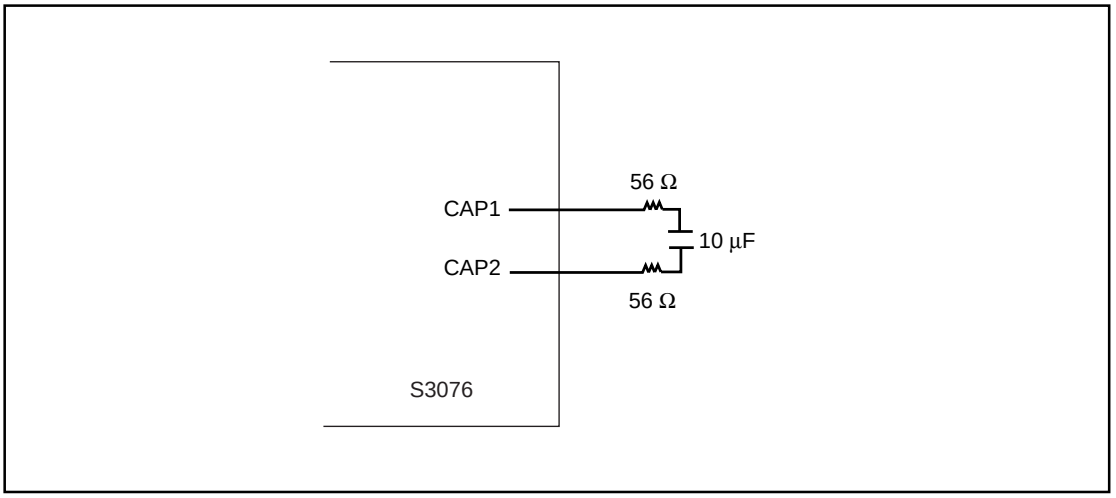
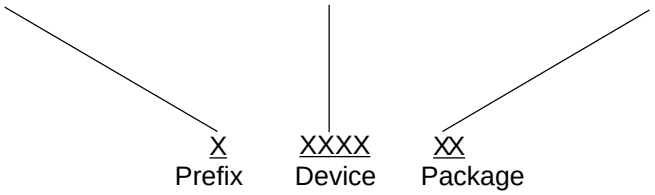


Figure 14. Loop Filter Capacitor Connections



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3076	TT – 48 Pin TQFP/TEP DI – Die



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Phone: (858) 450-9333 • (800)755-2622 • Fax: (858) 450-9885
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