General Description

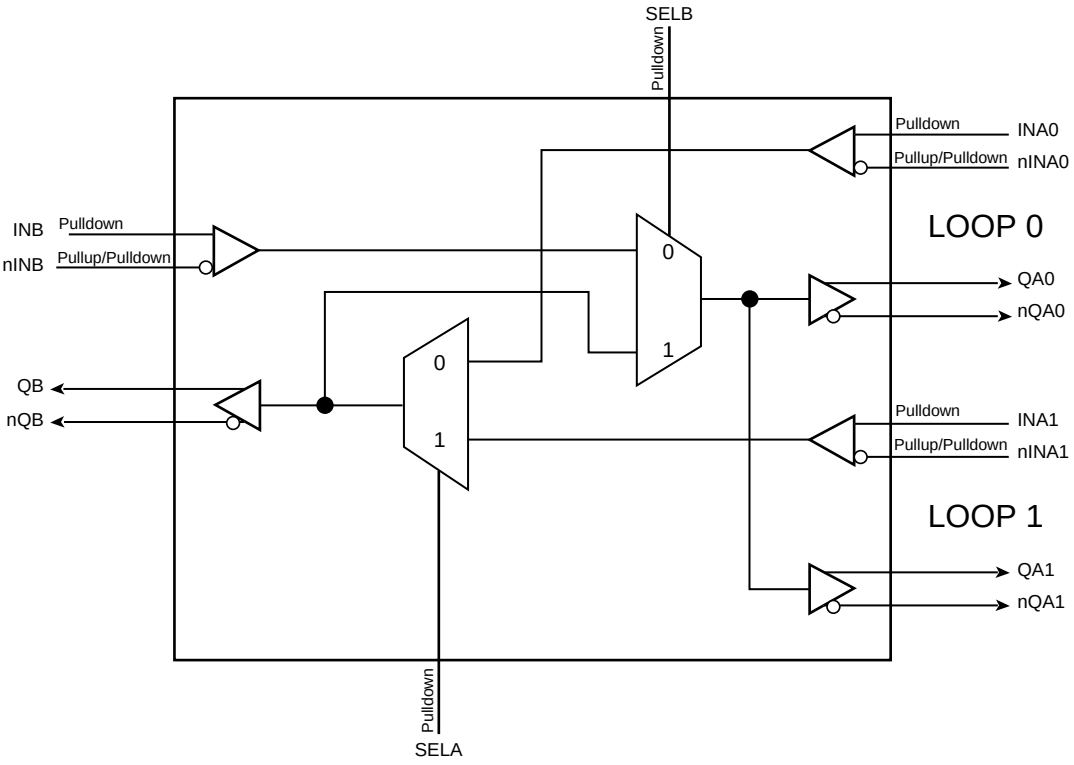
The 853S54I-01 is a 2:1/1:2 Multiplexer. The 2:1 Multiplexer allows one of 2 inputs to be selected onto one output pin and the 1:2 MUX switches one input to one of two outputs. This device may be useful for multiplexing multi-rate Ethernet PHYs which have 100Mbit and 1000Mbit transmit/receive pairs onto an optical SFP module which has a single transmit/receive pair. A 3RD mode allows loop back testing and allows the output of a PHY transmit pair to be routed to the PHY input pair. For examples, please refer to the Application Block diagrams on pages 2-3 of the data sheet.

The 853S54I-01 is optimized for applications requiring very high performance and has a maximum operating frequency in 2.5GHz. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

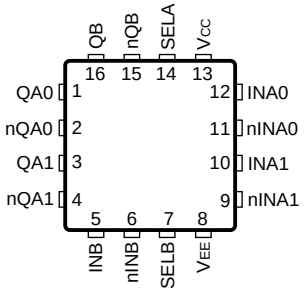
Features

- Dual 2:1, 1:2 MUX
- Three LVPECL output pairs
- Three differential clock inputs can accept: LVPECL, LVDS, CML
- Loopback test mode available
- Maximum output frequency: 2.5GHz
- Propagation delay: 550ps (maximum)
- Part-to-part skew: 275ps (maximum)
- Additive phase jitter, RMS: 27fs (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



853S54I-01

16-Lead VFQFN
3mm x 3mm x 0.925mm
package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	QA1, nQA1	Output		Differential output pair. LVPECL/ECL interface levels.
5	INB	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
6	nINB	Input	Pullup/ Pulldown	Inverting LVPECL differential clock input. $V_{CC}/2$ default when left floating.
7	SELB	Input	Pulldown	Select pin for QB output. See Table 3. LVCMOS/LVTTL interface levels.
8	V_{EE}	Power		Negative supply pin.
9	nINA1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
10	INA1	Input	Pulldown	Non-inverting differential LVPECL clock input.
11	nINA0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
12	INA0	Input	Pulldown	Non-inverting differential clock input.
13	V_{CC}	Power		Power supply pin.
14	SELA	Input	Pulldown	Select pin for QAx outputs. See Table 3. LVCMOS/LVTTL interface levels.
15, 16	nQB, QB	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37.5		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			37.5		kΩ

Function Tables

Table 3. Control Input Function Table

Control Inputs		
SELA	SELB	Mode
0	0	LOOP 0 selected
1	0	LOOP 1 selected
0	1	Loopback mode: LOOP 0
1	1	Loopback mode: LOOP 1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V TO 3.465V, V_{EE} = 0V OR V_{CC} = 0V, V_{EE} = -3.465V TO -2.375V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				45	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.375V TO 3.465V, V_{EE} = 0V OR V_{CC} = 0V, V_{EE} = -3.465V TO -2.375V,
T_A = 40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	0		0.8	V
			V_{CC} = 2.625V	0		0.7	V
I_{IH}	Input High Current	SELA, SELB	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SELA, SELB	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		V_{CC}-1.125	V_{CC}-1.025	V_{CC}-0.875	V_{CC}-1.075	V_{CC}-1.005	V_{CC}-0.880	V_{CC}-1.015	V_{CC}-0.97	V_{CC}-0.885	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC}-1.895	V_{CC}-1.755	V_{CC}-1.62	V_{CC}-1.875	V_{CC}-1.78	V_{CC}-1.685	V_{CC}-1.86	V_{CC}-1.765	V_{CC}-1.67	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 2		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input High Current	INAx, INB nINA, nINB			150			150			150	µA
I_{IL}	Input Low Current	INAx, INB	-10			-10			-10			µA
		nINA, nINB	-150			-150			-150			µA

NOTE: Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.165V to -0.925V.
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for INAx, nINAx and INB, nINB is V_{CC} + 0.3V.

Table 4D. ECL DC Characteristics, V_{EE} = -3.465V to -2.375V, V_{CC} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.0875	-1.075	-1.005	-0.880	-1.015	-0.97	-0.885	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 2		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1		V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
I_{IH}	Input High Current	INAx, INB nINA, nINB			150			150			150	µA
I_{IL}	Input Low Current	INAx, INB	-10			-10			-10			µA
		nINA, nINB	-150			-150			-150			µA

NOTE: Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for INAx, nINAx and INB, nINB is V_{CC} + 0.3V.

AC Electrical Characteristics

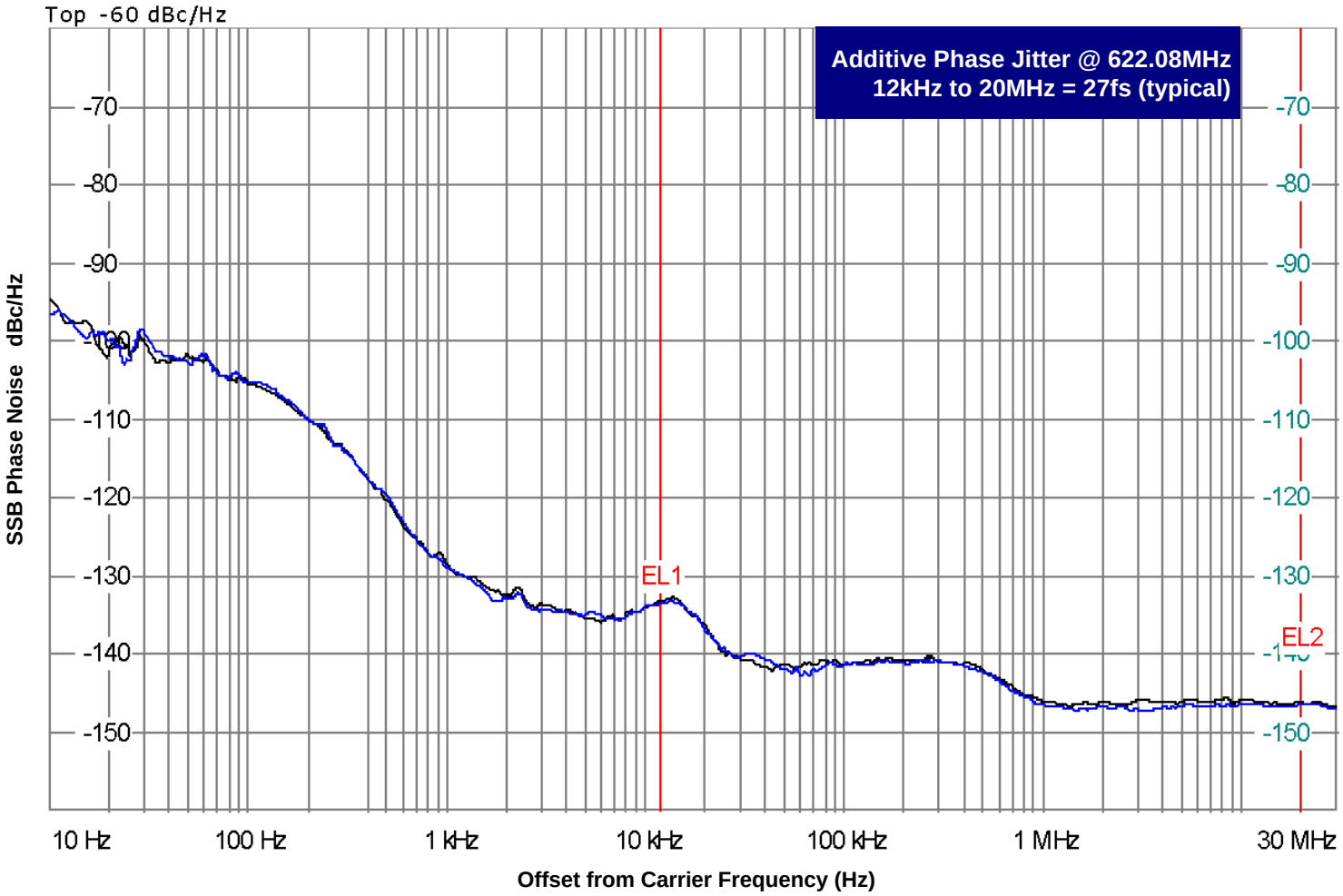
Table 5. AC Characteristics, V_{CC} = 2.375V TO 3.465V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1	INAx to QB	225		525	ps
		INB to QAx	200		475	ps
		INAx to QAx	250		550	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				275	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	*ƒ* = 622.08MHz, 12kHz – 20MHz		27		fs
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		325	ps
$MUX_{\_ISOLATION}$	MUX Isolation; NOTE 4	*ƒ* = 622.08MHz; Input Peak-to-Peak = 800mV		61		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at ≤ 1.3GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Q, nQ output measured differentially. See MUX Isolation Diagram in Parameter Measurement Information section.

Additive Phase Jitter

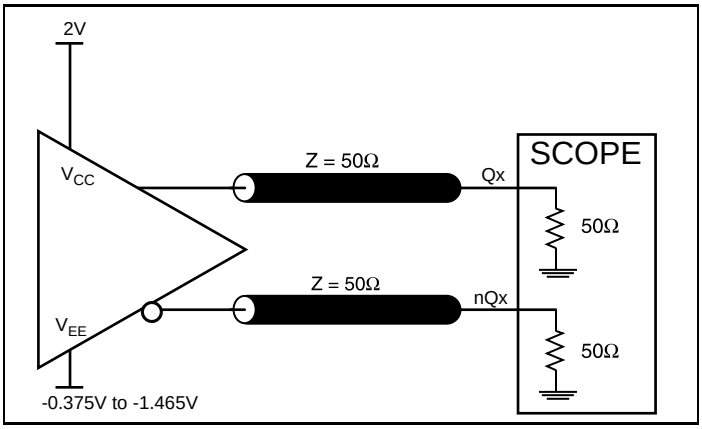
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



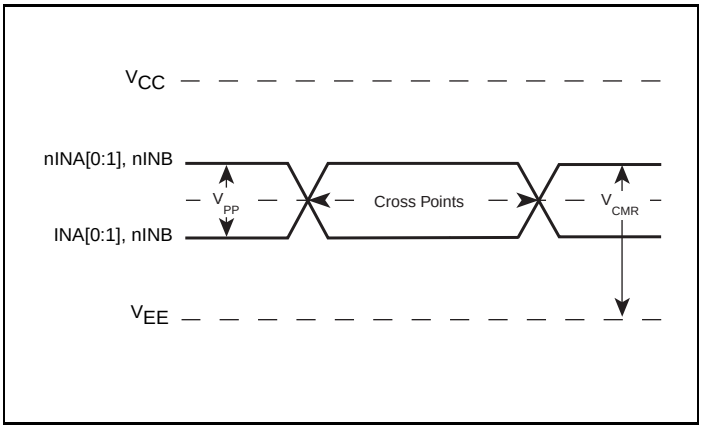
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Rohde & Schwarz SMA100A Signal Generator 9kHz – 6GHz as external input to Agilent 8133A 3GHz Pulse Generator.

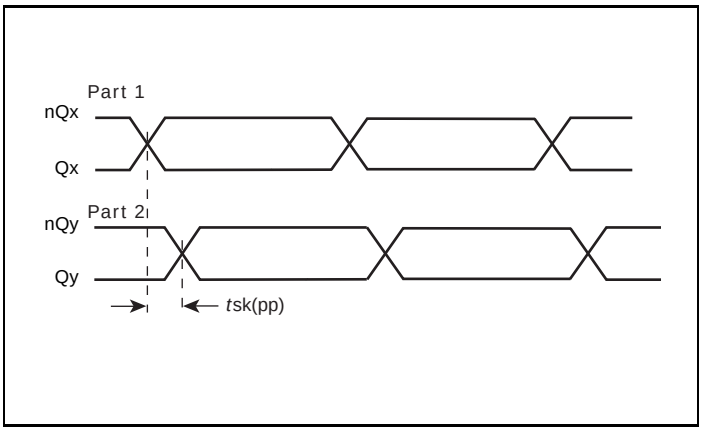
Parameter Measurement Information



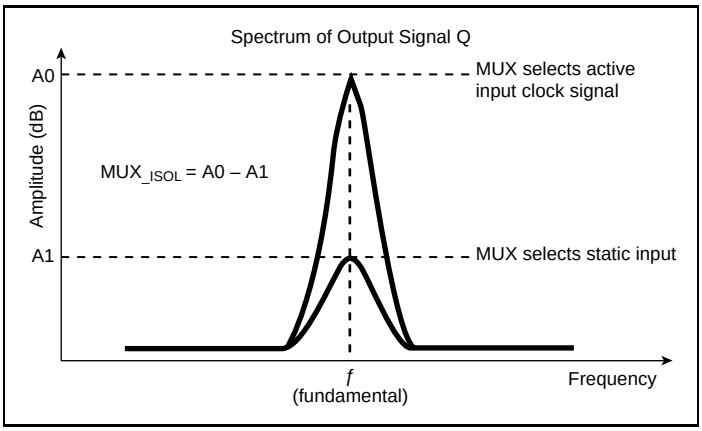
LVPECL Output Load AC Test Circuit



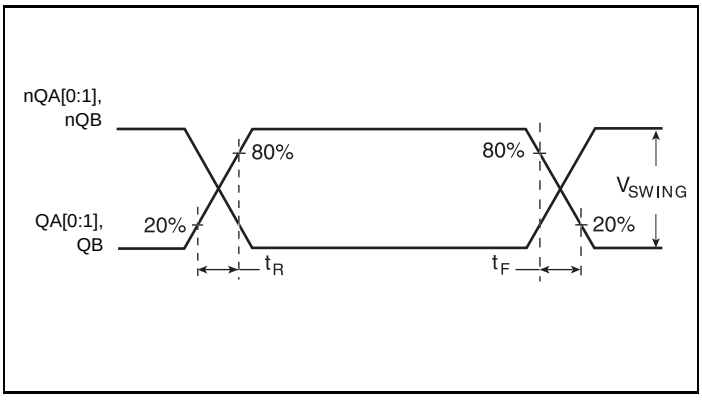
Differential Input Level



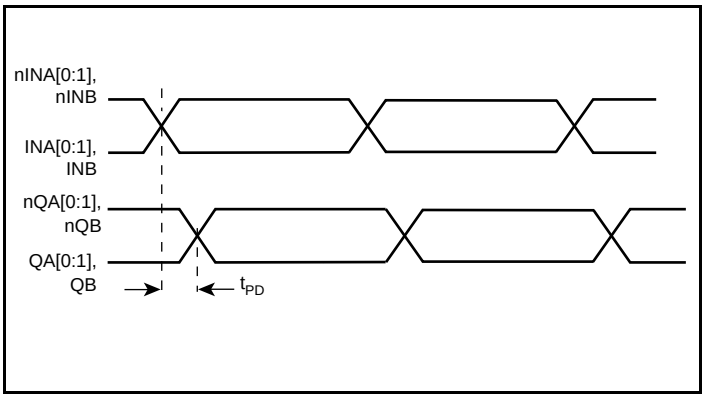
Part-to-Part Skew



MUX Isolation



Output Rise/Fall Time



Propagation Delay

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

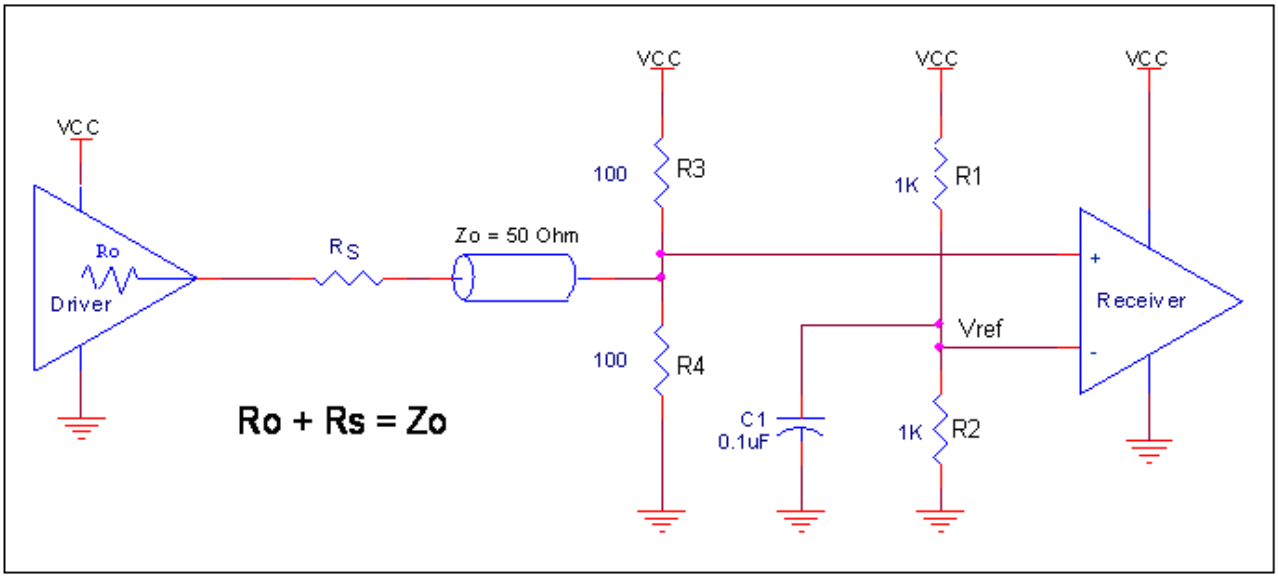


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs:

IN/nIN Inputs

For applications not requiring the use of the differential input, both INx and nINx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from INx to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

3.3V Differential Clock Input Interface

The IN /nIN accepts LVPECL, CML, LVDS and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2D* show interface examples for the IN /nIN input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

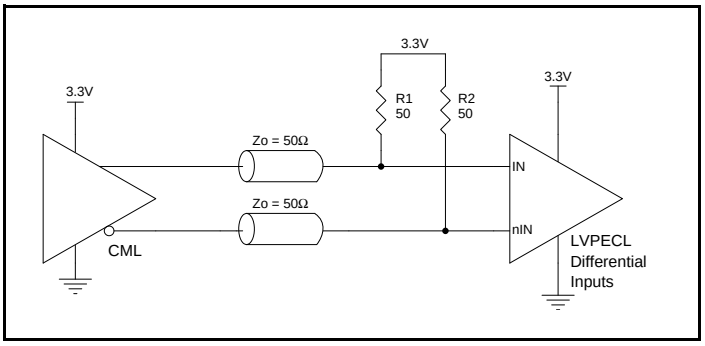


Figure 2A. IN/nIN Input Driven by an Open Collector CML Driver

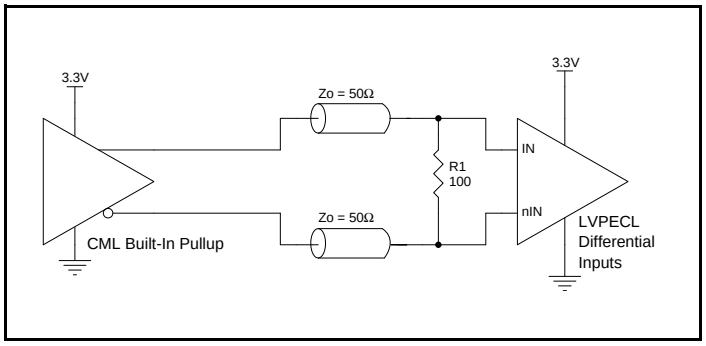


Figure 2B. IN/nIN Input Driven by a Built-In Pullup CML Driver

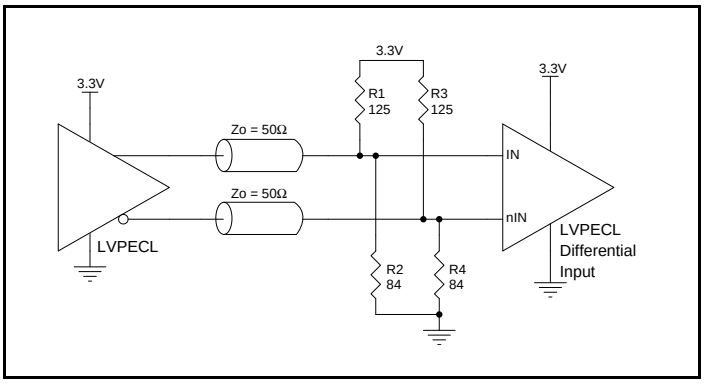


Figure 2C. IN/nIN Input Driven by a 3.3V LVPECL Driver

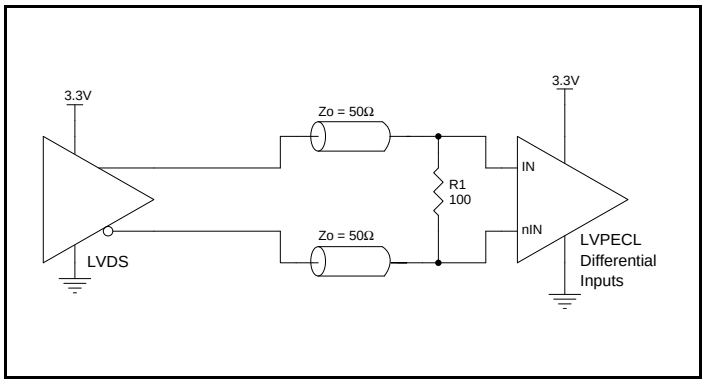


Figure 2D. IN/nIN Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The IN /nIN accepts LVPECL, CML, LVDS and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the IN /nIN input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

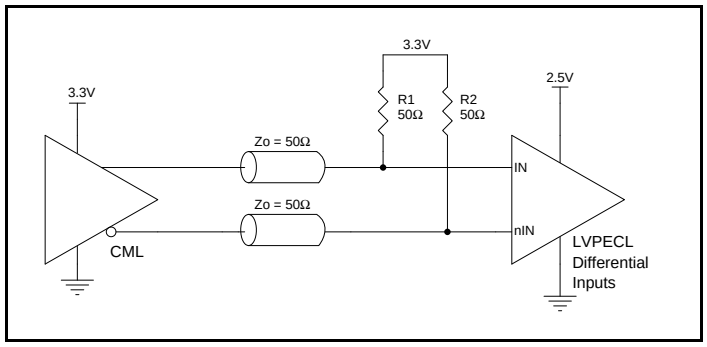


Figure 3A. IN/nIN Input Driven by an Open Collector CML Driver

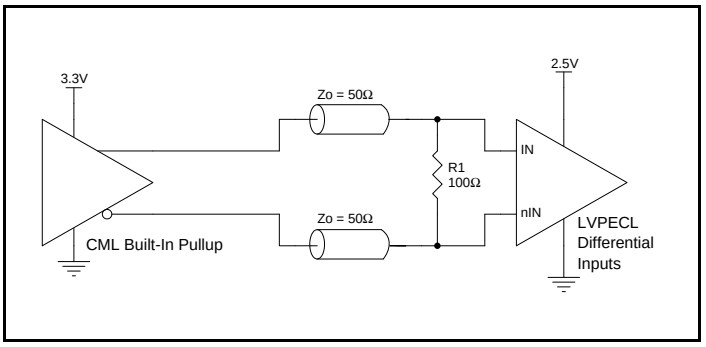


Figure 3B. IN/nIN Input Driven by a Built-In Pullup CML Driver

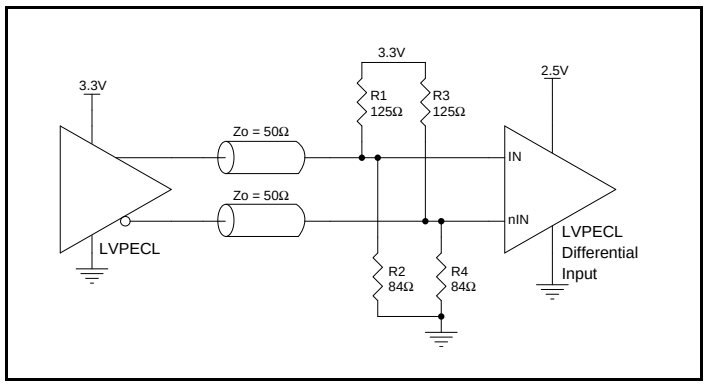


Figure 3C. IN/nIN Input Driven by a 3.3V LVPECL Driver

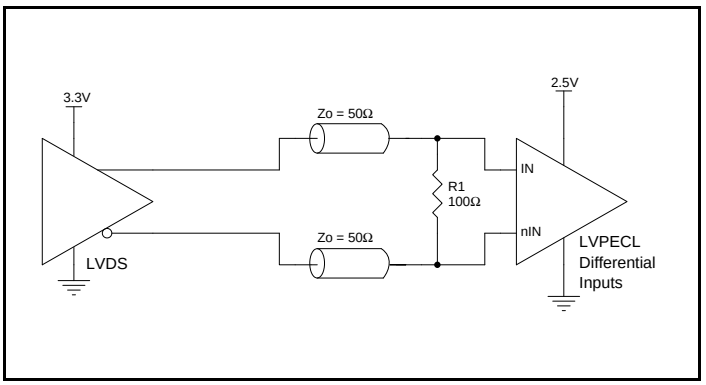


Figure 3D. IN/nIN Input Driven by a 3.3V LVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

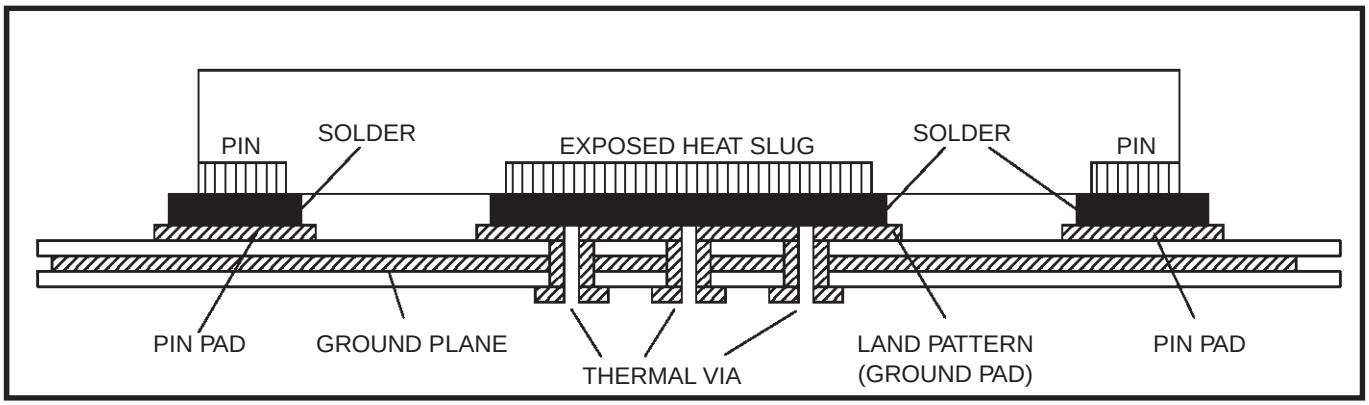


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

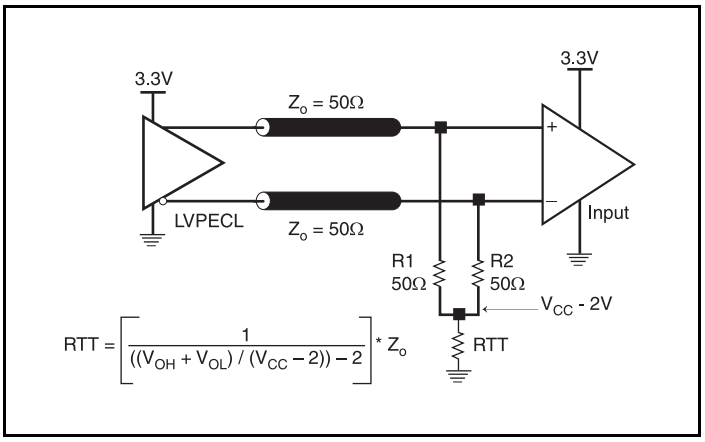


Figure 5A. 3.3V LVPECL Output Termination

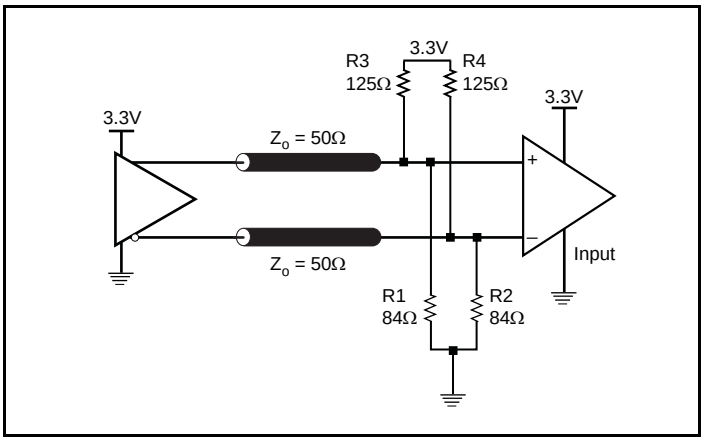


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

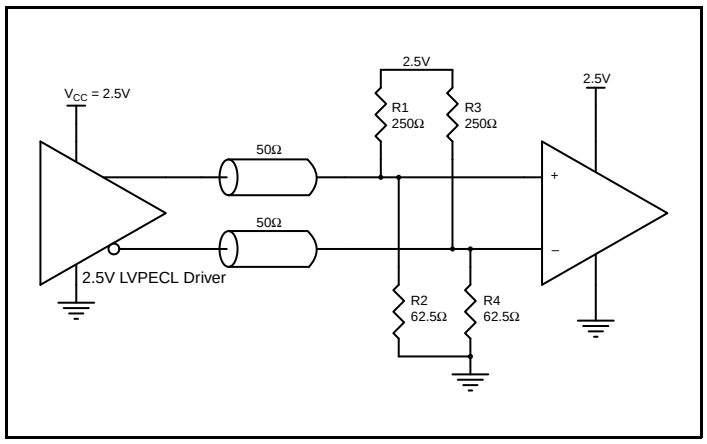


Figure 6A. 2.5V LVPECL Driver Termination Example

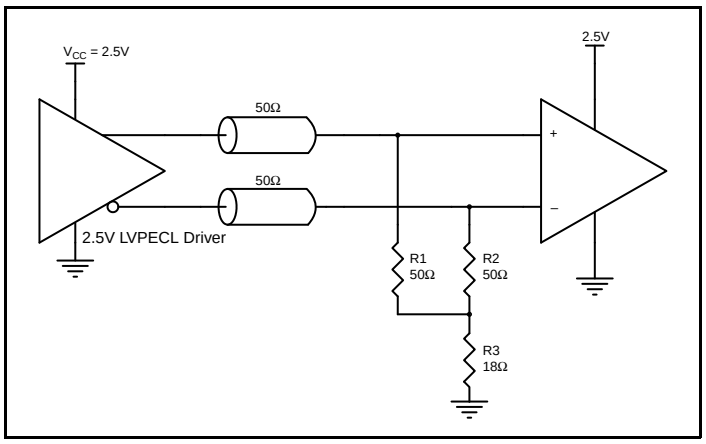


Figure 6B. 2.5V LVPECL Driver Termination Example

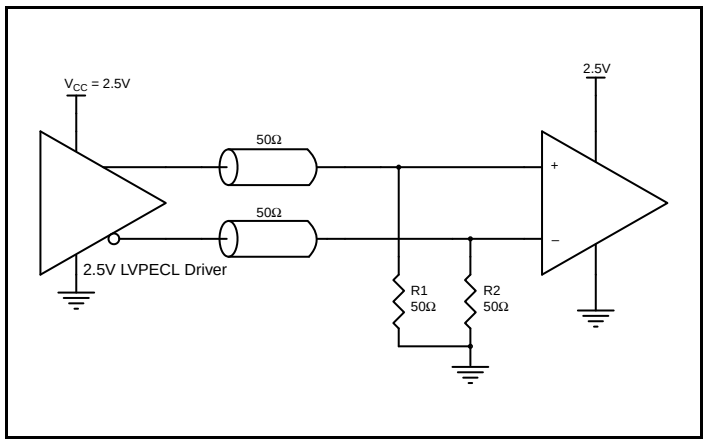


Figure 6C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 853S54I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 853S54I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 45mA = **155.925mW**
- Power $(outputs)_{MAX}$ = **30.75mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30.75mW = **92.25mW**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 155.925mW + 92.25mW = **248.175mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.248W * 74.7°C/W = 103.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7.*

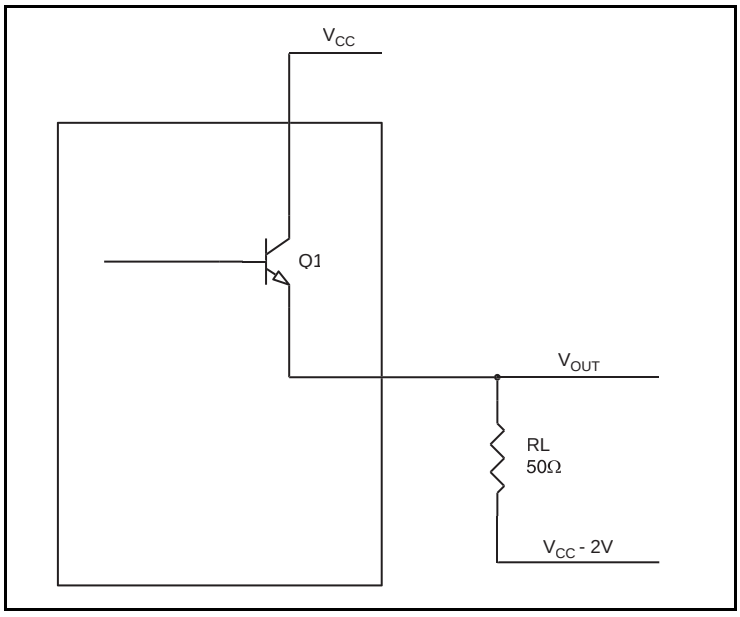


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CC_MAX} – 0.885V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **0.885V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CC_MAX} – 1.67V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.67V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
[(2V – 0.885V)/50Ω] * 0.885V = **19.73mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
[(2V – 1.67V)/50Ω] * 1.67V = **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.75mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

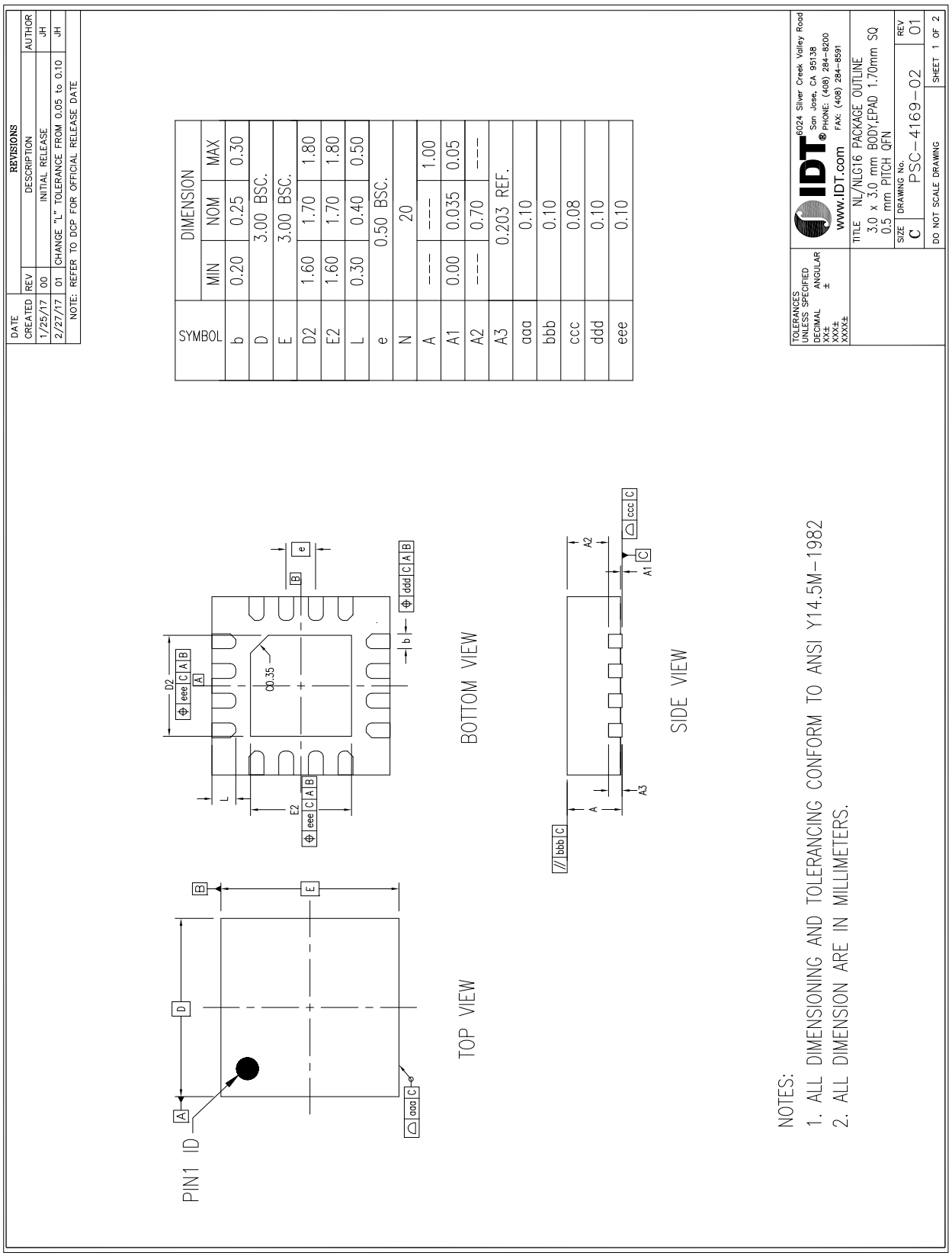
Transistor Count

The transistor count for 853S54I-01 is: 304

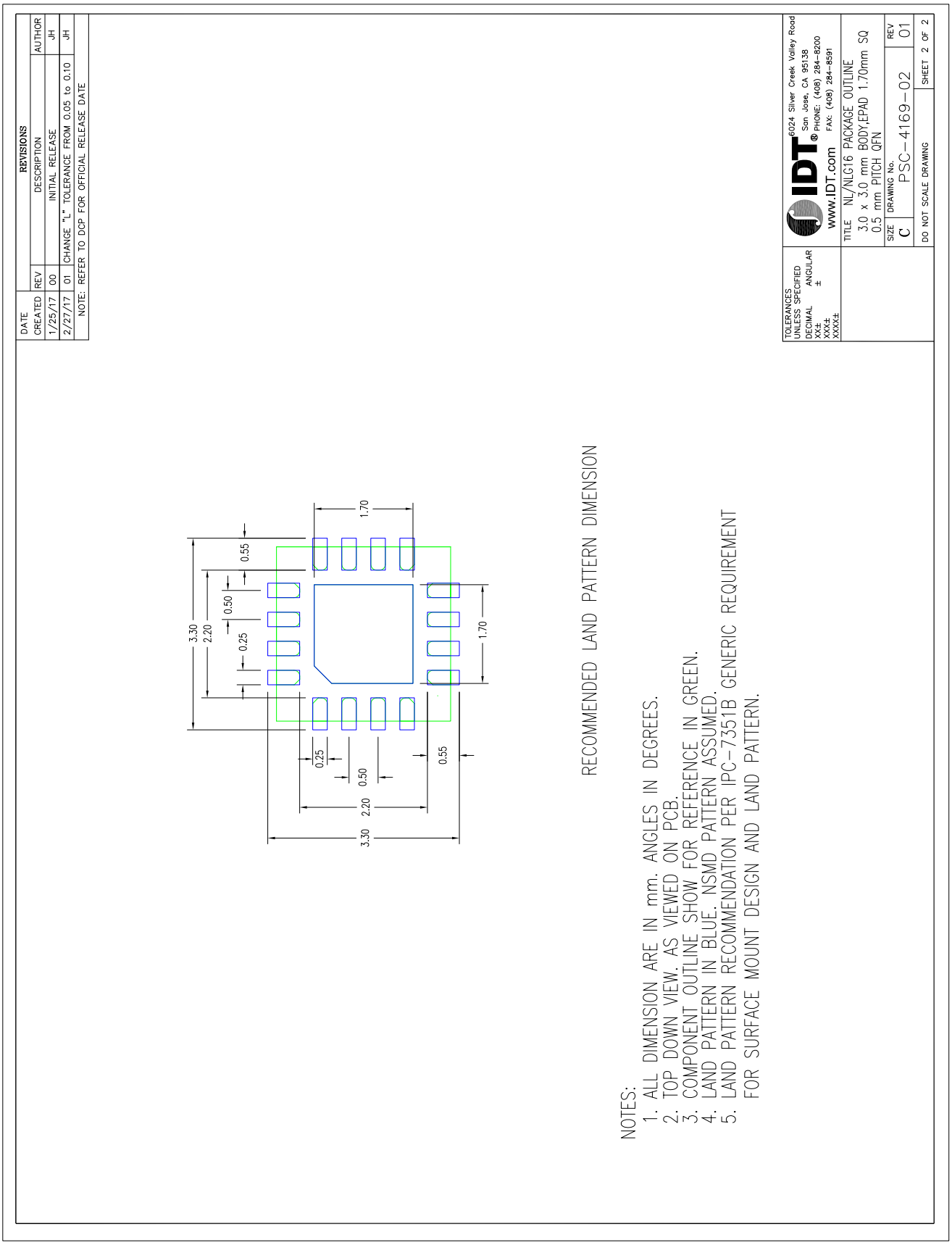
This device is pin and function compatible and a suggested replacement for 853S54I-01.

Package Outline and Package Dimensions

Package Outline - K Suffix for 16 Lead VFQFN



Package Outline - K Suffix for 16 Lead VFQFN, continued



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S54AKI-01LF	3A01	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
853S54AKI-01LFT	3A01	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Date	Description of Change
March 2, 2017	Page 2, Table 3. Control Input Function Table update. Pages 18-19. Updated ICS package drawing to IDT package drawing. Updated datasheet format.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support