256 MB 200-PIN DDR UNBUFFERED SODIMM
2.5 VOLT 32M x 64

Features

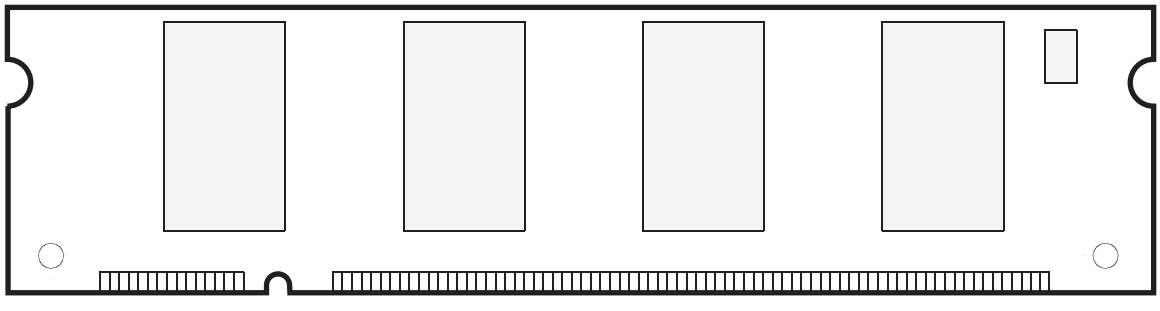
- JEDEC 200 Pin DDR Unbuffered Small-Outline, Dual In-Line memory module (SODIMM); 33,554,432 x 64 bit organization.
- Utilizes High Performance 16M x 16 DDR SDRAM in TSOPII-66 Packages
- Single +2.5V (± 0.2V) Power Supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All Inputs, Outputs are SSTL-2 Compatible
- 8192 Refresh Cycles every 64 ms
- Serial Presence Detect (SPD)
- DDR SDRAM Performance

	Component Used	-6	-7	-75	-8
t_{CK}	Clock Frequency (max.)	166 (PC333)	143 (PC266A)	133 (PC266B)	125 (PC200)
t_{AC}	Clock Access Time $\overline{\text{CAS}}$ Latency = 2.5	6	7	7.5	8

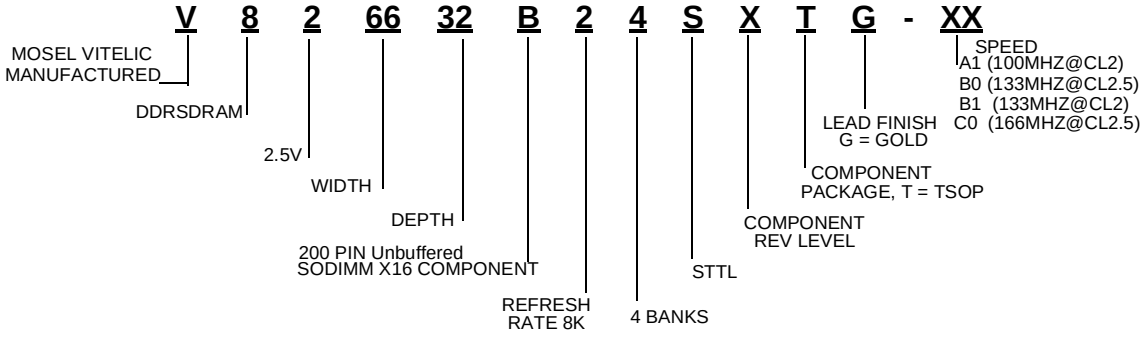
	Module Speed
A1	PC1600 (100MHz @ CL2)
B0	PC2100B (133MHz @ CL2.5)
B1	PC2100A (133MHz @ CL2)
C0	PC2700 (166MHz @ CL2.5)

Description

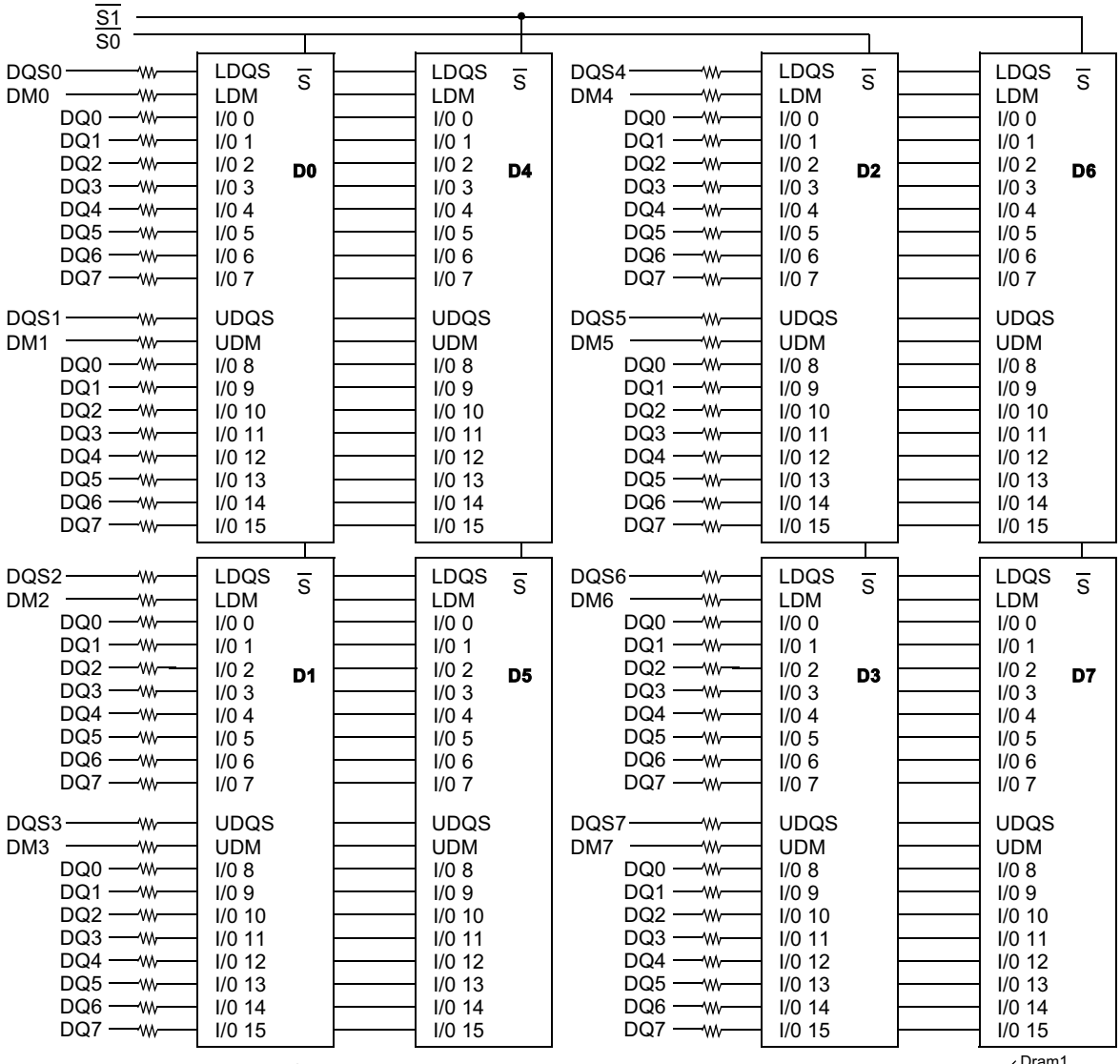
The V826632B24S memory module is organized 33,554,432 x 64 bits in a 200 pin memory module. The 32M x 64 memory module uses 8 Mosel-Vitelic 16M x 16 DDR SDRAM. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

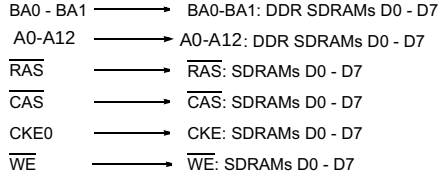


Part Number Information

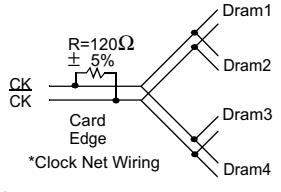


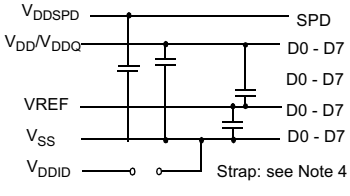
Block Diagram

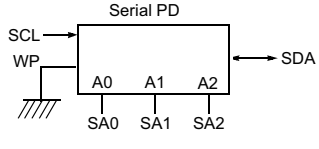




Clock Wiring	
Clock Input	SDRAMs
CK0/CK0 CK1/CK1 CK2/CK2	4 SDRAMs 4 SDRAMs NC







Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.

Pin Configurations (Front Side/Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	67	DQ27	135	DQ34	2	VREF	68	DQ31	136	DQ38
3	VSS	69	VDD	137	VSS	4	VSS	70	VDD	138	VSS
5	DQ0	71	CB0	139	DQ35	6	DQ4	72	CB4	140	DQ39
7	DQ1	73	CB1	141	DQ40	8	DQ5	74	CB5	142	DQ44
9	VDD	75	VSS	143	VDD	10	VDD	76	VSS	144	VDD
11	DQS0	77	DQS8	145	DQ41	12	DM0	78	DM8	146	DQ45
13	DQ2	79	CB2	147	DQS5	14	DQ6	80	CB6	148	DM5
15	VSS	81	VDD	149	VSS	16	VSS	82	VDD	150	VSS
17	DQ3	83	CB3	151	DQ42	18	DQ7	84	CB7	152	DQ46
19	DQ8	85	DU	153	DQ43	20	DQ12	86	DU/(RESET)	154	DQ47
21	VDD	87	VSS	155	VDD	22	VDD	88	VSS	156	VDD
23	DQ9	89	CK2	157	VDD	24	DQ13	90	VSS	158	$\overline{CK1}$
25	DQS1	91	$\overline{CK2}$	159	VSS	26	DM1	92	VDD	160	CK1
27	VSS	93	VDD	161	VSS	28	VSS	94	VDD	162	VSS
29	DQ10	95	CKE1	163	DQ48	30	DQ14	96	CKE0	164	DQ52
31	DQ11	97	DU(A13)	165	DQ49	32	DQ15	98	DU(BA2)	166	DQ53
33	VDD	99	A12	167	VDD	34	VDD	100	A11	168	VDD
35	CK0	101	A9	169	DQS6	36	VDD	102	A8	170	DM6
37	$\overline{CK0}$	103	VSS	171	DQ50	38	VSS	104	VSS	172	DQ54
39	VSS	105	A7	173	VSS	40	VSS	106	A6	174	VSS
Key		107	A5	175	DQ51	Key		108	A4	176	DQ55
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60
43	DQ17	111	A1	179	VDD	44	DQ21	112	A0	180	VDD
45	VDD	113	VDD	181	DQ57	46	VDD	114	VDD	182	DQ61
47	DQS2	115	A10/AP	183	DQS7	48	DM2	116	BA1	184	DM7
49	DQ18	117	BA0	185	DQ58	50	DQ22	118	$\overline{RAS}$	186	VSS
51	VSS	119	$\overline{WE}$	187	DQ58	52	VSS	120	$\overline{CAS}$	188	DQ62
53	DQ19	121	$\overline{S0}$	189	DQ59	54	DQ23	122	$\overline{S1}$	190	DQ63
55	DQ24	123	DU	191	VDD	56	DQ28	124	DU	192	VDD
57	VDD	125	VSS	193	SDA	58	VDD	126	VSS	194	SA0
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1
61	DQS3	129	DQ33	197	VDDSPD	62	DM3	130	DQ37	198	SA2
63	VSS	131	VDD	199	VDDID	64	VSS	132	VDD	200	DU
65	DQ26	133	DQS4			66	DQ30	134	DM4		

Notes:

* These pins are not used in this module.

Pin Names

Pin	Pin Description
A0~A12	Address Input (Multiplexed)
BA0~BA1	Bank Select Address
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Strobe Input/Output
CK0~CK2, $\overline{CK0}$~$\overline{CK2}$,	Clock Input
CKE0	Clock Enable Input
$\overline{S0}$, $\overline{S1}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DM0~DM7	Data - In Mask

Pin	Pin Description
VDD	Power Supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power Supply for Reference
VDDSPD	Serial EEPOM Power Supply (2.3V to 3.6V)
SDA	Serial Data I/O
SCL	Serial Clock
SA0~2	Address in EEPROM
VDDID	VDD Identification Flag
NC	No Connection

Serial Presence Detect Information

Bin Sort:

A1 (PC1600 @ CL2)
B0 (PC2100B @ CL2.5)
B1 (PC2100A @ CL2)
C0 (PC2700 @ CL2.5)

Byte #	Function described	Function Supported				Hex value			
		A1	B0	B1	C0	A1	B0	B1	C0
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes				80h			
1	Total # of Bytes of SPD memory device	256bytes				08h			
2	Fundamental memory type	SDRAM DDR				07h			
3	# of row address on this assembly	13				0Dh			
4	# of column address on this assembly	9				09h			
5	# of module Rows on this assembly	2 Bank				02h			
6	Data width of this assembly	64 bits				40h			
7	.....Data width of this assembly	-				00h			
8	VDDQ and interface standard of this assembly	SSTL 2.5V				04h			
9	DDR SDRAM cycle time at CAS Latency =2.5	8ns	7.5ns	7ns	6ns	80h	75h	70h	60h
10	DDR SDRAM Access time from clock at CL=2.5	±0.8ns	±0.75ns	±0.75ns	±0.70ns	80h	75h	75h	70h
11	DIMM configuration type(Non-parity, Parity, ECC)	Non-parity, ECC				00h			
12	Refresh rate & type	7.8us & Self refresh				82h			
13	Primary DDR SDRAM width	x16				10h			
14	Error checking DDR SDRAM data width	N/A				00h			
15	Minimum clock delay for back-to-back random column address	t_{CCD}=1CLK				01h			
16	DDR SDRAM device attributes : Burst lengths supported	2,4,8				0Eh			
17	DDR SDRAM device attributes : # of banks on each DDR SDRAM	4 banks				04h			
18	DDR SDRAM device attributes : CAS Latency supported	2,2.5				0Ch			
19	DDR SDRAM device attributes : CS Latency	0CLK				01h			
20	DDR SDRAM device attributes : WE Latency	1CLK				02h			
21	DDR SDRAM module attributes	Differential clock / non Registered				20h			
22	DDR SDRAM device attributes : General	+/-0.2V voltage tolerance				00h			
23	DDR SDRAM cycle time at CL =2	10ns	10ns	7.5ns	7.5ns	A0h	A0h	75h	75h
24	DDR SDRAM Access time from clock at CL =2	±0.8ns	±0.75ns	±0.75ns	±0.70ns	80h	75h	75h	70h
25	DDR SDRAM cycle time at CL =1.5	-	-	-	-	00h			
26	DDR SDRAM Access time from clock at CL =1.5	-	-	-	-	00h			
27	Minimum row precharge time (=t_{RP})	20ns	20ns	20ns	18ns	50h	50h	50h	48h

Serial Presence Detect Information (cont.)

Byte #	Function described	Function Supported				Hex value			
		A1	B0	B1	C0	A1	B0	B1	C0
28	Minimum row activate to row active delay(=t_{RRD})	15ns	15ns	15ns	12ns	3Ch	3Ch	3Ch	30h
29	Minimum RAS to CAS delay(=t_{RCD})	20ns	20ns	20ns	18ns	50h	50h	50h	48h
30	Minimum active to precharge time(=t_{RAS})	50ns	45ns	45ns	42ns	32h	2Dh	2Dh	2Ah
31	Module ROW density	128MB				20h			
32	Command and address signal input setup time	1.1ns	0.9ns	0.9ns	0.75ns	B0h	90h	90h	75h
33	Command and address signal input hold time	1.1ns	0.9ns	0.9ns	0.75ns	B0h	90h	90h	75h
34	Data signal input setup time	0.6ns	0.5ns	0.5ns	0.45ns	60h	50h	50h	45h
35	Data signal input hold time	0.6ns	0.5ns	0.5ns	0.45ns	60h	50h	50h	45h
36-40	Superset information (may be used in future)					00h			
41	SDRAM device minimum active to active/auto-refresh time (=t_{RC})	70ns	65ns	65ns	60ns	46h	41h	41h	3Ch
42	SDRAM device minimum active to autorefresh to active/auto-refresh time (=t_{RFC})	80ns	75ns	75ns	72ns	50h	4Bh	4Bh	48h
43	SDRAM device maximum device cycle time (=$t_{CK\ MAX}$)	12ns	12ns	12ns	12ns	30h	30h	30h	30h
44	SDRAM device maximum skew between DQS and DQ signals (=t_{DQSQ})	0.6ns	0.5ns	0.5ns	0.45ns	3Ch	32h	32h	2Dh
45	SDRAM device maximum read datahold skew factor (=t_{QHS})	1ns	0.75ns	0.75ns	0.60ns	A0h	75h	75h	60h
46-61	Superset information (may be used in future)	-				00h			
62	SPD data revision code	Initial release				00h			
63	Checksum for Bytes 0 ~ 62	-				CFh	0Ah	DAh	33h
64	Manufacturer JEDEC ID code	Mosel Vitelic				40h			
65 -71	..... Manufacturer JEDEC ID code					00h			
72	Manufacturing location	02=Taiwan 05=China 0A=S-CH							
73-90	Module part number (ASCII)	V826632B24S							
91	Manufacturer revison code (For PCB)	0				00			
92	Manufacturer revison code (For component)	0				00			
93	Manufacturing date (Week)	-				-			
94	Manufacturing date (Year)	-				-			
95~98	Assembly serial #	-				-			
99~127	Manufacturer specific data (may be used in future)	Undefined				00h			
128~255	Open for customer use	Undefined				00h			

DC Operating Conditions

(T_A = 0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Power Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1
Input High Voltage	V_{IH}	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	V_{REF} - 0.15	V	2
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	
Reference Voltage	V_{REF}	1.15	1.25	1.35	V	3
Input Leakage Current	I_I	-2	-	2	µA	
Output Leakage Current	IO_z	-5	-	5	µA	
Output High Current (V_{OUT} = 1.95V)	IO_H	-16.8	-	-	mA	
Output Low Current (V_{OUT} = 0.35V)	IO_L	16.8	-	-	mA	

Notes: 1. V_{DDQ} must not exceed the level of V_{DD}.
2. V_{IL} (min) is acceptable -1.5V AC pulse width <= 5ns of duration.
3. The value of V_{REF} is approximately equal to 0.5V_{DDQ}.

AC Operating Conditions

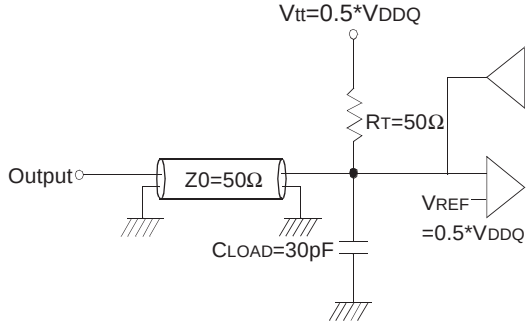
(T_A = 0 to 70 °C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH(AC)}$	V_{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	$V_{IL(AC)}$		V_{REF} - 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$V_{IX(AC)}$	0.5*$V_{DDQ-0.2}$	0.5*$V_{DDQ+0.2}$	V	2

Notes: 1. VID is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of VIX is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

AC Operating Test Conditions (T_A = 0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Value	Unit
Reference Voltage	V_{DDQ} x 0.5	V
Termination Voltage	V_{DDQ} x 0.5	V
AC Input High Level Voltage (V_{IH}, min)	V_{REF} + 0.31	V
AC Input Low Level Voltage (V_{IL}, max)	V_{REF} - 0.31	V
Input Timing Measurement Reference Level Voltage	V_{REF}	V
Output Timing Measurement Reference Level Voltage	V_{TT}	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (R_T)	50	Ohm
Series Resistor (R_S)	25	Ohm
Output Load Capacitance for Access Time Measurement (C_L)	30	pF



Output Load Circuit (SSTL_2)

Input/Output Capacitance

(V_{DD} = 2.5V, V_{DDQ} = 2.5V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA_0 ~ BA_1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	CIN_1	36	45	pF
Input capacitance (CKE_0)	CIN_2	36	45	pF
Input capacitance ($\overline{CS_0}$)	CIN_3	34	42	pF
Input capacitance (CLK_1, CLK_2)	CIN_4	34	38	pF
Data & DQS input/output capacitance (DQ_0~DQ_{63})	C_{OUT}	8	9	pF
Input capacitance (DM0~DM8)	CIN_5	8	9	pF

DDR SDRAM I_{DD} SPEC TABLE

Symbol		C0(DDR333@CL=2.5)	B1(DDR266@CL=2)	B0(DDR266@CL=2.5)	A1(DDR200@CL=2)	Unit	Notes
IDD0		590	560	560	460	mA	
IDD1		730	650	650	585	mA	
IDD2P		24	24	24	24	mA	
IDD2F		210	160	160	150	mA	
IDD2Q		165	150	150	130	mA	
IDD3P		285	245	245	210	mA	
IDD3N		450	370	370	330	mA	
IDD4R		1030	870	870	770	mA	
IDD4W		985	820	820	690	mA	
IDD5		950	850	850	760	mA	
IDD6	Normal	24	24	24	24	mA	
	Low power	15	15	15	15	mA	Optional
IDD7A		1640	1380	1380	1200	mA	

* Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

Detailed test conditions for DDR SDRAM IDD1 & IDD

IDD1 : Operating current: One bank operation

1. Typical Case : Vdd = 2.5V, T=25' C

2. Worst Case : Vdd = 2.7V, T= 10' C

3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA

4. Timing patterns
 - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
   Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst
 - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst
 - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Symbol	(PC333)		(PC266A)		(PC266B)		(PC200)		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
Row Cycle Time		t_{RC}	60	-	65	-	65	-	70	-	ns	
Auto Refresh Row Cycle Time		t_{RFC}	72	-	75	-	75	-	80	-	ns	
Row Active Time		t_{RAS}	42	120K	45	120K	45	120K	50	120K	ns	
Row Address to Column Address Delay		t_{RCD}	18	-	20	-	20	-	20	-	ns	
Row Active to Row Active Delay		t_{RRD}	12	-	15	-	15	-	15	-	ns	
Column Address to Column Address Delay		t_{CCD}	1	-	1	-	1	-	1	-	CLK	
Row Precharge Time		t_{RP}	18	-	20	-	20	-	20	-	ns	
Write Recovery Time		t_{WR}	12	-	15	-	15	-	15	-	ns	
Last Data-In to Read Command		t_{DRL}	1	-	1	-	1	-	1	-	CLK	
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	35	-	35	-	35	-	35	-	ns	
System Clock Cycle Time	$\overline{CAS}$ Latency = 2.5	t_{CK}	6	12	7	12	7.5	12	8	12	ns	
	$\overline{CAS}$ Latency = 2		7.5	12	7.5	12	10	12	10	12	ns	
Clock High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
Clock Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
Data-Out edge to Clock edge Skew		t_{AC}	-0.75	0.75	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.75	0.75	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.45	-	0.5	-	0.5	-	0.6	ns	
Data-Out hold time from DQS		t_{QH}	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	ns	1
Clock Half Period		t_{HP}	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	ns	1
Input Setup Time (fast slew rate)		t_{IS}	0.75	-	0.9	-	0.9	-	1.1	-	ns	2,3,5,6
Input Hold Time (fast slew rate)		t_{IH}	0.75	-	0.9	-	0.9	-	1.1	-	ns	2,3,5,6
Input Setup Time (slow slew rate)		t_{IS}	0.8	-	1.0	-	1.0	-	1.1	-	ns	2,4,5,6
Input Hold Time (slow slew rate)		t_{IH}	0.8	-	1.0	-	1.0	-	1.1	-	ns	2,4,5,6
Input Pulse Width		t_{IPW}	0.4	0.6	2.2	-	2.2	-	-	-	ns	6
Write DQS High Level Width		t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Write DQS Low Level Width		t_{DQSL}	0.75	1.25	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
CLK to First Rising edge of DQS-In		t_{DQSS}	0.45	-	0.75	1.25	0.75	1.25	0.75	1.25	CLK	
Data-In Setup Time to DQS-In (DQ & DM)		t_{DS}	0.45	-	0.5	-	0.5	-	0.6	-	ns	7
Data-in Hold Time to DQS-In (DQ & DM)		t_{DH}	1.75	-	0.5	-	0.5	-	0.6	-	ns	7
DQ & DM Input Pulse Width		t_{DIPW}	0.9	1.1	1.75	-	1.75	-	2	-	ns	
Read DQS Preamble Time		t_{RPRE}	0.4	0.6	0.9	1.1	0.9	1.1	0.9	1.1	CLK	
Read DQS Postamble Time		t_{RPST}	0	-	0.4	0.6	0.4	0.6	0.4	0.6	CLK	

AC Characteristics (cont.)

Parameter	Symbol	(PC333)		(PC266A)		(PC266B)		(PC200)		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write DQS Preamble Setup Time	t_{WPRES}	0.25	-	0	-	0	-	0	-	CLK	
Write DQS Preamble Hold Time	t_{WPREH}	0.4	0.6	0.25	-	0.25	-	0.25	-	CLK	
Write DQS Postamble Time	t_{WPST}	2	-	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Mode Register Set Delay	t_{MRD}	10	-	2	-	2	-	2	-	CLK	
Power Down Exit Time	t_{PDEX}	75	-	10	-	10	-	10	-	ns	
Exit Self Refresh to Non-Read Command	t_{XSNR}	200	-	75	-	75	-	80	-	ns	
Exit Self Refresh to Read Command	t_{XSRD}	-	7.8	200	-	200	-	200	-	CLK	8
Average Periodic Refresh Interval	t_{REFI}	**(PC333)**		-	7.8	-	7.8	-	7.8	us	

Notes: 1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
5. CK, $\overline{CK}$ slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(DQS) : DQ, DM
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.

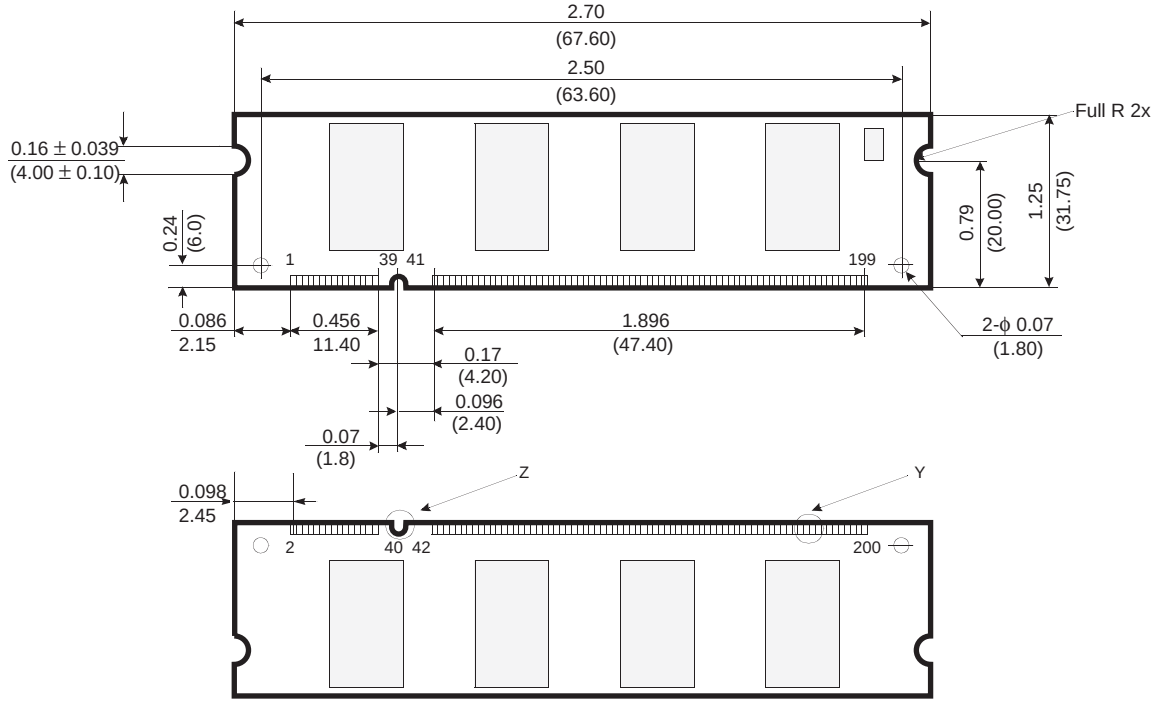
Absolute Maximum Ratings

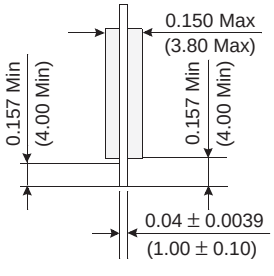
Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5 ~ 3.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 3.6	V
Output Short Circuit Current	I_{OS}	50	mA
Power Dissipation	P_D	8	W
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • Sec

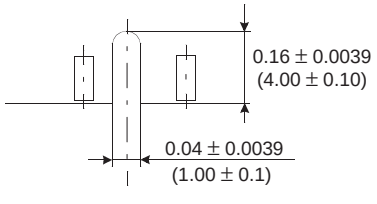
Note: Operation at above absolute maximum rating can adversely affect device reliability

Package Dimensions

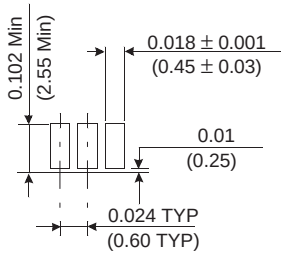
Units : Inches (Millimeters)







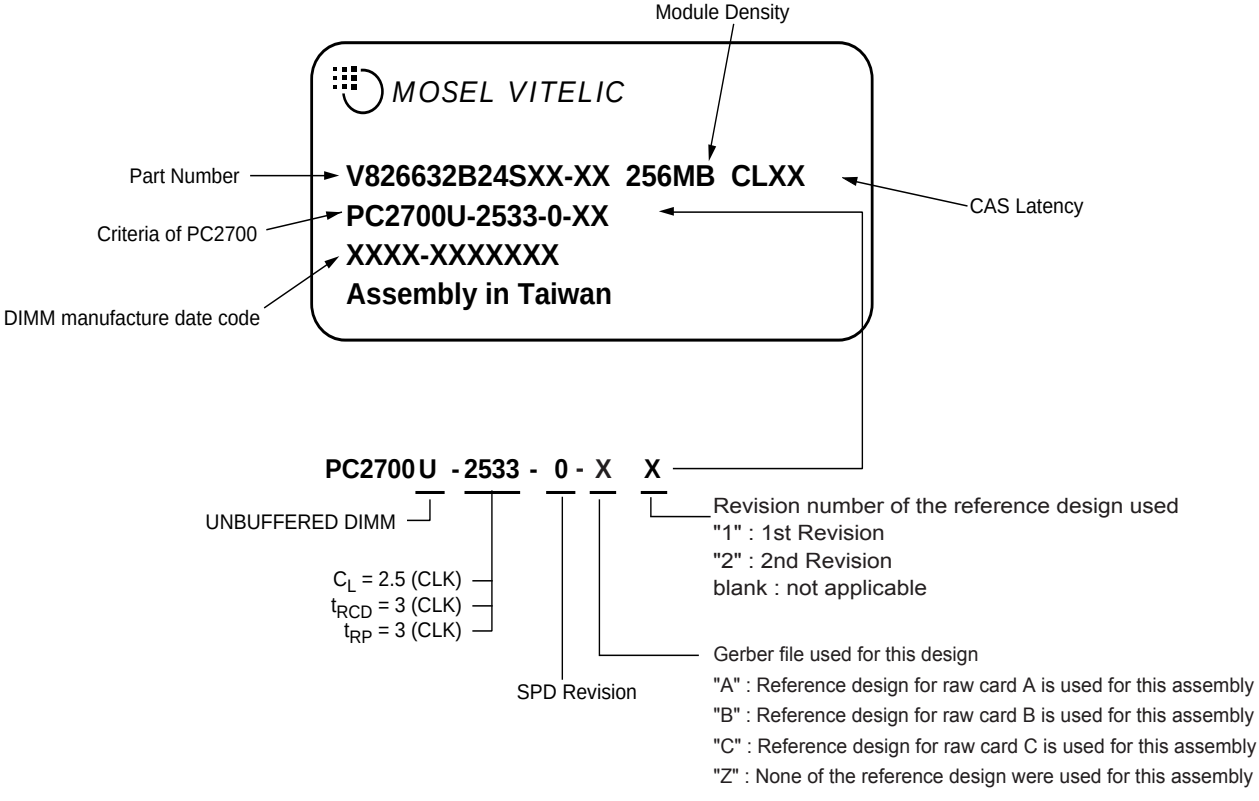
Detail Z

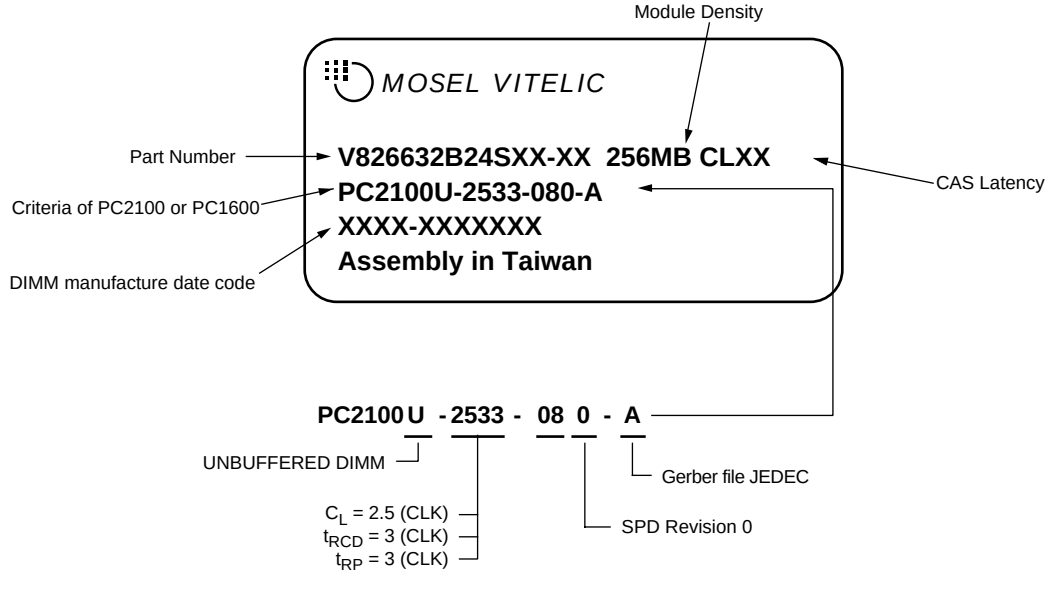


Detail Y

Tolerances : ±.006(.15) unless otherwise specified

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