4.5-V to 18-V, 3-A OUTPUT SYNCHRONOUS STEP DOWN SWITCHER WITH INTEGRATED FET (SWIFT™)

Check for Samples: TPS54325-Q1

FEATURES

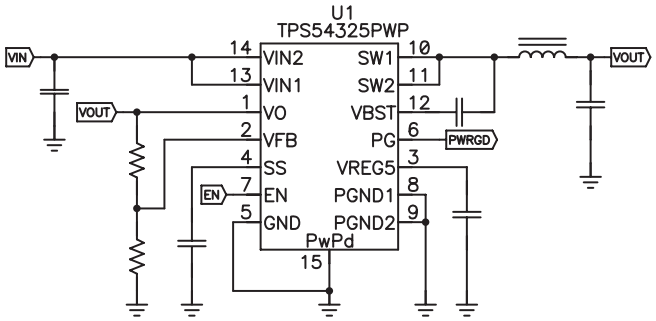
- **Qualified for Automotive Applications**
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide V_{CC} Input Voltage Range: 4.5 V to 18 V**
- **Wide V_{IN} Input Voltage Range: 2.0 V to 18 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Highly Efficient Integrated FET's Optimized for Lower Duty Cycle Applications**
  –120 mΩ (High Side) and 70 mΩ (Low Side)
- **High Efficiency, less than 10 µA at shutdown**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **700-kHz Switching Frequency (f_{SW})**
- **Cycle By Cycle Over Current Limit**
- **Power Good Output**

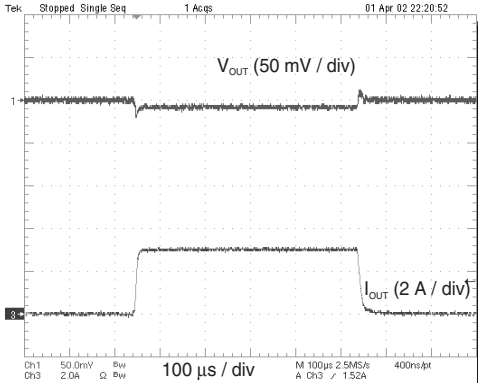
APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
  - **Digital TV Power Supply**
  - **High Definition Blue-ray Disc™ Players**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**

DESCRIPTION

The TPS54325-Q1 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54325-Q1 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54325-Q1 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS54325-Q1 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VCC input , and from 2.0-V to 18-V VIN input power supply voltage. The output voltage can be programmed between 0.76 V and 5.5 V. The device also features an adjustable slow start time and a power good function. The TPS54325-Q1 is available in the 14 pin HTSSOP package, and designed to operate from –40°C to 105°C.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SWIFT, D-CAP2, PowerPAD are trademarks of Texas Instruments.
Blue-ray Disc is a trademark of Blu-ray Disc.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	PowerPAD™ (HTSSOP) – PWP	Reel of 2000	TPS54325TPWPRQ1	54325Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_I	Input voltage range	V_{IN}, V_{CC}, EN	–0.3 to 20	V
		V_{BST}	–0.3 to 26	V
		V_{BST} (vs SW1, SW2)	–0.3 to 6.5	V
		V_{FB}, V_O, SS, PG	–0.3 to 6.5	V
		SW1, SW2	–2 to 20	V
		SW1, SW2 (10 ns transient)	–3 to 20	V
V_O	Output voltage range	V_{REG5}	–0.3 to 6.5	V
		P_{GND1}, P_{GND2}	–0.3 to 0.3	V
V_{diff}	Voltage from GND to POWERPAD		–0.2 to 0.2	V
ESD rating	Electrostatic discharge	Human Body Model (HBM)	2	kV
		Charged Device Model (CDM)	1000	V
T_J	Operating junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54325-Q1 PWP 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	46.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.7	
θ_{JB}	Junction-to-board thermal resistance	31.1	
ψ_{JT}	Junction-to-top characterization parameter	36.6	
ψ_{JB}	Junction-to-board characterization parameter	7.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	31.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, VCC, VIN = 12V (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply input voltage range		4.5	18	V
V_{IN}	Power input voltage range		2	18	V
V_I	Input voltage range	V_{BST}	–0.1	24	V
		V_{BST} (vs SW1, SW2)	–0.1	6	
		SS, PG	–0.1	6	
		EN	–0.1	18	
		V_O, V_{FB}	–0.1	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10 ns transient)	–3	18	
		P_{GND1}, P_{GND2}	–0.1	0.1	
V_O	Output voltage range	V_{REG5}	–0.1	6	V
I_O	Output Current range	I_{VREG5}	0	10	mA
T_A	Operating free-air temperature		–40	105	°C
T_J	Operating junction temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating - non-switching supply current	V_{CC} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		850	1300	µA
I_{VCCSDN}	Shutdown supply current	V_{CC} current, T_A = 25°C, EN = 0 V			10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	2			V
V_{ENL}	EN low-level input voltage	EN			0.4	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V	757	765	775	mV
		T_A = 0°C to 105°C, V_O = 1.05 V(1)	753		777	
		T_A = -40°C to 105°C, V_O = 1.05 V(1)	750		780	
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
R_{Dischg}	V_O discharge resistance	EN = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6.0 V < V_{CC} < 18 V, 0 < I_{VREG5} < 5 mA	5.3	5.5	5.7	V
V_{LN5}	Line regulation	6.0 V < V_{CC} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{LD5}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	Output current	V_{CC} = 6 V, V_{REG5} = 4.0 V, T_A = 25°C		70		mA
MOSFET						
R_{dsonh}	High side switch resistance	25°C, V_{BST} - SW1, SW2 = 5.5 V		120		mΩ
R_{dsonl}	Low side switch resistance	25°C		70		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	T_A = 25°C to 105°C	3.5	4.1		A
		T_A = -40°C	3.25	3.5		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (1)		150		°C
		Hysteresis (1)		25		

(1) Not production tested.

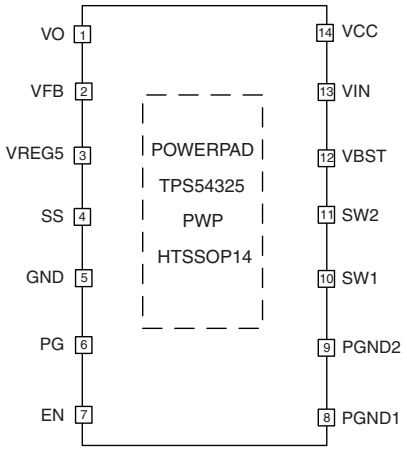
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
T_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		145		ns
$T_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260		ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 0 V	1.4	2.0	2.6	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (good)	85	90	95	%
		V_{FB} falling (fault)		85		
I_{PG}	PG sink current	PG = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	115	120	125	%
T_{OVPDEL}	Output OVP prop delay			5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65	70	75	%
		Hysteresis		10		
T_{UVPDEL}	Output UVP delay			0.25		ms
T_{UVPEN}	Output UVP enable delay	Relative to soft-start time		x 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake up V_{REG5} voltage	3.45	3.70	3.95	V
		Hysteresis V_{REG5} voltage	0.15	0.25	0.35	

DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)



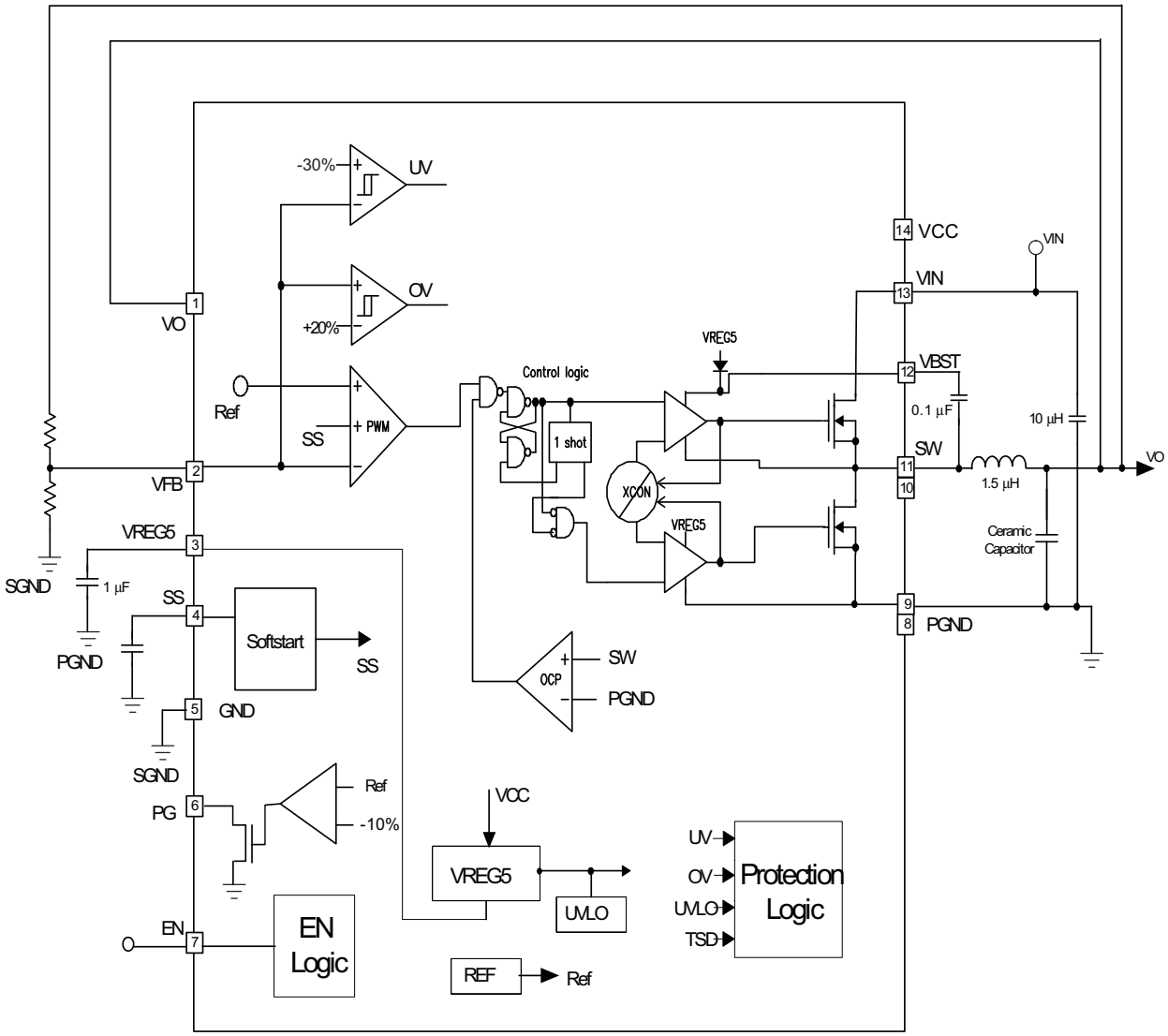
TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
VO	1	Connect to output of converter. This terminal is used for On-Time Adjustment.
VFB	2	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1µF) should be connected to GND.
SS	4	Soft-start control. A external capacitor should be connected to GND.
GND	5	Signal ground pin

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
PG	6	Open drain power good output
EN	7	Enable control input
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN	13	Power input and connected to high side NFET drain
VCC	14	Supply input for 5 V internal linear regulator for the control circuitry
PowerPAD™	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

FUNCTIONAL BLOCK DIAGRAM



OVERVIEW

The TPS54325-Q1 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54325-Q1 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot timer is set by the converter input voltage ,VIN, and the output voltage ,VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54325-Q1 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54325-Q1 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

Soft Start and Pre-Biased Soft Start

The TPS54325-Q1 has an adjustable soft start . When the EN pin becomes high, 2.0-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 2 µA.

$$Tss(ms) = \frac{C6(nF) \bullet Vref}{Iss(\mu A)} = \frac{C6(nF) \bullet 0.765}{2} \quad (1)$$

The TPS54325-Q1 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage (V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Power Good

The TPS54325-Q1 has power-good output. The power-good function is activated after soft start has finished. If the output voltage becomes within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. During start up, power good start after 1.7 times soft-start time to avoid a glitch of power-good signal. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after 10 µs internal delay.

Output Discharge Control

The TPS54325-Q1 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The device discharges outputs using an internal 50-Ω MOSFET which is connected to VO and PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

Current Protection

The TPS54325-Q1 has cycle-by-cycle over current limiting control. The inductor current is monitored during the OFF state and the controller keeps the OFF state when the inductor current is larger than the over current trip level. In order to provide both good accuracy and cost effective solution, the device supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

The inductor current is monitored by the voltage between PGND pin and SW1/SW2 pin. In an over current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown.

Over/Under Voltage Protection

The TPS54325-Q1 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 µs, the device latches off both internal top and bottom MOSFET. This function is enabled approximately 1.7 x soft-start time.

UVLO Protection

The TPS54325-Q1 has under voltage lock out protection (UVLO) that monitors the voltage of V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54325-Q1 is shut off. This is non-latch protection.

Thermal Shutdown

The TPS54325-Q1 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the device is shut off. This is non-latch protection.

TYPICAL CHARACTERISTICS

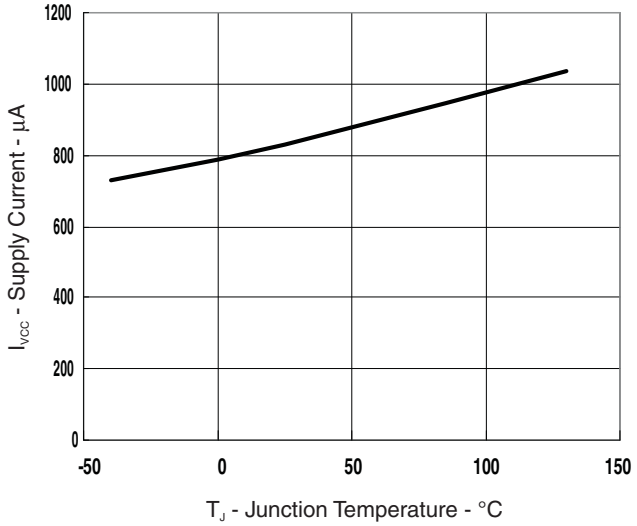


Figure 1. V_{CC} TEMPERATURE vs. JUNCTION TEMPERATURE

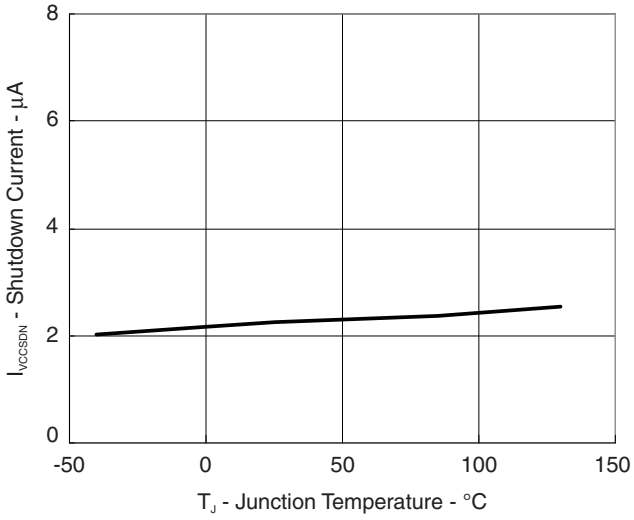


Figure 2. V_{CC} SHUTDOWN CURRENT vs. JUNCTION TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

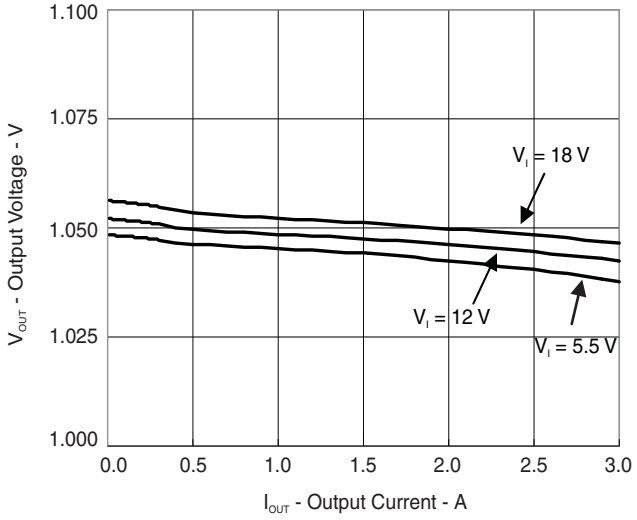


Figure 3. 1.05-V OUTPUT VOLTAGE vs. OUTPUT CURRENT

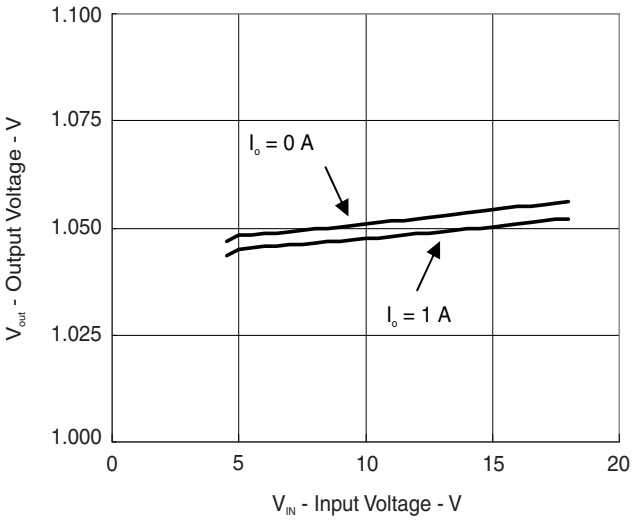


Figure 4. 1.05-V OUTPUT VOLTAGE vs. INPUT VOLTAGE

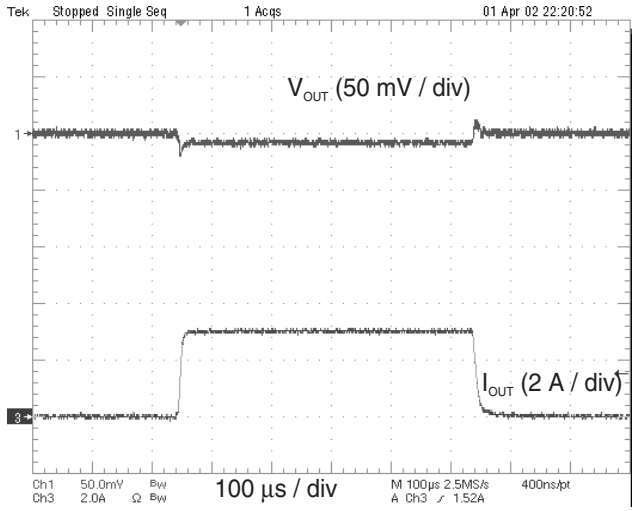


Figure 5. 1.05-V, 0-A TO 3-A LOAD TRANSIERESPONSE

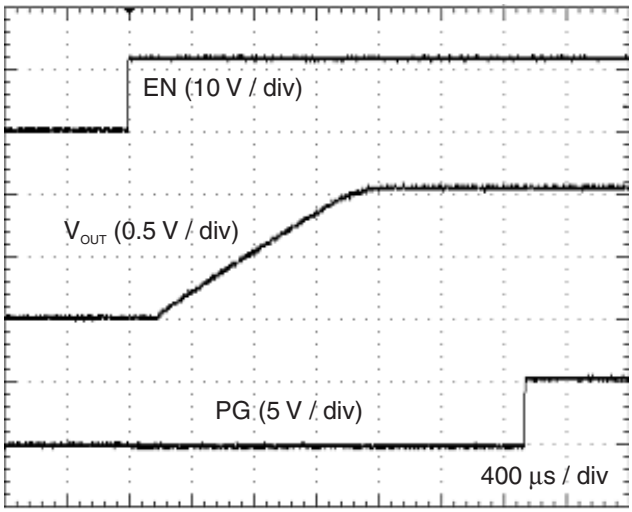


Figure 6. START-UP WAVE FORM

TYPICAL CHARACTERISTICS (continued)

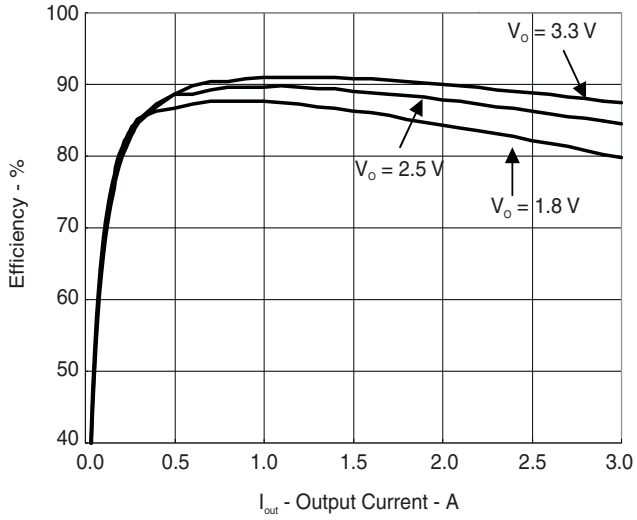


Figure 7. EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 12 V)

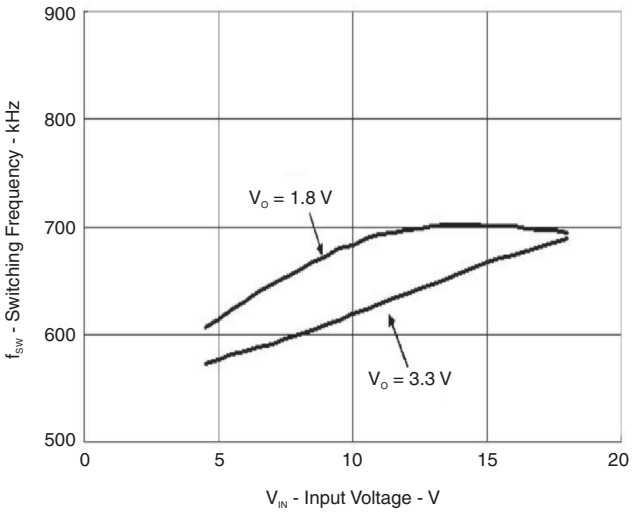


Figure 8. SWITCHING FREQUENCY vs. INPUT VOLTAGE (I_O=1 A)

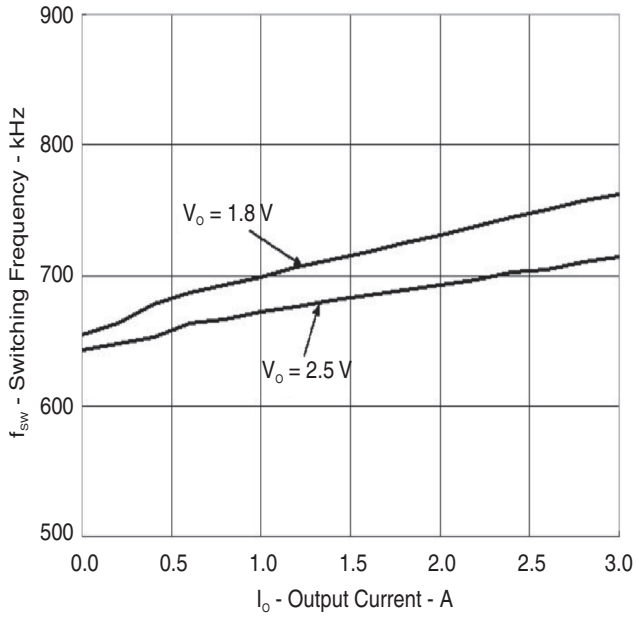


Figure 9. SWICHING FREQUENCY vs. OUTPUT CURRENT

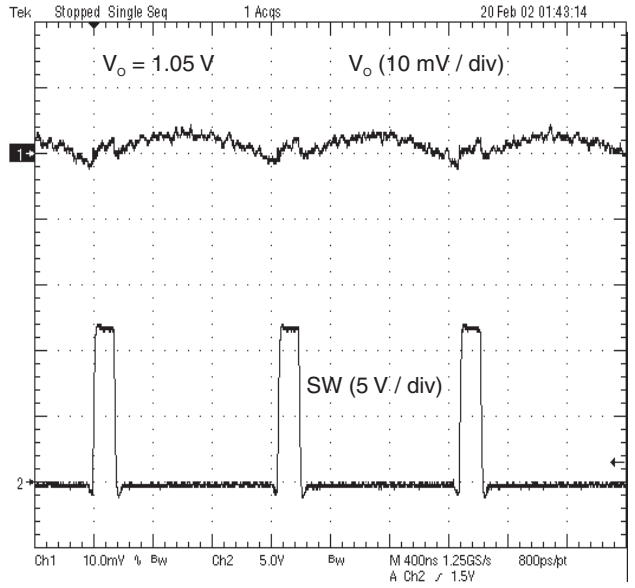


Figure 10. VOLTAGE RIPPLE AT OUTPUT

TYPICAL CHARACTERISTICS (continued)

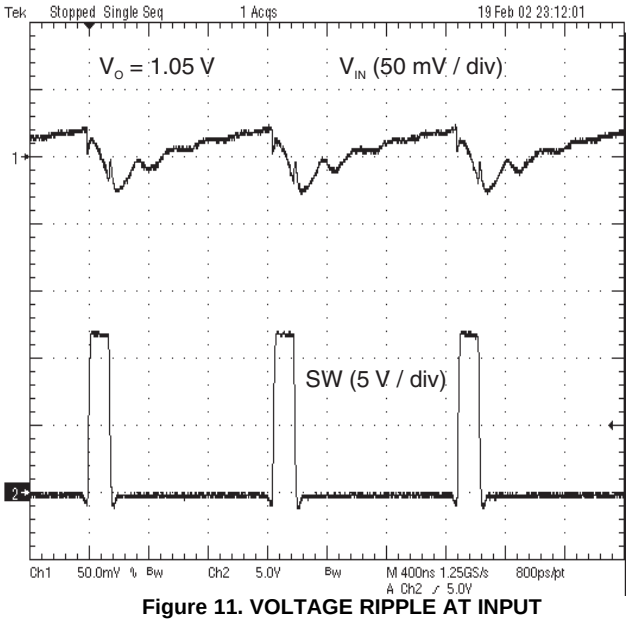


Figure 11. VOLTAGE RIPPLE AT INPUT

DESIGN GUIDE

Step By Step Design Procedure

To begin the design process, you must define these parameters for your application as follows:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

Output Inductor Selection

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improves S/N ratio and contributes to stable operation. Smaller ripple currents result in lower output voltage ripple. When using low ESR output capacitors output ripple voltage is usually low, so larger ripple currents are acceptable. The coefficient Kind represents the percentage of ripple current. The value of Kind must not be greater than 0.4. Use 0.3 when using low ESR output capacitors. Equation 2 can be used to calculate L1. Use 700 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 4 and the RMS current of Equation 5.

$$L_O = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{I_{OUT} \bullet f_{SW} \bullet Kind} \tag{2}$$

$$Ilp\text{-}p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \tag{3}$$

$$I_{lpeak} = I_O + \frac{Ilp\text{-}p}{2} \tag{4}$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Ilp\text{-}p^2} \tag{5}$$

Output Capacitor Selection

The capacitor value and ESR determines the amount of output voltage ripple. Recommended to use ceramic output capacitor. Using Equation 6 to Equation 8, an initial estimate for the capacitor value, ESR, and RMS current can be calculated. If the load transients are significant consider using the load step, instead of ripple current to calculate the maximum ESR. Minimum C_O should be over 20 µF.

$$C_O > \frac{1}{8 \bullet f_{SW}} \bullet \frac{1}{\left(\frac{V_{O(ripple)}}{I_{(ripple)}} - R_{ESR}\right)} \tag{6}$$

$$R_{ESR} < \frac{V_{O(ripple)}}{I_{l(ripple)}} \tag{7}$$

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \tag{8}$$

Input Capacitor Selection

The TPS54325-Q1 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage. In case of separate V_{CC} and V_{IN}, then a ceramic capacitor over 10 µF is recommended for the V_{IN} and also placing ceramic capacitor over 0.1 µF for the V_{CC} is recommended.

Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 9 and Equation 10 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \bullet \left(1 + \frac{R1}{R2}\right) \quad (9)$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \bullet V_{OUT}) \bullet \left(1 + \frac{R1}{R2}\right) \quad (10)$$

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be connected to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Breif, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

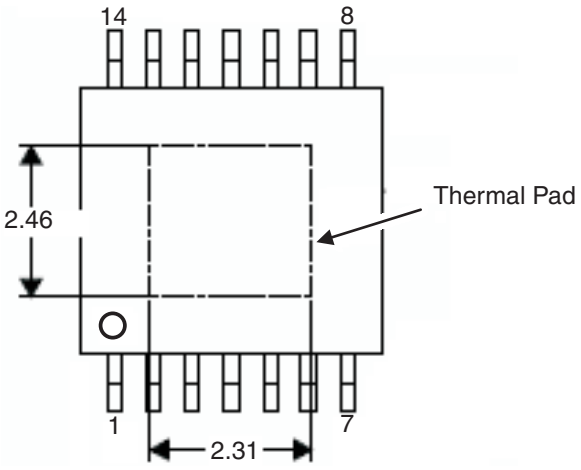


Figure 12. Thermal Pad Dimensions

LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. If VIN and VCC is shorted, VIN and VCC patterns need to be connected with broad pattern lines.
15. VIN Capacitor should be placed as near as possible to the device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS54325TPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	54325Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

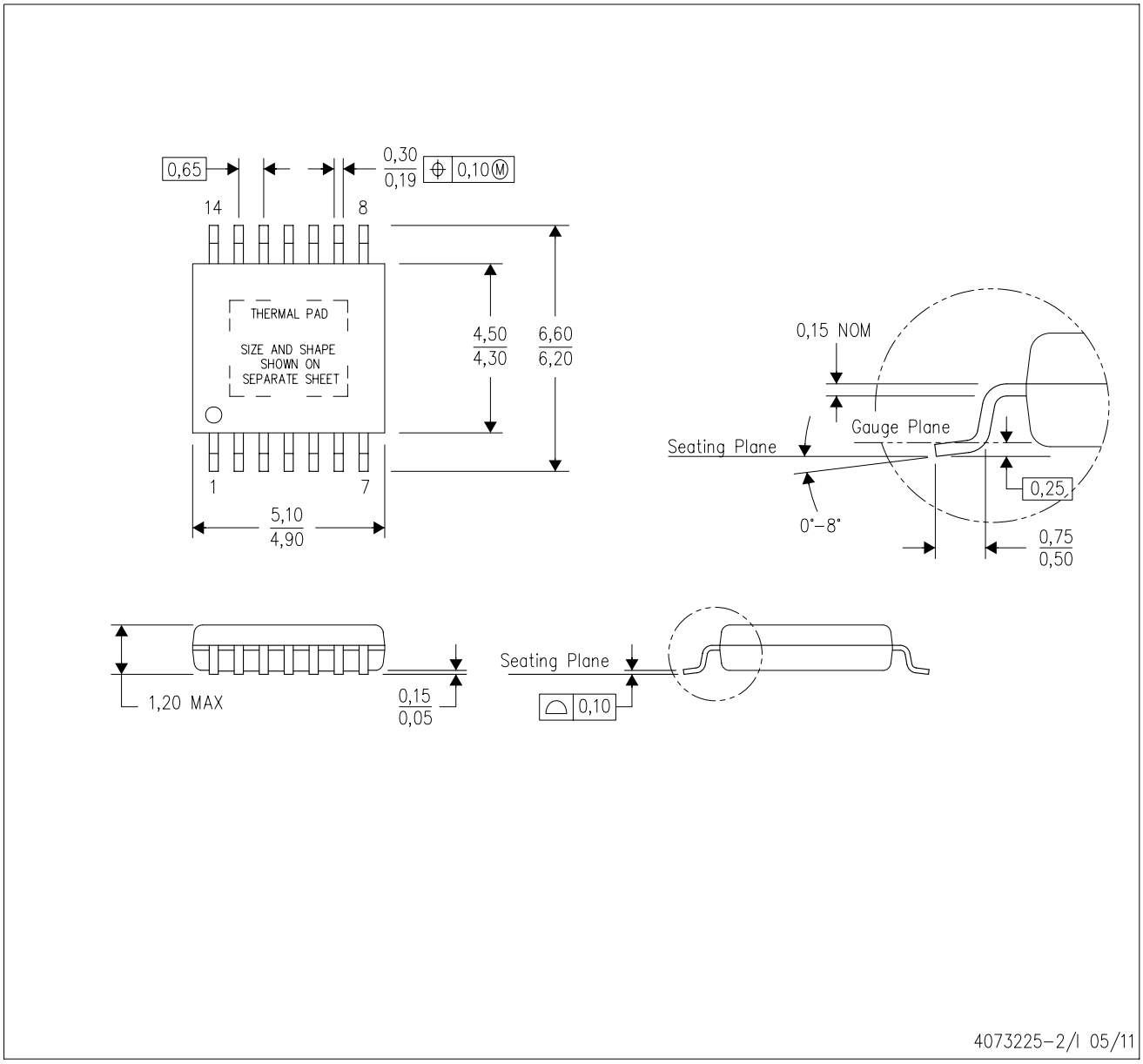
OTHER QUALIFIED VERSIONS OF TPS54325-Q1 :

- Catalog: TPS54325

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

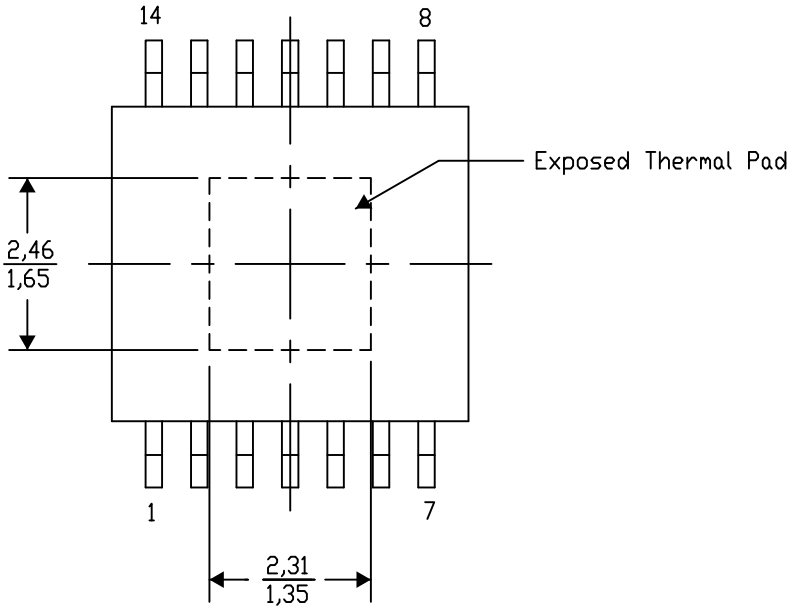
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–2/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

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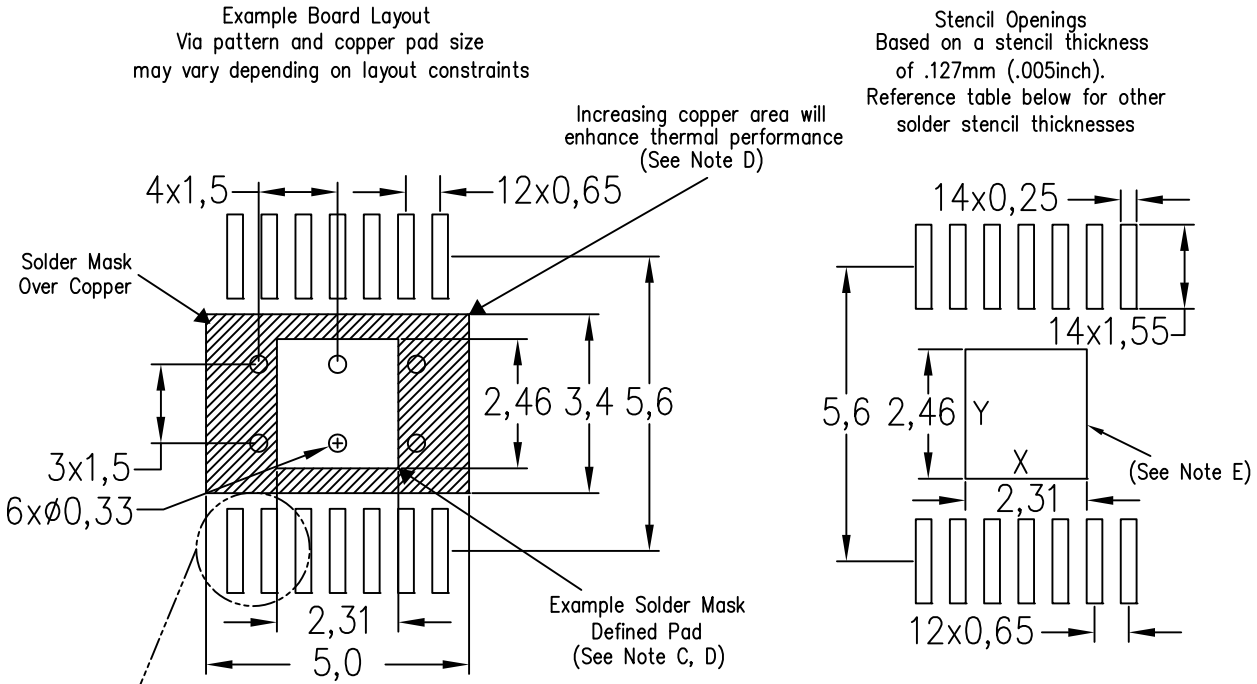
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/U 10/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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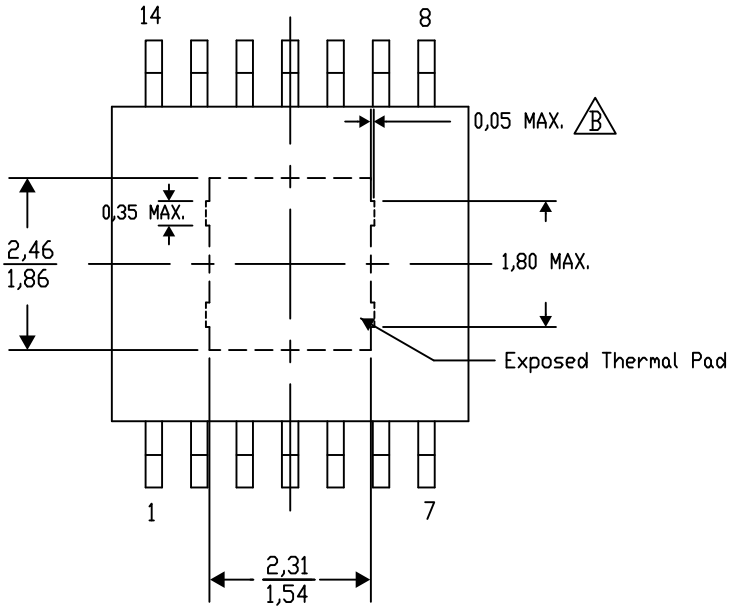
The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–44/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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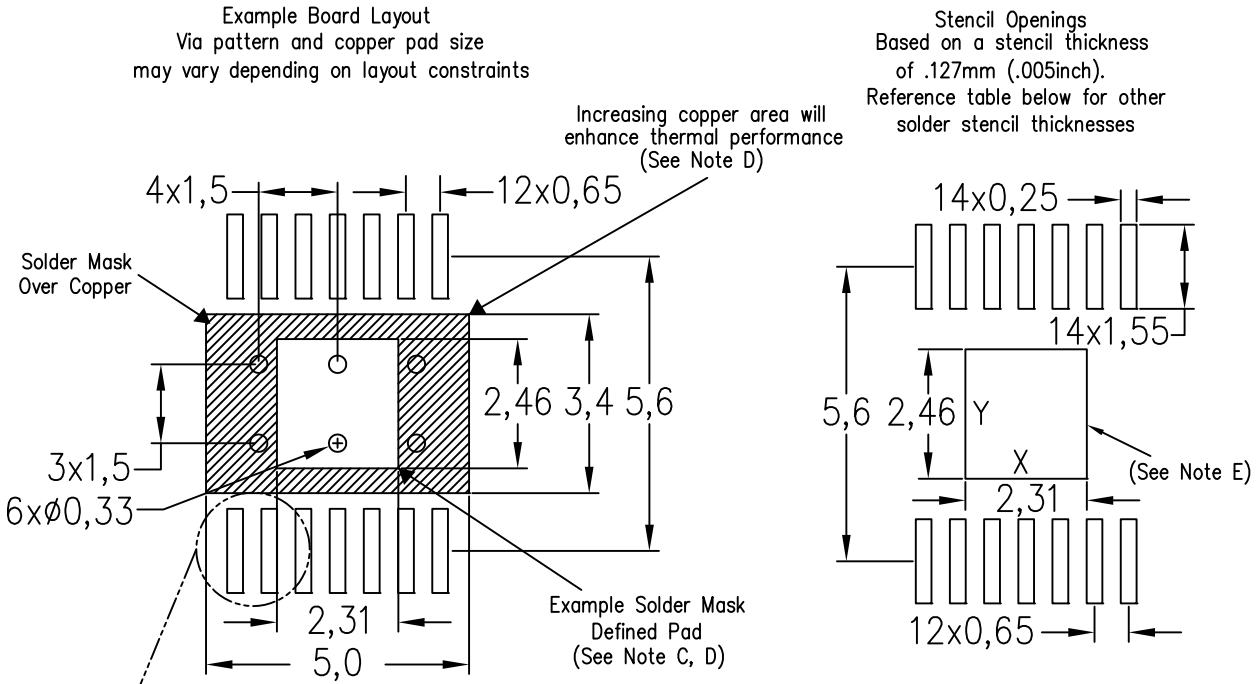
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/U 10/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
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F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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