54AC373,54ACT373

54AC373 54ACT373 Octal Transparent Latch with TRI-STATE Outputs

Literature Number: SNOS138

National Semiconductor

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54AC373 • 54ACT373
Octal Transparent Latch with TRI-STATE® Outputs

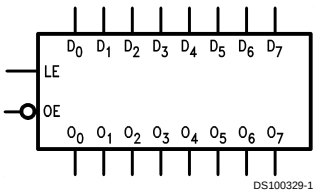
General Description

The 'AC/'ACT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Features

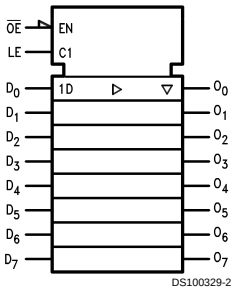
- I_{CC} and I_{OZ} reduced by 50%
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT373 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  — 'AC373: 5962-87555
  — 'ACT373: 5962-87556

Logic Symbols



DS100329-1

IEEE/IEC



DS100329-2

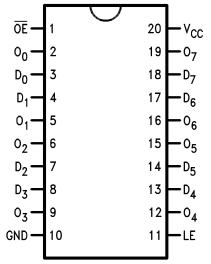
Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

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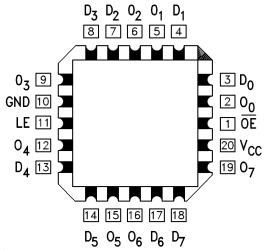
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100329-3

Pin Assignment for LCC



DS100329-4

Functional Description

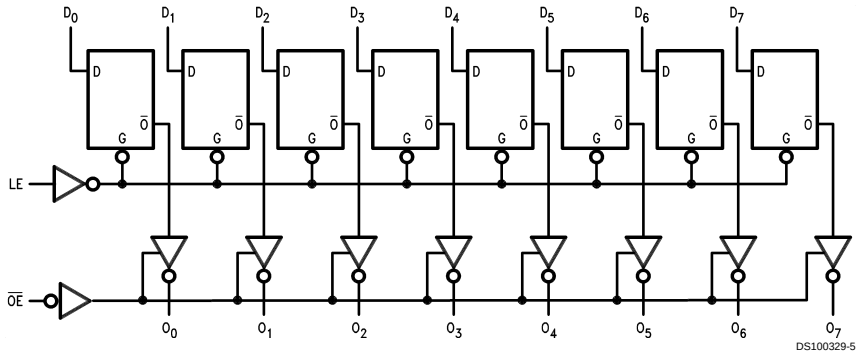
The 'AC/'ACT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{\mathbf{OE}}$	$\mathbf{D_n}$	$\mathbf{O_n}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



DS100329-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 µA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} −12 mA
		4.5	3.7		I_{OH} −24 mA
		5.5	4.7		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 µA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OL} 12 mA
		4.5	0.50		I_{OL} 24 mA
		5.5	0.50		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND

DC Characteristics for ’AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded, thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25˚C is identical to 74AC @ 25˚C.

DC Characteristics for ’ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
					(Note 5) V_{IN} = V_{IL} or V_{IH}
		4.5 5.5	3.70 4.70	V	I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
					(Note 5) V_{IN} = V_{IL} or V_{IH}
		4.5 5.5	0.50 0.50	V	I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{OLD}	(Note 6) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25˚C is identical to 74ACT @ 25˚C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units
			Min	Max	
t_{PLH}	Propagation Delay	3.3	1.0	16.5	ns
	D_n to O_n	5.0	1.5	11.5	
t_{PHL}	Propagation Delay	3.3	1.0	16.0	ns
	D_n to O_n	5.0	1.5	11.5	
t_{PLH}	Propagation Delay	3.3	1.0	16.5	ns
	LE to O_n	5.0	1.5	12.0	
t_{PHL}	Propagation Delay	3.3	1.0	15.0	ns
	LE to O_n	5.0	1.5	11.0	
t_{PZH}	Output Enable Time	3.3	1.0	14.0	ns
		5.0	1.5	10.5	
t_{PZL}	Output Enable Time	3.3	1.0	13.5	ns
		5.0	1.5	10.0	
t_{PHZ}	Output Disable Time	3.3	1.0	16.0	ns
		5.0	1.5	13.5	
t_{PLZ}	Output Disable Time	3.3	1.0	13.0	ns
		5.0	1.5	10.5	

Note 8: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	3.3	6.5	ns	
	D_n to LE	5.0	5.0		
t_h	Hold Time, HIGH or LOW	3.3	1.0	ns	
	D_n to LE	5.0	1.0		
t_w	LE Pulse Width,	3.3	6.5	ns	
	HIGH	5.0	5.0		

Note 9: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 10)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units
			Min	Max	
t_{PLH}	Propagation Delay D_n to O_n	5.0	1.5	12.5	ns
t_{PHL}	Propagation Delay D_n to O_n	5.0	1.5	12.5	ns
t_{PLH}	Propagation Delay LE to O_n	5.0	1.5	12.5	ns
t_{PHL}	Propagation Delay LE to O_n	5.0	1.5	11.5	ns
t_{PZH}	Output Enable Time	5.0	1.5	11.5	ns
t_{PZL}	Output Enable Time	5.0	1.5	11.0	ns
t_{PHZ}	Output Disable Time	5.0	1.5	14.0	ns
t_{PLZ}	Output Disable Time	5.0	1.5	11.0	ns

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

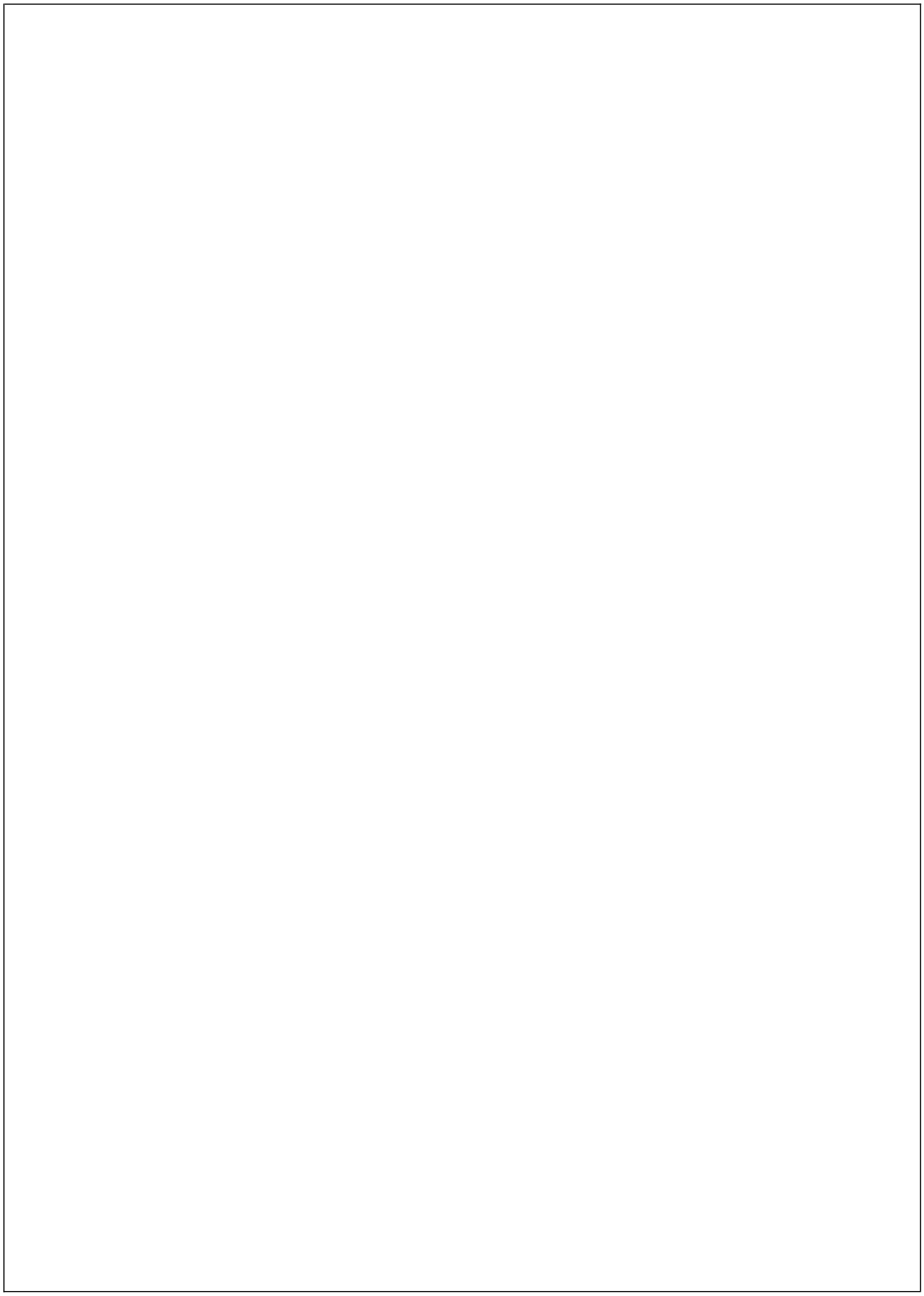
AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 11)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units
			Guaranteed Minimum	
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	8.5	ns
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	1.0	ns
t_w	LE Pulse Width, HIGH	5.0	8.5	ns

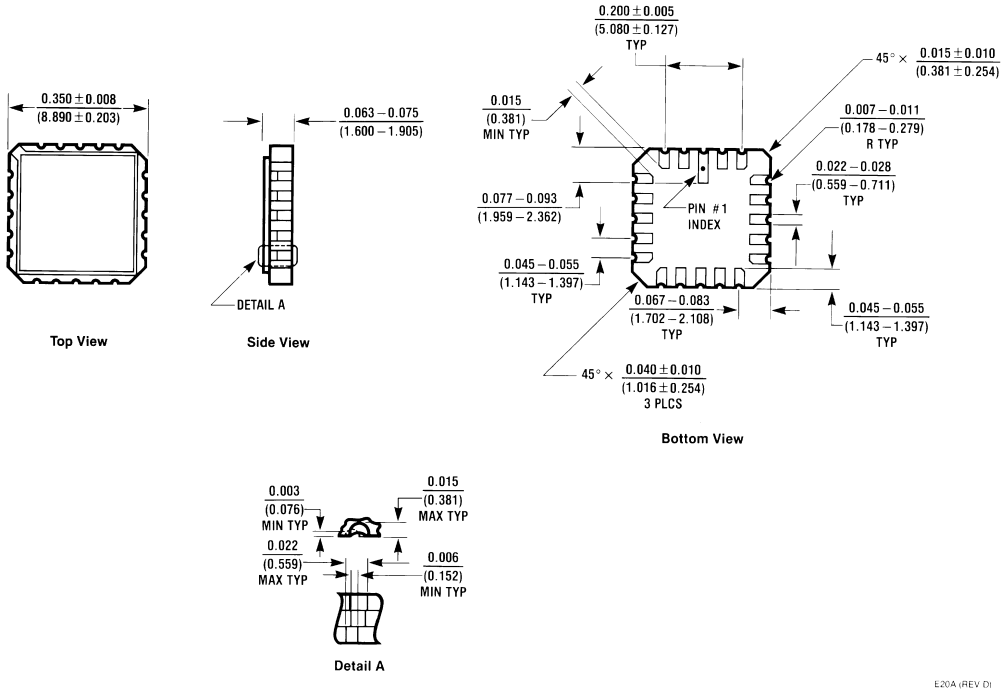
Note 11: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

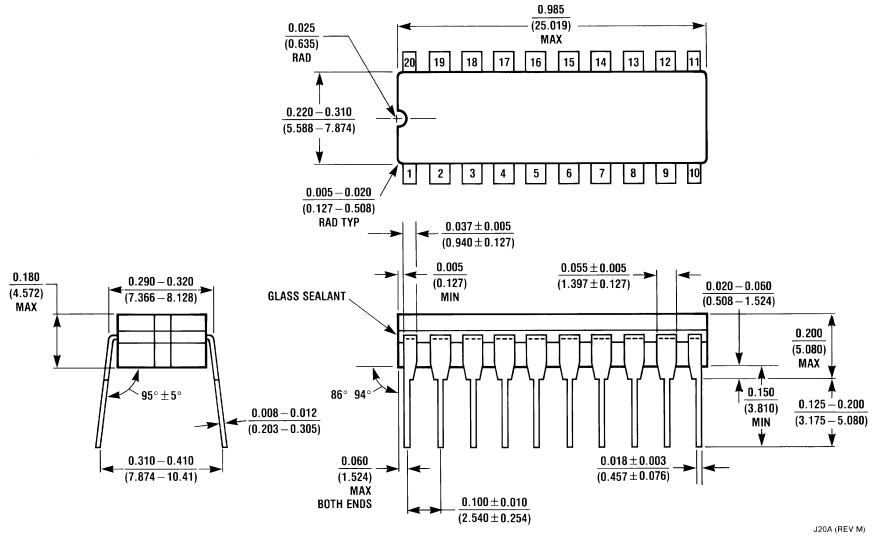
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V



Physical Dimensions inches (millimeters) unless otherwise noted

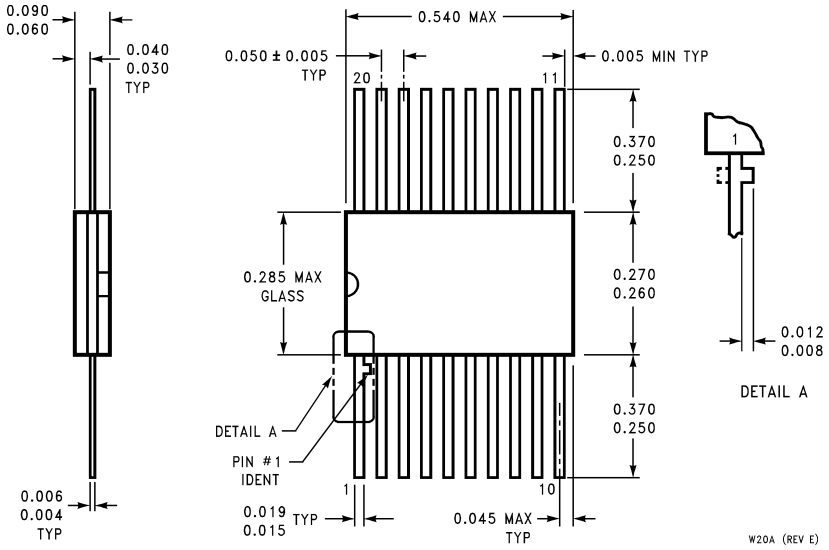


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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