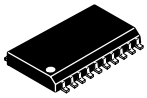
# MC100LVEL38

# 3.3V ECL ÷2, ÷4/6 Clock Generation Chip



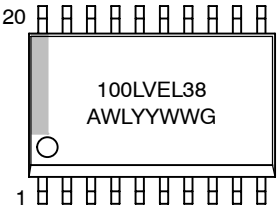
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**SO−20 WB**
**DW SUFFIX**
**CASE 751D**

**MARKING DIAGRAM***




| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*For additional marking information, refer to Application Note AND8002/D.

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

### Description

The MC100LVEL38 is a low skew ÷2, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the ÷2 and the ÷4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2 and the ÷4/6 outputs of a single device.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

### Features

- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: >2 kV Human Body Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:
  $V_{CC}$ = 3.0 V to 3.8 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  $V_{CC}$ = 0 V with $V_{EE}$ = −3.0 V to −3.8 V
- Internal Input 75 kΩ Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 388 devices
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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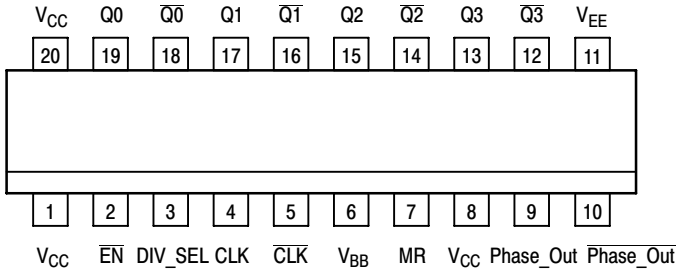



**Figure 1. Pinout: 20-Lead SOIC** (Top View)

Warning: All $V_{CC}$ and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

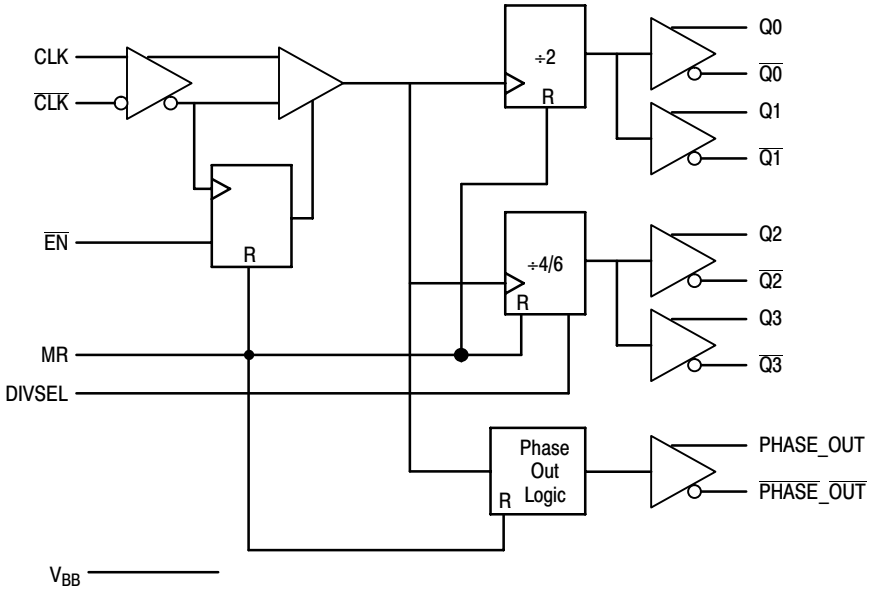



**Figure 2. Logic Diagram**

**Table 1. PIN DESCRIPTION**

| Pin | Function |
|---|---|
| CLK, $\overline{CLK}$ | ECL Diff Clock Inputs |
| $Q_0$, $Q_1$; $\overline{Q_0}$, $\overline{Q_1}$ | ECL Diff ÷2 Outputs |
| $Q_2$, $Q_3$; $\overline{Q_2}$, $\overline{Q_3}$ | ECL Diff ÷4/6 Outputs |
| $\overline{EN}$ | ECL Sync Enable Input |
| MR | ECL Master Reset Input |
| DIVSEL | ECL Frequency Select Input |
| Phase_Out, $\overline{Phase_Out}$ | ECL Phase Sync Diff. Signal Output |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |

**Table 2. FUNCTION TABLE**

| CLK | $\overline{EN}$ | MR | Function |
|---|---|---|---|
| Z | L | L | Divide |
| ZZ | H | L | Hold $Q_{0-3}$ |
| X | X | H | Reset $Q_{0-3}$ |

Z = Low-to-High Transition
ZZ = High-to-Low Transition
X = Don't Care

| DVSEL | $Q_2$, $Q_3$ OUTPUTS |
|---|---|
| L | Divide by 4 |
| H | Divide by 6 |

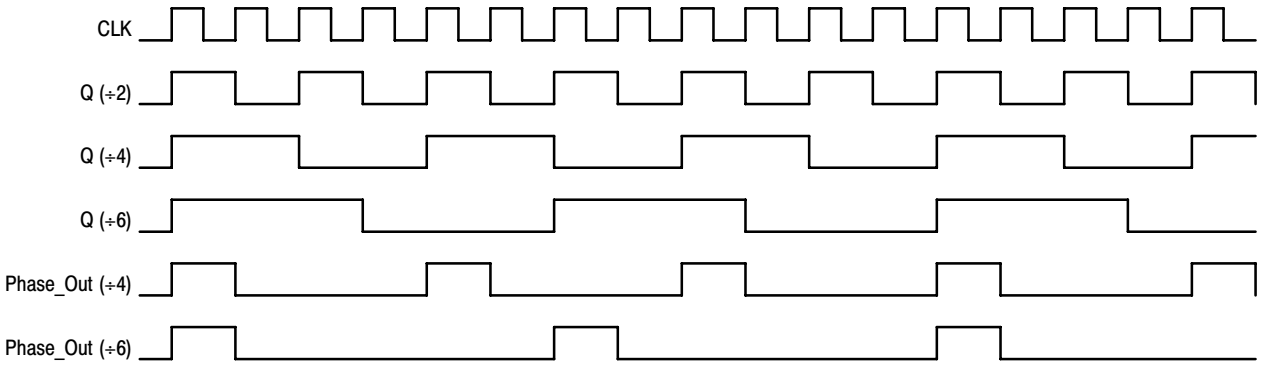



**Figure 3. Timing Diagrams**

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 8 to 0 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −8 to 0 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6 to 0<br>−6 to 0 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | SOIC−20<br>SOIC−20 | 90<br>60 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | SOIC−20 | 30 to 35 | °C/W |
| $T_{sol}$ | Wave Solder Pb<br>Pb−Free | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C | | 265<br>265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. LVPECL DC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0.0 V (Note 1)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{EE}$ | Power Supply Current | | 50 | 60 | | 50 | 60 | | 54 | 65 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| $V_{BB}$ | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 6) | 1.65 | | 2.75 | 1.65 | | 2.75 | 1.65 | | 2.75 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\ Min}$ and 1.0 V.

**Table 5. LVNECL DC CHARACTERISTICS** $V_{CC}$ = 0.0 V; $V_{EE}$ = −3.3 V (Note 4)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{EE}$ | Power Supply Current | | 50 | 60 | | 50 | 60 | | 54 | 65 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 5) | −1085 | −1005 | −880 | −1025 | −955 | −880 | −1025 | −955 | −880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 5) | −1830 | −1695 | −1555 | −1810 | −1705 | −1620 | −1810 | −1705 | −1620 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | −1165 | | −880 | −1165 | | −880 | −1165 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | −1810 | | −1475 | −1810 | | −1475 | −1810 | | −1475 | mV |
| $V_{BB}$ | Output Voltage Reference | −1.38 | | −1.26 | −1.38 | | −1.26 | −1.38 | | −1.26 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 6) | −1.65 | | −0.55 | −1.65 | | −0.55 | −1.65 | | −0.55 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary ±0.3 V.
5. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
6. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\ Min}$ and 1.0 V.

**Table 6. AC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0.0 V or $V_{CC}$ = 0.0 V; $V_{EE}$ = −3.3 V (Note 7)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| fmax | Maximum Toggle Frequency (Divide by 2) | 1.0 | 1.2 | | 1.0 | 1.2 | | 1.0 | 1.2 | | GHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>CLK to Q (Differential)<br>CLK to Q (Single−Ended)<br>CLK to Phase_Out (Differential)<br>CLK to Phase_Out (Single−Ended)<br>MR to.Q | <br>810<br>710<br>800<br>750<br>510 | | <br>1010<br>1010<br>1000<br>1050<br>810 | <br>850<br>750<br>840<br>790<br>540 | | <br>1050<br>1050<br>1040<br>1090<br>840 | <br>900<br>800<br>890<br>840<br>570 | | <br>1100<br>1100<br>1090<br>1140<br>870 | ps |
| $t_{SKEW}$ | Within-Device Skew (Note 8) $Q_0 - Q_3$<br>All | | | <br>50<br>75 | | | <br>50<br>75 | | | <br>50<br>75 | ps |
| | Part-to-Part $Q_0 - Q_3$ (Differential)<br>All | | | 200<br>240 | | | 200<br>240 | | | 200<br>240 | |
| $t_S$ | Setup Time $\overline{EN}$ to $\overline{CLK}$<br>DIVSEL to CLK | 150 | | | 150 | | | 150 | | | ps |
| $t_H$ | Hold Time $\overline{CLK}$ to $\overline{EN}$<br>CLK to Div_Sel | 150<br>200 | | | 150<br>200 | | | 150<br>200 | | | ps |
| $V_{PP}$ | Input Swing (Note 9) CLK | 250 | | 1000 | 250 | | 1000 | 250 | | 1000 | mV |
| $t_{RR}$ | Reset Recovery Time | | | 100 | | | 100 | | | 100 | ps |
| $t_{PW}$ | Minimum Pulse Width CLK<br>MR | 800<br>700 | | | 800<br>700 | | | 800<br>700 | | | ps |
| $t_r$, $t_f$ | Output Rise/Fall Times Q (20% − 80%) | 280 | | 550 | 280 | | 550 | 280 | | 550 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. $V_{EE}$ can vary ±0.3 V.
8. Skew is measured between outputs under identical transitions.
9. $V_{PP}$(min) is minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100 mV.

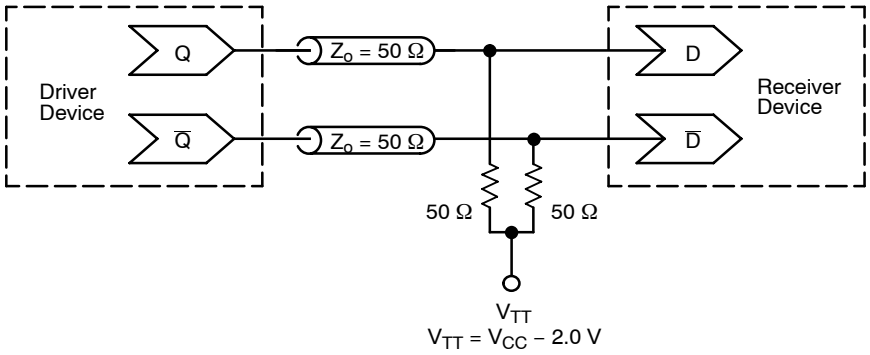



**Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Package† |
|---|---|---|
| MC100LVEL38DW | SOIC−20 | 38 Units / Rail |
| MC100LVEL38DWG | SOIC−20 (Pb−Free) | 38 Units / Rail |
| MC100LVEL38DWR2 | SOIC−20 | 1000 / Tape & Reel |
| MC100LVEL38DWR2G | SOIC−20 (Pb−Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

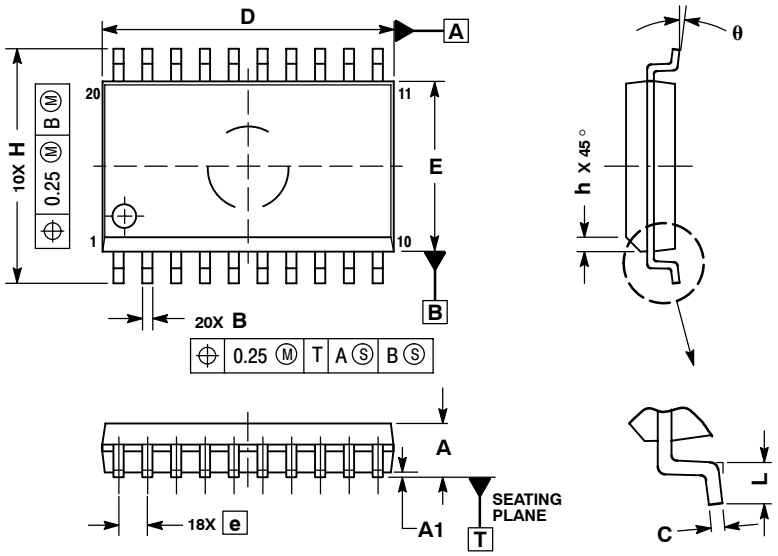
**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

**SO−20 WB**
**DW SUFFIX**
CASE 751D−05
ISSUE G




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

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