

Pulse Width Modulation Amplifier

FEATURES

- WIDE SUPPLY RANGE—16-100V
- 30A CONTINUOUS TO 60°C case
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

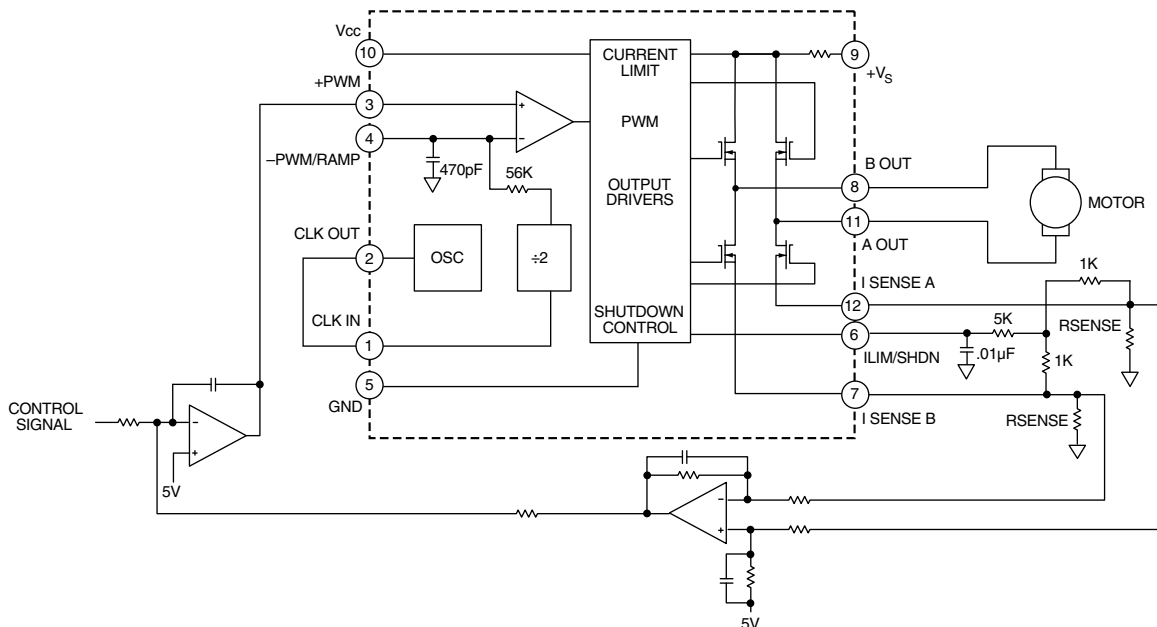
APPLICATIONS

- MOTORS TO 4HP
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

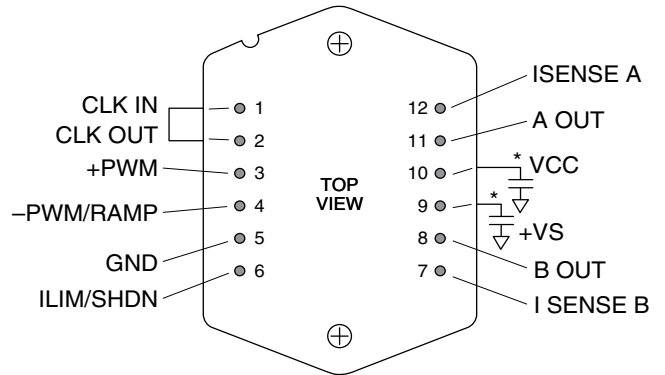
The SA03 is a pulse width amplifier that can supply 3000W to the load. An internal 45kHz oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the basic switching of 22.5 kHz. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

BLOCK DIAGRAM AND TYPICAL APPLICATION



**12-PIN POWER DIP
PACKAGE STYLE CR**

EXTERNAL CONNECTIONS



Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/-PWM then A OUT > B OUT.

* See text.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, +V _S	100V
SUPPLY VOLTAGE, V _{CC}	16V
POWER DISSIPATION, internal	300W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction ²	150°C
TEMPERATURE, storage	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, -PWM	0 to +11V
INPUT VOLTAGE, I _{LIM}	0 to +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS ²	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level ⁴	I _{OUT} ≤ 1mA	4.8		5.3	V
CLK OUT, low level ⁴	I _{OUT} ≤ 1mA	0		.4	V
FREQUENCY		44	45	46	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level ⁴		0		.9	V
CLK IN, high level ⁴		3.7		5.4	V
OUTPUT					
TOTAL R _{ON}				.16	Ω
EFFICIENCY, 10A output	V _S = 100V		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22	22.5	23	kHz
CURRENT, continuous ⁴	60°C case	30			A
CURRENT, peak ⁴		40			A
POWER SUPPLY					
VOLTAGE, V _S	Full temperature range	16 ⁵	60	100	V
VOLTAGE, V _{CC}	Full temperature range	14	15	16	V
CURRENT, V _{CC}	I _{OUT} = 0			80	mA
CURRENT, V _{CC} , shutdown				50	mA
CURRENT, V _S	No Load			50	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL³					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

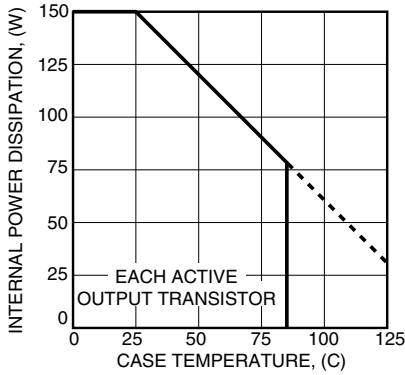
- NOTES: 1. Each of the two active output transistors can dissipate 150W.
 2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical specification.
 3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
 4. Guaranteed but not tested.
 5. If 100% duty cycle is not required V_{S(MIN)} = 0V.

CAUTION

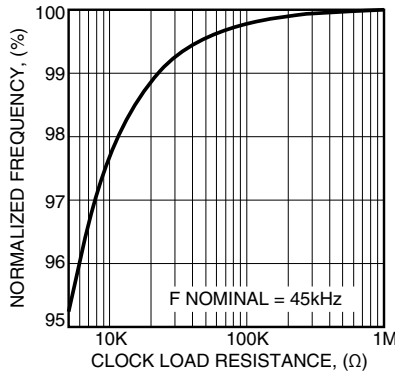
The SA03 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

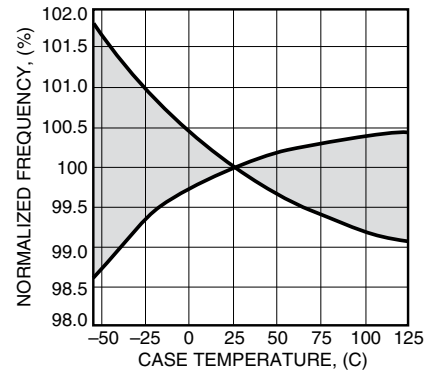
POWER DERATING



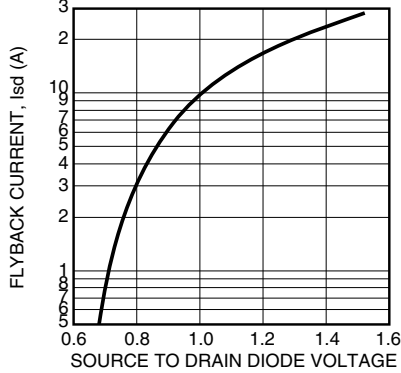
CLOCK LOADING



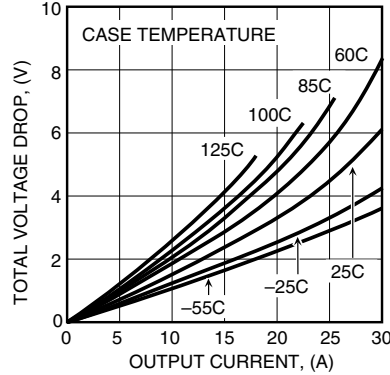
CLOCK FREQUENCY OVER TEMP



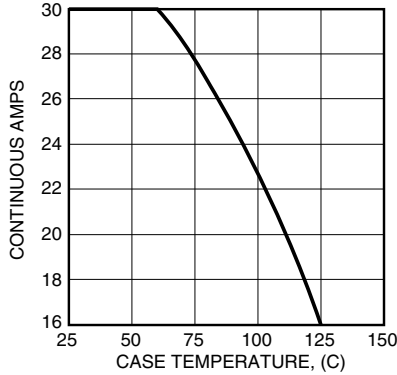
REVERSE DIODE



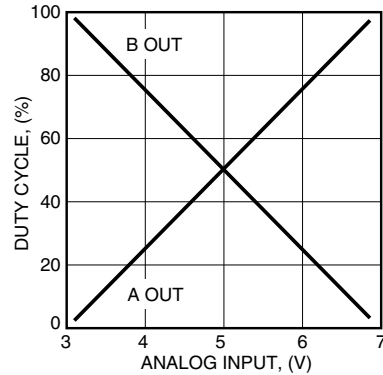
TOTAL VOLTAGE DROP



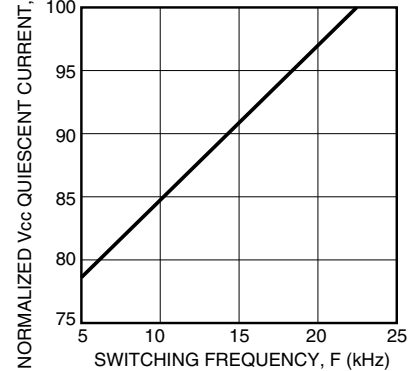
CONTINUOUS OUTPUT



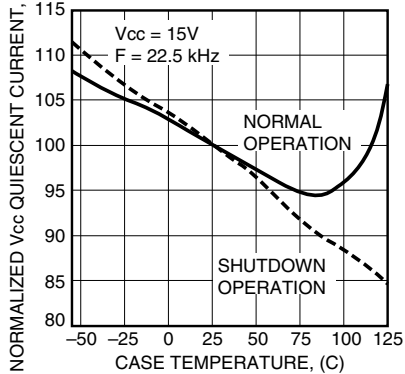
DUTY CYCLE VS ANALOG INPUT



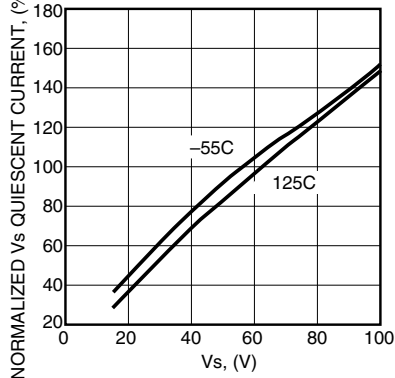
Vcc QUIESCENT CURRENT



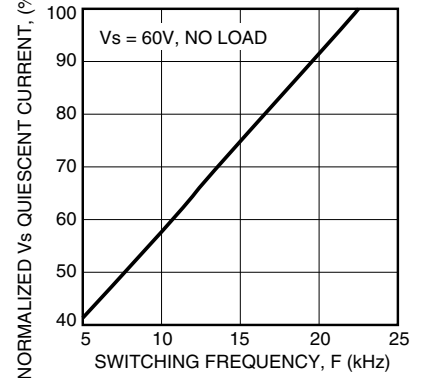
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm filter design; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the -PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the -PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM then A OUT > B OUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

PROTECTION CIRCUITS

In addition to the externally programmable current limit there is also a fixed internal current limit which senses only the high side current. It is nominally set to 140% of the continuous rated output current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. Also, the temperature of the output transistors is continually monitored. Should a fault condition occur which raises the temperature of the output transistors to 165°C the thermal protection circuit will activate and also latch off the output transistors. In either case, it will be necessary to remove the fault condition and recycle power to V_{CC} to restart the circuit.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

Switching noise spikes will invariably be found at the I SENSE pins. The

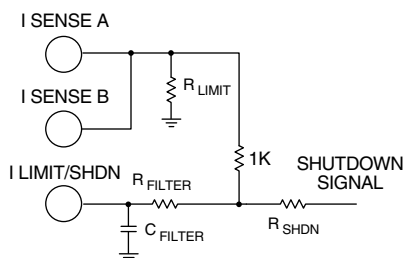


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

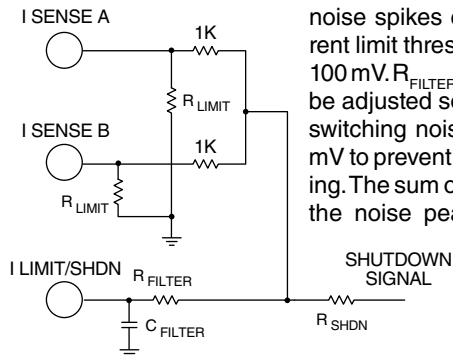


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

noise spikes could trip the current limit threshold which is only 100 mV. R_{LIMIT} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are $C_{FILTER} = .01\mu F$, $R_{FILTER} = 5k$.

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1 V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The V_S supply should be bypassed with at least a 1 μF ceramic capacitor in parallel with another low ESR capacitor of at least 10 μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the V_{CC} supply are less stringent, but still necessary. A .1 μF to .47 μF ceramic capacitor connected directly to the V_{CC} pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA03 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.



CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.

For inquiries via email, please contact apex.support@cirrus.com.

International customers can also request support by contacting their local Cirrus Logic Sales Representative.

To find the one nearest to you, go to www.cirrus.com

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs, Apex Precision Power, Apex and the Apex Precision Power logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.
