

2-Vrms DirectPath™ Line Driver With Programmable-Fixed Gain

Check for Samples: [DRV612](#)

FEATURES

- **DirectPath™**
 - Eliminates Pops/Clicks
 - Eliminates Output DC-Blocking Capacitors
 - 3-V to 3.6-V Supply Voltage
- **Low Noise and THD**
 - SNR > 105 dB at $-1\times$ Gain
 - Typical $V_n < 12\ \mu\text{Vrms}$ 20 Hz–20 kHz at $-1\times$ Gain
 - THD+N < 0.003% at 10-k Ω Load and $-1\times$ Gain
- **2-Vrms Output Voltage Into 600- Ω Load**
- **Single-Ended Input and Output**
- **Programmable Gain Select Reduces Component Count**
 - 13 \times Gain Values
- **Active Mute With More Than 80 dB Attenuation**
- **Short Circuit and Thermal Protection**
- **± 8 -kV HBM ESD-Protected Outputs**

APPLICATIONS

- PDP / LCD TV
- DVD Players
- Mini/Micro Combo Systems
- Soundcards

DESCRIPTION

The DRV612 is a single-ended, 2-Vrms stereo line driver designed to reduce component count, board space and cost. It is ideal for single-supply electronics where size and cost are critical design parameters.

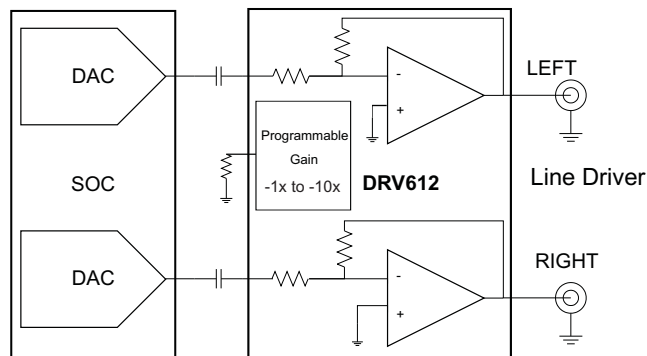
The DRV612 does not require a power supply greater than 3.3 V to generate its 5.6- V_{PP} output, nor does it require a split-rail power supply.

Designed using TI's patented DirectPath technology, which integrates a charge pump to generate a negative supply rail that provides a clean, pop-free ground-biased output. The DRV612 is capable of driving 2 Vrms into a 600- Ω load. DirectPath technology also allows the removal of the costly output dc-blocking capacitors.

The device has fixed-gain single-ended inputs with a gain-select pin. Using a single resistor on this pin, the designer can choose from 13 internal programmable gain settings to match the line driver with the codec output level. It also reduces the component count and board space.

Line outputs have ± 8 kV HBM ESD protection, enabling a simple ESD protection circuit. The DRV612 has built-in active mute control with more than 80 dB attenuation for pop-free mute on/off control.

The DRV612 is available in a 14-pin TSSOP and 16-pin QFN. For a footprint-compatible stereo headphone driver, see TPA6139A2 ([SLOS700](#)).



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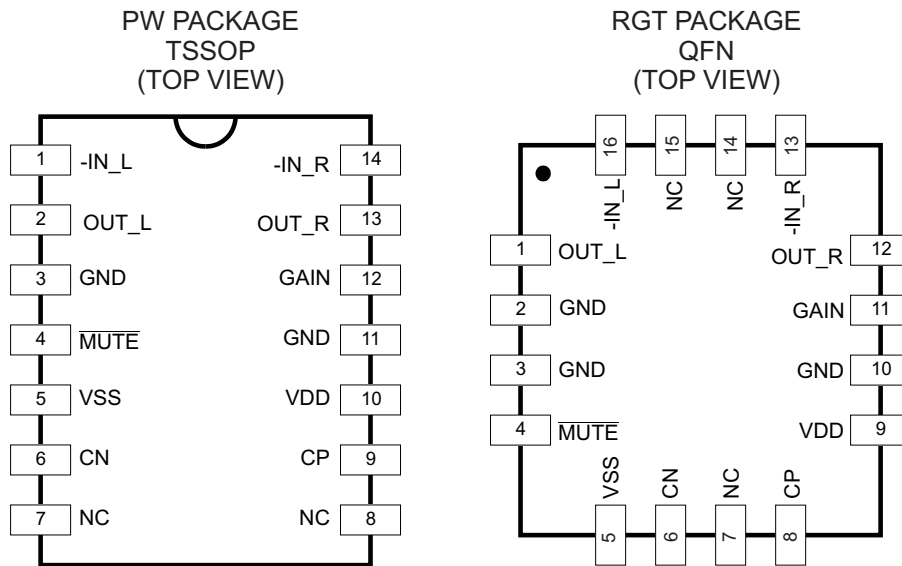
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

GENERAL INFORMATION

TERMINAL ASSIGNMENT

The DRV612 is available in package:

- 14-pin TSSOP package (PW) or 16-pin QFN package (RGT)

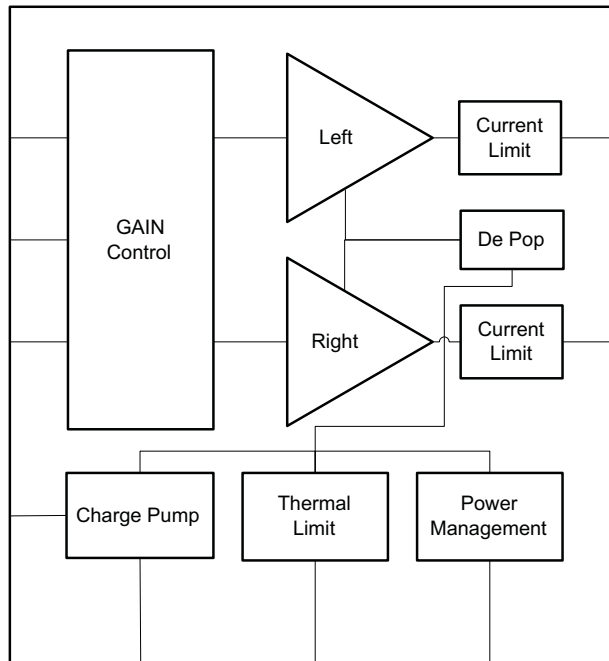


PIN FUNCTIONS

| PIN | | | FUNCTION ⁽¹⁾ | DESCRIPTION |
|-------------|--------|-------------|-------------------------|---|
| NAME | PW NO. | RGT NO. | | |
| -IN_L | 1 | 16 | I | Negative input, left channel |
| OUT_L | 2 | 1 | O | Output, left channel |
| GND | 3, 11 | 2, 3, 10 | P | Ground |
| MUTE | 4 | 4 | I | MUTE, active low |
| VSS | 5 | 5 | O | Change Pump negative supply voltage |
| CN | 6 | 6 | I/O | Charge Pump flying capacitor negative connection |
| NC | 7, 8 | 7, 14, 15 | | No internal connection |
| CP | 9 | 8 | I/O | Charge Pump flying capacitor positive connection |
| VDD | 10 | 9 | P | Supply voltage, connect to positive supply |
| GAIN | 12 | 11 | I | Gain set programming pin; connect a resistor to ground. See Table 1 for recommended resistor values |
| OUT_R | 13 | 12 | O | Output, right channel |
| -IN_R | 14 | 13 | I | Negative input, right channel |
| Thermal Pad | n/a | Thermal Pad | P | Connect to ground |

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE | DESCRIPTION |
|----------------|-----------|--------------|
| –40°C to 85°C | DRV612PW | 14-pin TSSOP |
| | DRV612RGT | 16-pin QFN |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | DRV612 RGT (16-Pin) | DRV612 PW (14-Pin) | UNITS |
|-------------------------------|--|------------------------|-----------------------|-------|
| | | | | |
| θ_{JA} | Junction-to-ambient thermal resistance | 52 | 130 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance | 71 | 49 | |
| θ_{JB} | Junction-to-board thermal resistance | 26 | 63 | |
| Ψ_{JT} | Junction-to-top characterization parameter | 3.0 | 3.6 | |
| Ψ_{JB} | Junction-to-board characterization parameter | 26 | 62 | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/SPRA953).

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | | UNIT |
|---|--|----------------|-----------|------|
| | | MIN | MAX | |
| Voltage range | VDD to GND | −0.3 | 4 | V |
| | V _I , Input voltage | VSS − 0.3 | VDD + 0.3 | |
| | MUTE to GND | −0.3 | VDD + 0.3 | |
| Temperature | Maximum operating junction temperature range, T _J | −40 | 150 | °C |
| | Storage temperature | −65 | 150 | |
| Electrostatic discharge (HBM) QSS 009-105 (JESD22-A114A) | | OUT_L, OUT_R | 8 | kV |
| | | All other pins | 2 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

| | | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------|--------------------------|-----|-----|-----|------|
| VDD | Supply voltage | DC supply voltage | 3.0 | 3.3 | 3.6 | V |
| R _L | | | 600 | 10k | | Ω |
| V _{IL} | Low-level input voltage | $\overline{\text{MUTE}}$ | 38 | 40 | 43 | %VDD |
| V _{IH} | High-level input voltage | $\overline{\text{MUTE}}$ | 57 | 60 | 66 | %VDD |
| T _A | Free-air temperature | | –0 | 25 | 85 | °C |

ELECTRICAL CHARACTERISTICS

VDD = 3.3V, R_{LD} = 5 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|--|-----|-----|-------|------|
| V _{OS} | Output offset voltage | | 0.5 | 1 | mV |
| PSRR | Power-supply rejection ratio | 70 | 80 | | dB |
| V _{OH} | High-level output voltage | 3.1 | | | V |
| V _{OL} | Low-level output voltage | | | –3.05 | V |
| V _{uvp_on} | VDD, undervoltage detection | | | 2.8 | V |
| V _{uvp_hysteresis} | VDD, undervoltage detection, hysteresis | | 200 | | mV |
| F _{CP} | Charge-pump switching frequency | | 350 | | kHz |
| I _{IH} | High-level input current, $\overline{\text{MUTE}}$ | | | 1 | μA |
| I _{IL} | Low-level input current, $\overline{\text{MUTE}}$ | | | 1 | μA |
| I _(VDD) | Supply current, no load | | 18 | | mA |
| | Supply current, MUTED | | 18 | | mA |
| T _{SD} | Thermal shutdown | | 150 | | °C |
| | Thermal shutdown hysteresis | | 15 | | °C |

ELECTRICAL CHARACTERISTICS, LINE DRIVER

VDD = 3.3 V, R_{LOAD} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, 1× gain select (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|-----|--------|-----|------------------|
| V _O | Output voltage, outputs in phase | | 2.2 | | V _{rms} |
| THD+N | Total harmonic distortion plus noise | | 0.007% | | |
| SNR | Signal-to-noise ratio | | 105 | | dB |
| DNR | Dynamic range | | 105 | | dB |
| V _n | Noise voltage | | 12 | | μV |
| Z _O | Output impedance when muted | | 0.07 | 1 | Ω |
| | Input-to-output attenuation when muted | | 80 | | dB |
| | Slew rate | | 4.5 | | V/μs |
| G _{BW} | Unity-gain bandwidth | | 8 | | MHz |
| | Crosstalk – Line L-R and R-L | | –91 | | dB |
| I _{limit} | Current limit | | 25 | | mA |

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PROGRAMMABLE GAIN SETTINGS⁽¹⁾⁽²⁾

VDD = 3.3 V, R_{load} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, 1× gain select, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|---------------------------------|-----|------|-----|------|
| R_Tol | Gain programming resistor tolerance | | | | 2% | |
| ΔA _V | Gain matching | Between left and right channels | | 0.25 | | dB |
| | Gain step tolerance | | | 0.1 | | dB |
| Gain steps | Gain resistor 2% tolerance 249k or higher 82k5 51k1 34k8 27k4 20k5 15k4 11k5 9k09 7k50 6k19 5k11 4k22 | | | –2 | | V/V |
| | | | | –1 | | |
| | | | | –1.5 | | |
| | | | | –2.3 | | |
| | | | | –2.5 | | |
| | | | | –3 | | |
| | | | | –3.5 | | |
| | | | | –4 | | |
| | | | | –5 | | |
| | | | | –5.6 | | |
| | | | | –6.4 | | |
| | | | | –8.3 | | |
| | | | | –10 | | |
| Input impedance | Gain resistor 2% tolerance 249k or higher 82k5 51k1 34k8 27k4 20k5 15k4 11k5 9k09 7k50 6k19 5k11 4k22 | | | 37 | | kΩ |
| | | | | 55 | | |
| | | | | 44 | | |
| | | | | 33 | | |
| | | | | 31 | | |
| | | | | 28 | | |
| | | | | 24 | | |
| | | | | 22 | | |
| | | | | 18 | | |
| | | | | 17 | | |
| | | | | 15 | | |
| | | | | 12 | | |
| | | | | 10 | | |

- (1) If the GAIN pin is left floating, an internal pullup sets the gain to –2×.
(2) Gain setting is latched during power up.

TYPICAL CHARACTERISTICS, LINE DRIVER

$V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2.5\text{ k}\Omega$, $C_{PUMP} = C_{(VSS)} = 1\text{ }\mu\text{F}$, Gain = -2 V/V (unless otherwise noted)

THD+N vs OUTPUT VOLTAGE
3.3 V, 10 k Ω , 1 kHz

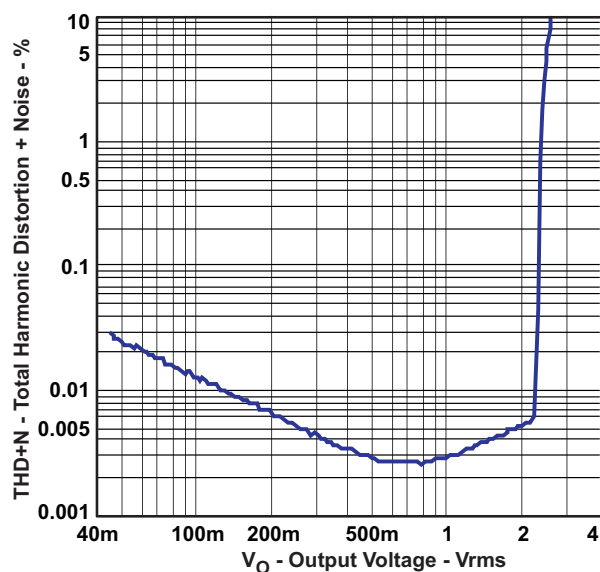


Figure 1.

THD+N vs OUTPUT VOLTAGE
3.3 V, 600 Ω load, 1 kHz

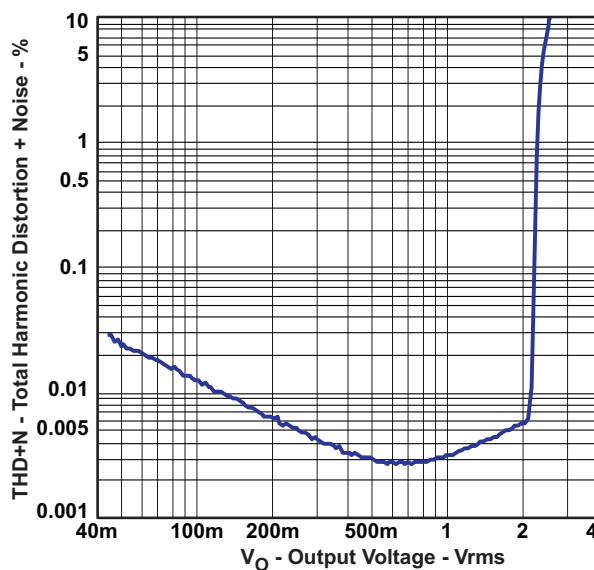
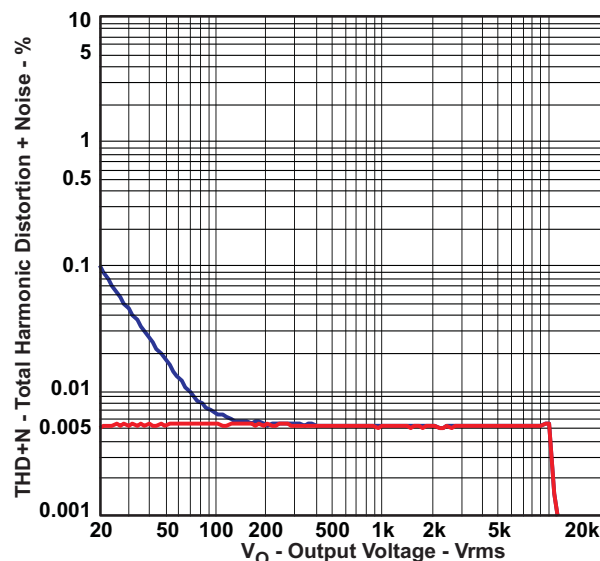


Figure 2.

THD+N vs FREQUENCY
3.3 V, 10 k Ω load, 2 Vrms



Blue: 10- μF ceramic ac-coupling capacitor.
Red: 10- μF electrolytic ac-coupling capacitor

Figure 3.

CHANNEL SEPARATION
3.3 V, 5 k Ω load, 2 Vrms, Blue L to R, Red R to L

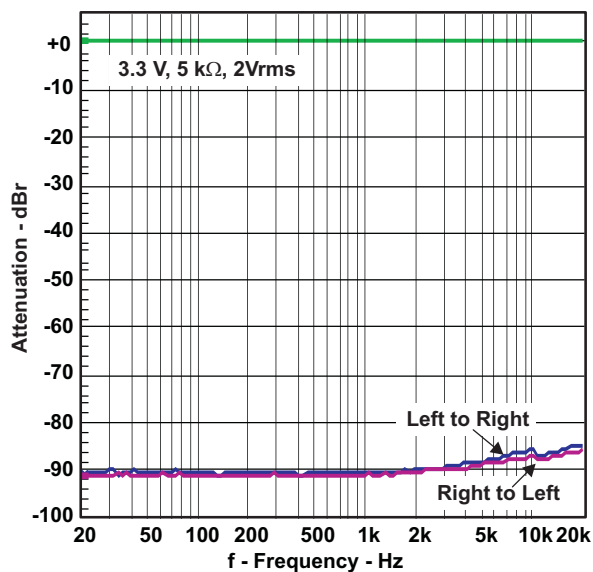


Figure 4.

TYPICAL CHARACTERISTICS, LINE DRIVER (continued)

$V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2.5\text{ k}\Omega$, $C_{PUMP} = C_{VSS} = 1\text{ }\mu\text{F}$, Gain = -2V/V (unless otherwise noted)

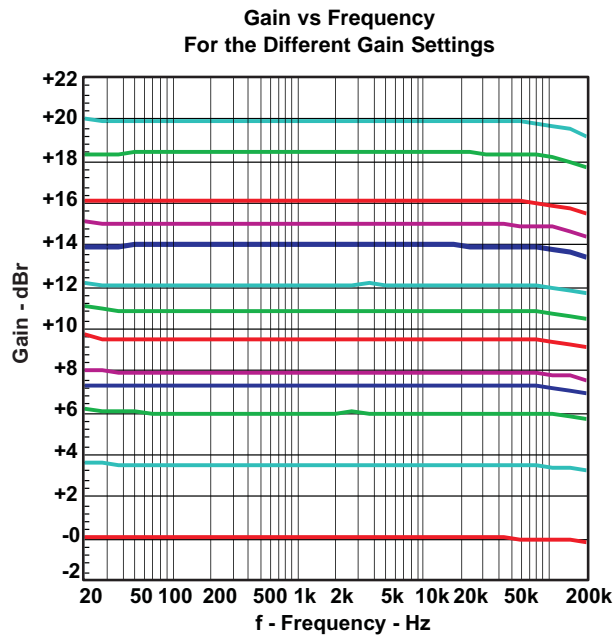


Figure 5.

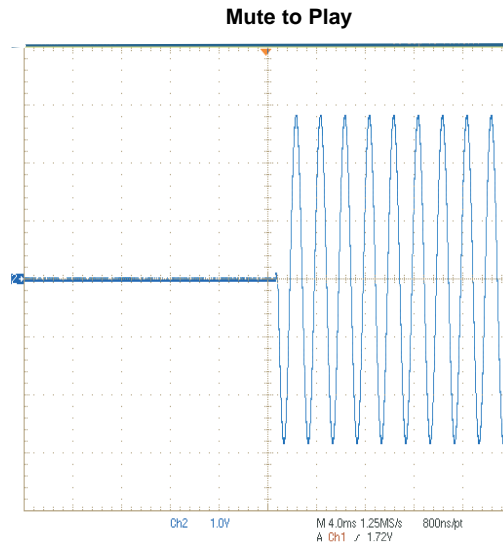


Figure 6.

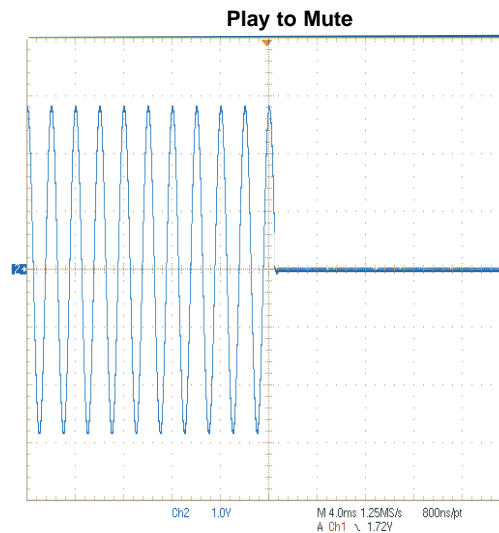


Figure 7.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in [Figure 8](#) illustrates the conventional line-driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

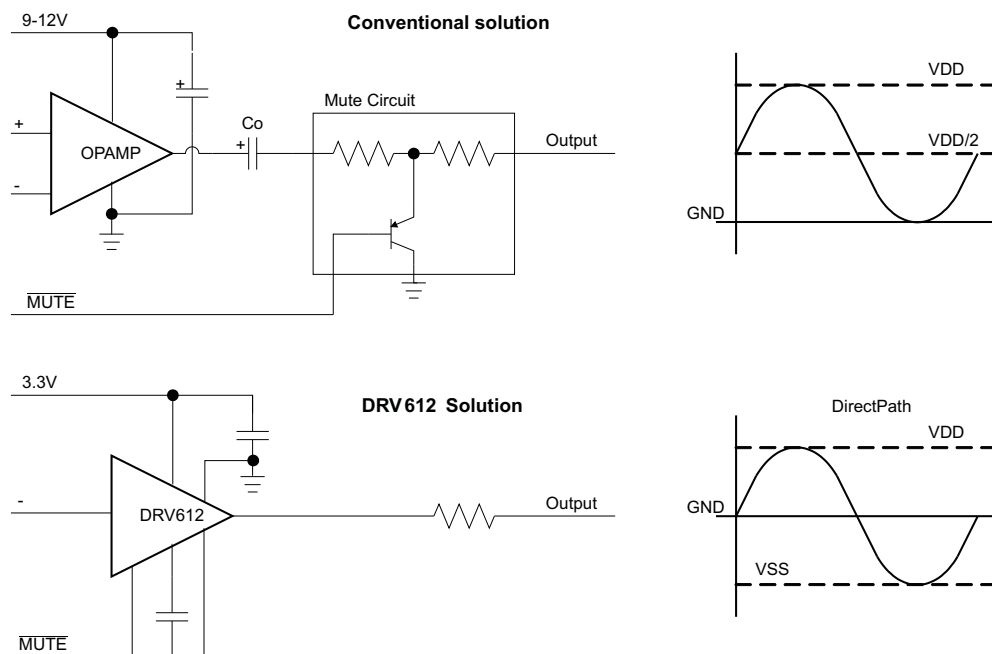


Figure 8. Conventional and DirectPath Line Driver

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click- and pop-reduction circuit, the DirectPath amplifier requires no output dc-blocking capacitors.

The bottom block diagram and waveform of [Figure 8](#) illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV612.

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COMPONENT SELECTION

Charge Pump Flying Capacitor and VSS Capacitor

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 μF is typical.

Decoupling Capacitors

The DRV612 is a DirectPath line-driver amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF , placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DRV612 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10- μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

Gain-Setting

The gain setting is programmed with the GAIN pin. Gain setting is latched during power on. [Table 1](#) lists the gain settings.

NOTE: If gain pin is left unconnected (open) default gain of $-2\times$ is selected.

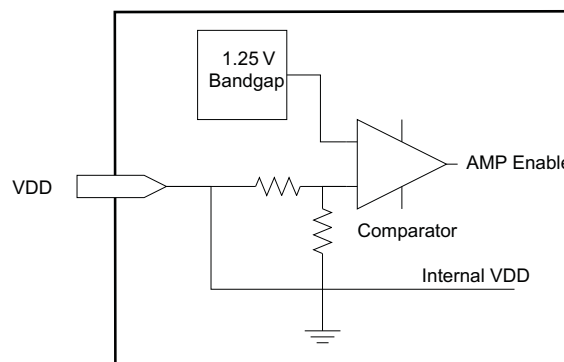
Table 1. Gain Settings

| Gain_set RESISTOR | GAIN | GAIN (dB) | INPUT RESISTANCE |
|-------------------------------|--------------|-----------|------------------|
| 249 k Ω ⁽¹⁾ | $-2\times$ | 6 | 37 k Ω |
| 82k5 | $-1\times$ | 0.0 | 55 k Ω |
| 51k1 | $-1.5\times$ | 3.5 | 44 k Ω |
| 34k8 | $-2.3\times$ | 7.2 | 33 k Ω |
| 27k4 | $-2.5\times$ | 8 | 31 k Ω |
| 20k5 | $-3\times$ | 9.5 | 28 k Ω |
| 15k4 | $-3.5\times$ | 10.9 | 24 k Ω |
| 11k5 | $-4.0\times$ | 12 | 22 k Ω |
| 9k09 | $-5\times$ | 14 | 18 k Ω |
| 7k5 | $-5.6\times$ | 15 | 17 k Ω |
| 6k19 | $-6.4\times$ | 16.1 | 15 k Ω |
| 5k11 | $-8.3\times$ | 18.4 | 12 k Ω |
| 4k22 | $-10\times$ | 20 | 10 k Ω |

(1) or higher

Internal Undervoltage Detection

The DRV612 contains an internal precision band-gap reference voltage and a comparator used to monitor the supply voltage, VDD. The internal VDD monitor is set at 2.8 V with 200-mV hysteresis.



Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV612. These capacitors block the dc portion of the audio source and allow the DRV612 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the dc gain to 1, limiting the dc-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN} . The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 2. Then the frequency and/or capacitance can be determined when one of the two values is given.

$$f_{C_{IN}} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi f_{C_{IN}} R_{IN}} \quad (1)$$

For a fixed cutoff frequency of 2 Hz, the size of the input capacitance is shown in Table 2 with the capacitors rounded up to nearest E6 values. For 20-Hz cutoff, simply divide the capacitor values with 10; e.g., for 1× gain, 150 nF is needed.

Table 2. Input Capacitor for Different Gain and Cutoff

| Gain_set RESISTOR | GAIN | Gain (dB) | INPUT RESISTANCE | 2 Hz Cutoff |
|----------------------|-------|--------------|---------------------|----------------|
| 249 kΩ | –2 × | 6 | 37 kΩ | 2.2 μF |
| 82k5 | –1 × | 0.0 | 55 kΩ | 1.5 μF |
| 51k1 | –1.5× | 3.5 | 44 kΩ | 2.2 μF |
| 34k8 | –2.3× | 7.2 | 33 kΩ | 3.3 μF |
| 27k4 | –2.5× | 8 | 31 kΩ | 3.3 μF |
| 20k5 | –3× | 9.5 | 28 kΩ | 3.3 μF |
| 15k4 | –3.5× | 10.9 | 24 kΩ | 3.3 μF |
| 11k5 | –4× | 12 | 22 kΩ | 4.7 μF |
| 9k09 | –5× | 14 | 18 kΩ | 4.7 μF |
| 7k5 | –5.6× | 15 | 17 kΩ | 4.7 μF |
| 6k19 | –6.4× | 16.1 | 15 kΩ | 6.8 μF |
| 5k11 | –8.3× | 18.4 | 12 kΩ | 6.8 μF |
| 4k22 | –10× | 20 | 10 kΩ | 10 μF |

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{MUTE}}$ pin low during power-supply ramp-up and -down. The pins should be kept low until the input ac-coupling capacitors are fully charged before asserting the $\overline{\text{MUTE}}$ pin high, this way proper pre-charge of the ac-coupling is performed and pop-less power up is achieved. Figure 9 illustrates the preferred sequence.

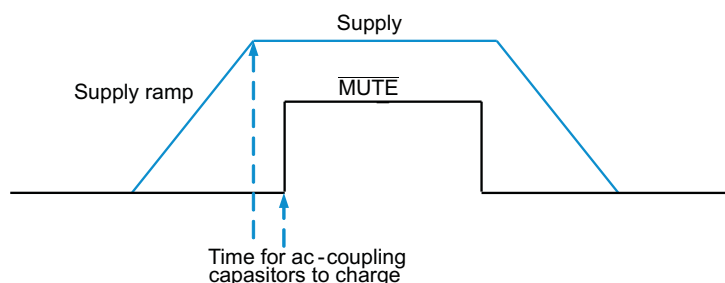


Figure 9. Power-Up/Down Sequence

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CAPACITIVE LOAD

The DRV612 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger for the line driver output.

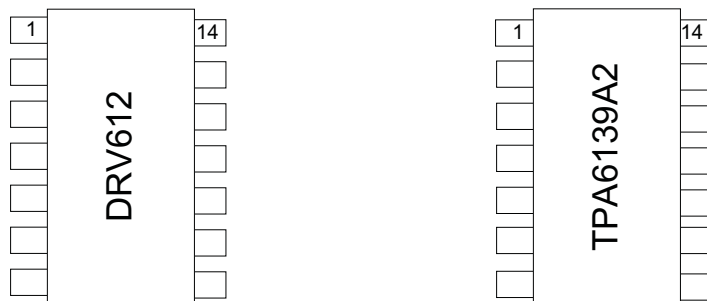
LAYOUT RECOMMENDATIONS

A proposed layout for the DRV612 can be seen in the DRV612EVM User's Guide ([SLOU248](#)), and the Gerber files can be downloaded from <http://focus.ti.com/docs/toolsw/folders/print/DRV612evm.html>. To access this information, open the DRV612 product folder and look in the Tools and Software folder.

Ground traces are recommended to be routed as a star ground to minimize hum interference. VDD, VSS decoupling capacitors and the charge-pump capacitors should be connected with short traces.

FOOTPRINT COMPATIBLE WITH TPA6139A2

The DRV612 stereo line driver is pin compatible with the headphone amplifier TPA6139A2. Therefore, a single PCB layout can be used with stuffing options for different board configurations.



APPLICATION CIRCUIT

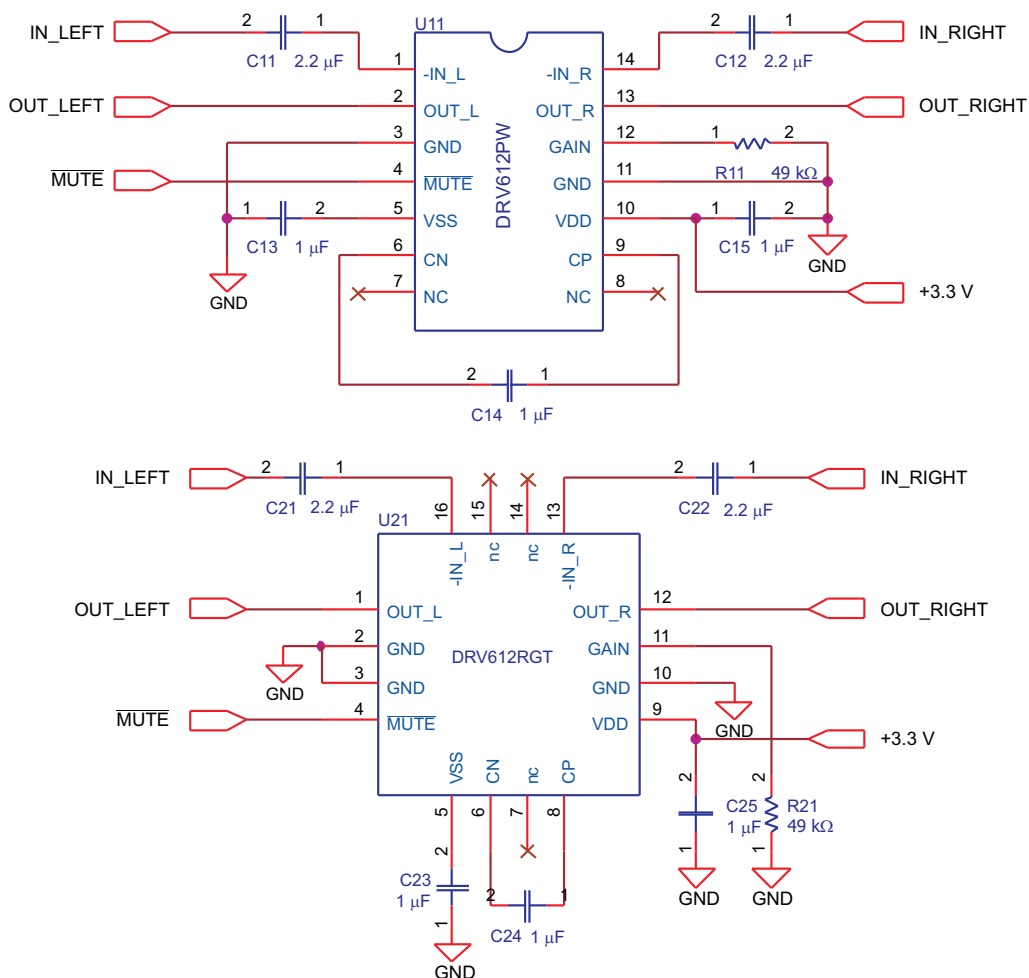


Figure 10. Single-Ended Input and Output, Gain Set to $-1.5\times$

REVISION HISTORY

| Changes from Original (December 2010) to Revision A | Page |
|---|------|
| • Added the QFN pinout drawing | 2 |
| • Added the QFN device To the PIN FUNCTIONS table | 2 |
| • Changed the Abs Max Storage Temp From: MIN = -40 To: MIN = -65 | 4 |
| • Changed the Gain resistor 2% tolerance values in the Programmable Gain Settings table For Gain Steps and Input Impedance | 6 |
| • Changed Note 1 of the PROGRAMMABLE GAIN SETTINGS table From: If pin 12, GAIN, is left floating To: If the GAIN pin is left floating | 6 |
| • Changed From: $C_{PUMP} = C_{(VSS)} = 10 \mu F$ To: $C_{PUMP} = C_{(VSS)} = 1 \mu F$ in the Typical Characteristics condition text | 7 |
| • Changed the Gain_set RESISTOR values in Table 1 | 10 |
| • Changed the Gain_set RESISTOR values in Table 2 | 11 |
| • Removed references to DRV614 from the FOOTPRINT COMPATIBLE WITH TPA6139A2 section | 13 |
| <hr/> | |
| Changes from Revision A (February 2011) to Revision B | Page |
| • Deleted the Product Preview note from the RGT package | 3 |
| • Changed $R_{IN} = 10 \text{ k}\Omega$, $R_{fb} = 20 \text{ k}\Omega$ To Gain = -2V/V in the Typical Characteristics condition text | 7 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DRV612PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DRV612 | Samples |
| DRV612PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DRV612 | Samples |
| DRV612RGTR | ACTIVE | QFN | RGT | 16 | 3000 | TBD | Call TI | Call TI | -40 to 85 | D612 | Samples |
| DRV612RGTT | ACTIVE | QFN | RGT | 16 | 250 | TBD | Call TI | Call TI | -40 to 85 | D612 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV612PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV612PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 38.0 |

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

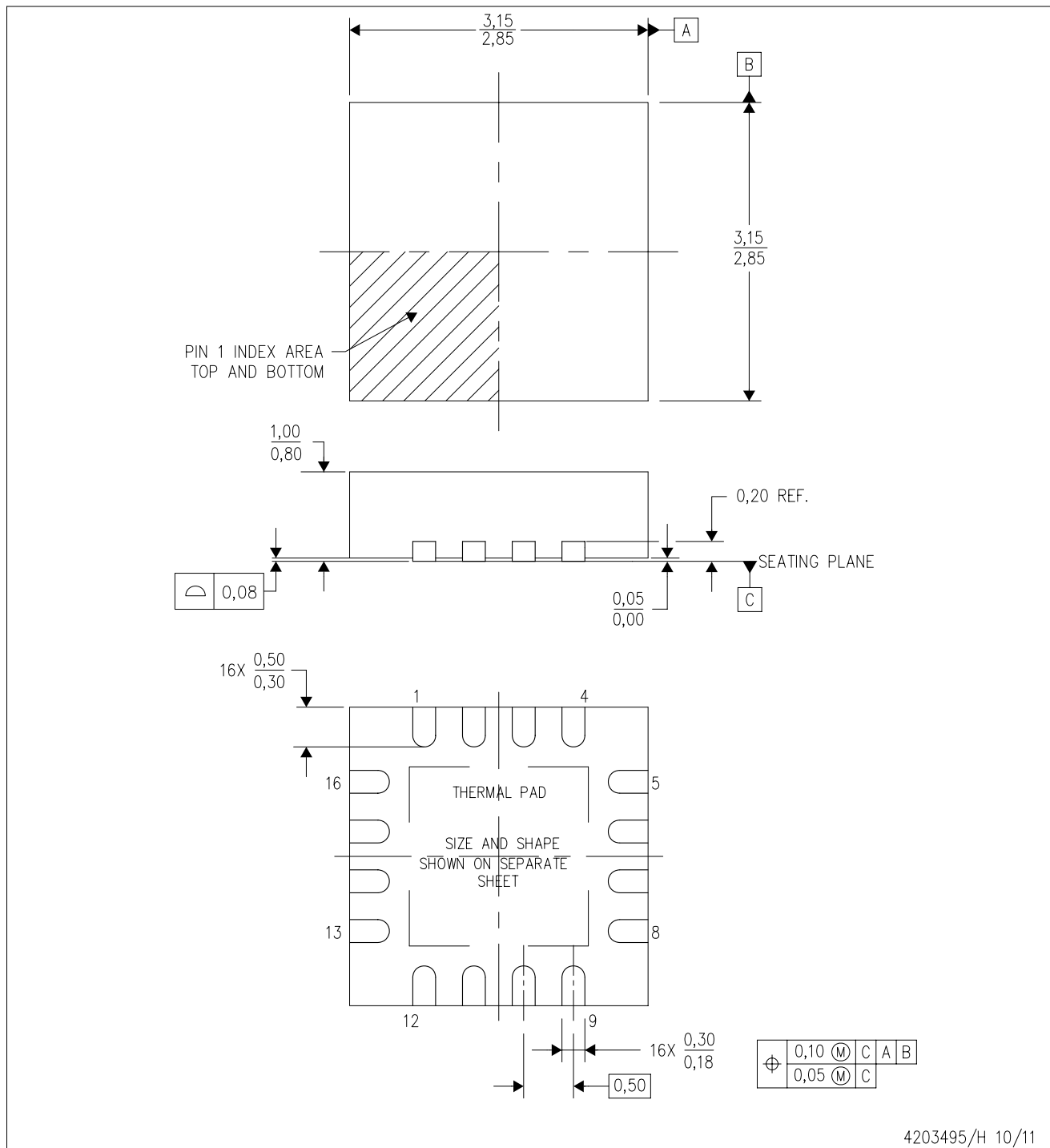
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

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