



## 7 & 8-Channel High-Speed ESD Protection Arrays

### Features

- Seven or eight channels of high-speed ESD protection
- Meets IEC-61000-4-2 Level 4 ESD protection requirements ( $\pm 8\text{kV}$  contact discharge)
- Meets IEC-61000-4-2  $\pm 15\text{kV}$  air discharge requirements
- Low loading capacitance at 3pF typical
- Low supply and leakage currents – ideal for battery-powered devices
- Small MSOP-10 package
- Lead-free versions available

### Applications

- High speed data line ESD protection
- DVI ports
- High resolution video (e.g. VGA ports)
- Expansion ports for Notebook/Handheld Computers
- 5V pseudo RS-232 ports

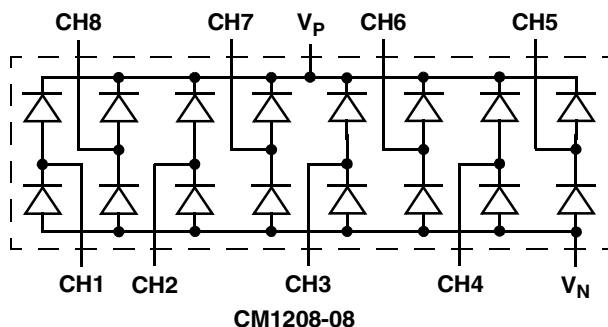
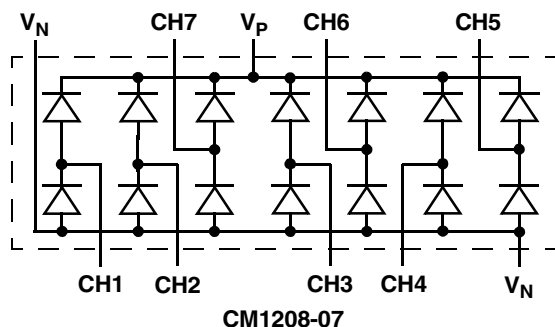
### Product Description

The CM1208-07/CM1208-08 is a diode array designed to provide either 7 or 8 channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes, which steers the ESD current pulse to either the positive ( $V_P$ ) or negative ( $V_N$ ) supply. The CM1208-07/08 devices will protect against ESD pulses up to 15kV contact discharge per the International Standard IEC61000-4-2.

These devices are particularly well-suited for portable electronics (e.g. handheld and notebook computers) because of its small package footprint, high ESD protection level, and low loading capacitance. They are also suitable for protecting video output lines and I/O ports in computers, set top boxes, digital TVs and peripheral equipment.

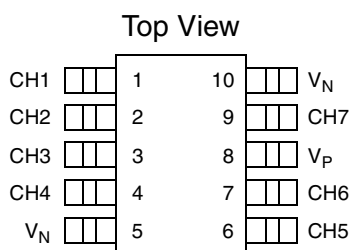
The CM1208-07/CM1208-08 is housed in a 10 pin MSOP package and is available with optional lead-free finishing.

### Electrical Schematics

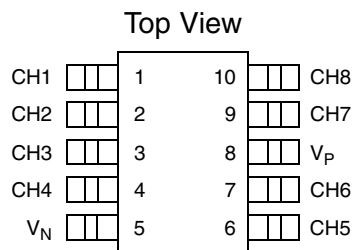




## PACKAGE / PINOUT DIAGRAMS



10-pin MSOP  
 CM1208-07MS  
 CM1208-07MR



10-pin MSOP  
 CM1208-08MS  
 CM1208-08MR

Note: These drawings are not to scale.

## PIN DESCRIPTIONS

DEVICE	PIN	NAME	TYPE	DESCRIPTION
-07,-08	1	CH 1	I/O	ESD Channel
-07,-08	2	CH 2	I/O	ESD Channel
-07,-08	3	CH 3	I/O	ESD Channel
-07,-08	4	CH 4	I/O	ESD Channel
-07,-08	5	$V_N$	GND	Negative voltage supply rail or ground reference rail
-07,-08	6	CH 5	I/O	ESD Channel
-07,-08	7	CH 6	I/O	ESD Channel
-07,-08	8	$V_P$	Supply	Positive voltage supply rail
-07,-08	9	CH 7	I/O	ESD Channel
-07	10	$V_N$	GND	Negative voltage supply rail or ground reference rail
-08	10	CH 8	I/O	ESD Channel

## Ordering Information

## PART NUMBERING INFORMATION

Pins	Package	Standard Finish		Lead-free Finish	
		Ordering Part Number <sup>1</sup>	Part Marking	Ordering Part Number <sup>1</sup>	Part Marking
10	MSOP	CM1208-07MS	0807	CM1208-07MR	807R
10	MSOP	CM1208-08MS	0808	CM1208-08MR	808R

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.



## Specifications

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply Voltage ( $V_P - V_N$ )	6.0	V
Diode Forward DC Current (Note 1)	20	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	( $V_N - 0.5$ ) to ( $V_P + 0.5$ )	V
Package Power Rating MSOP Package	300	mW

Note 1: Only one diode conducting at a time.

### STANDARD OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C
Operating Supply Voltage ( $V_P - V_N$ )	0 to 5.5	V

**ELECTRICAL OPERATING CHARACTERISTICS** (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_P$	Supply Current	$(V_P - V_N) = 5.0V$			10	$\mu A$
$V_F$	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 20mA$ ; $T_A = 25^\circ C$	0.60 0.65	0.7 0.8	0.95 0.95	V V
$I_{LEAK}$	Channel Leakage Current	$T_A = 25^\circ C$		$\pm 0.1$	$\pm 1.0$	$\mu A$
$C_{IN}$	Channel Input Capacitance	At 1 MHz, OSC Level = 30mV, $V_P = 5V$ , $V_N = 0V$ , $V_{CH} = 2.5V$ ; Note 2 applies		3	5	pF
$V_{ESD}$	ESD Protection Peak Discharge Voltage at any channel input a) Contact discharge per IEC 61000-4-2 standard b) Human Body Model, MIL-STD-883, Method 3015	Notes 2, 3 & 5 Notes 2, 3 & 4	$\pm 8$ $\pm 15$			kV kV
$V_{CL}$	Channel Clamp Voltage  Positive Transients Negative Transients	At 8kV ESD HBM; $T_A = 25^\circ C$ ; Note 2, 3 & 4			$V_P + 5.0$ $V_N - 5.0$	V V

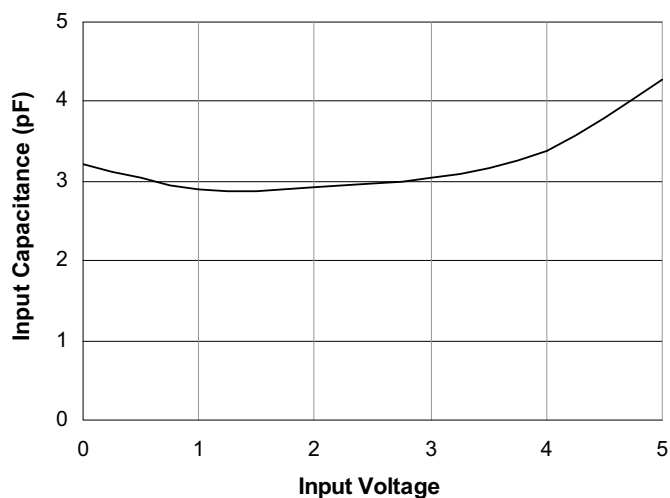
Note 1: All parameters specified at  $T_A = -40$  to  $+85^\circ C$  unless otherwise noted.

Note 2: These parameters guaranteed by design and characterization.

Note 3: From I/O pins to  $V_P$  or  $V_N$  only. A bypass capacitor between  $V_P$  and  $V_N$  is required. It is recommended that  $V_P$  be bypassed to  $V_N$  with a 0.2 $\mu F$  ceramic capacitor.

Note 4: Human Body Model per MIL-STD-883, Method 3015,  $C_{Discharge} = 100pF$ ,  $R_{Discharge} = 1.5K\Omega$ ,  $V_P = 5.0V$ ,  $V_N$  grounded.

Note 5: Standard IEC 61000-4-2 with  $C_{Discharge} = 150pF$ ,  $R_{Discharge} = 330\Omega$ ,  $V_P = 5.0V$ ,  $V_N$  grounded.

**Performance Information****Typical Channel Input Capacitance vs. Channel Input Voltage at  $T_A = 25^\circ C$** **Typical Variation of  $C_{IN}$  vs.  $V_{IN}$** 

( $V_P = 5V$ ,  $V_N = 0V$ , 0.2  $\mu F$  chip capacitor between  $V_P$  and  $V_N$ )

## Application Information

### Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to [Figure 1](#), which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by  $L_1$  and  $L_2$ . The voltage  $V_{CL}$  on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where  $I_{ESD}$  is the ESD current pulse, and  $V_{SUPPLY}$  is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here  $d(I_{ESD})/dt$  can be approximated by  $\Delta I_{ESD}/\Delta t$ , or  $30/(1 \times 10^{-9})$ . So just 10nH of series inductance ( $L_1$  and  $L_2$  combined) will lead to a 300V increment in  $V_{CL}$ !

Similarly for negative ESD pulses, parasitic series inductance from the  $V_N$  pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the  $V_{CL}$  equation above, the  $V_{SUPPLY}$  term, in reality, is given by  $(V_{DC} + I_{ESD} \times R_{OUT})$ , where  $V_{DC}$  and  $R_{OUT}$  are the nominal supply DC output voltage and effective output imped-

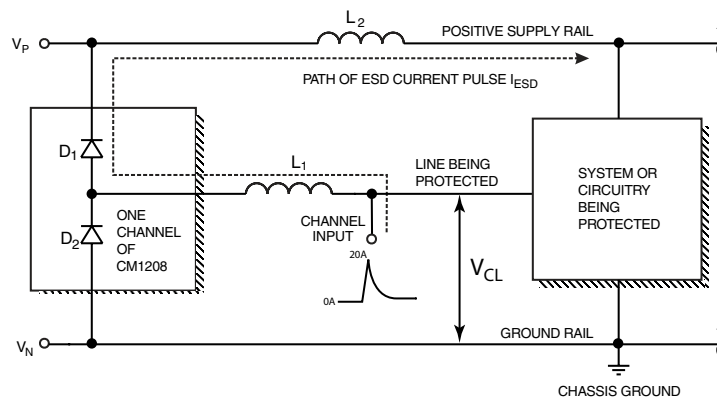
ance of the power supply respectively. As an example, a  $R_{OUT}$  of 1 ohm would result in a 10V increment in  $V_{CL}$  for a peak  $I_{ESD}$  of 10A.

To mitigate these effects, a high frequency bypass capacitor should be connected between the  $V_P$  pin of the ESD Protection Array and the ground plane. The value of this bypass capacitor should be chosen such that it will absorb the charge transferred by the ESD pulse with minimal change in  $V_P$ . Typically a value in the 0.1 $\mu$ F to 0.2 $\mu$ F range is adequate for IEC-61000-4-2 level 4 contact discharge protection (8kV). For higher ESD voltages, the bypass capacitor should be increased accordingly. Ceramic chip capacitors mounted with short printed circuit board traces are good choices for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the  $V_P$  pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

### Additional Information

See also California Micro Devices Application Note AP209, "Design Considerations for ESD Protection."



**Figure 1. Application of Positive ESD Pulse between Input Channel and Ground**

## Mechanical Details

### MSOP Mechanical Specifications:

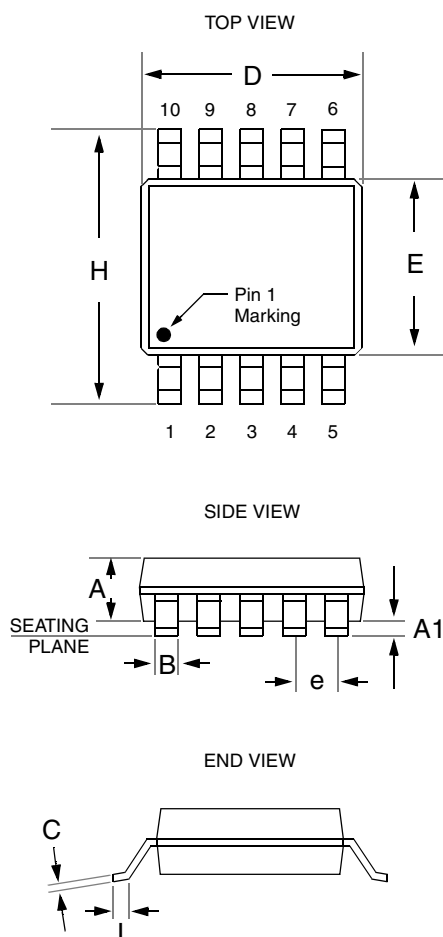
CM1208-07/08 devices are packaged in 10-pin MSOP packages. Dimensions are presented below.

For complete information on the MSOP-10 package, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.18	0.40	0.006	0.016
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.76	5.00	0.187	0.197
L	0.40	0.70	0.0137	0.029
# per tube	80 pieces*			
# per tape and reel	4000			
Controlling dimension: inches				

\* This is an approximate number which may vary.

### Mechanical Package Diagrams



**Package Dimensions for MSOP-10**