Integrated Circuit Systems, Inc.

ICS9DB102

2 Output PCI Express* Buffer with CLKREQ# Function

Recommended Application:

- 1-to-2 Zero-delay or fanout buffer for PCI Express

Output Features:

- 2 - 0.7V current mode differential output pairs (HSCL)

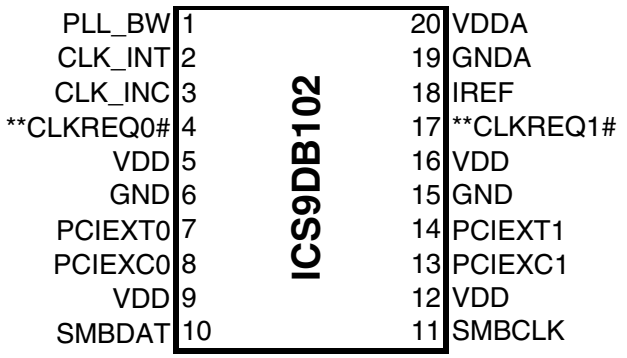
Key Specifications:

- Cycle-to-cycle jitter < 35ps
- Output-to-output skew < 25 ps

Features/Benefits:

- CLKREQ# pin for outputs 1 and 4/output enable for Express Card applications
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled

Pin Configuration



Note: Pins preceeded by '**' have internal 120K ohm pull down resistors

20-pin SSOP & TSSOP

*Other names and brands may be claimed as the property of others.

Pin Description

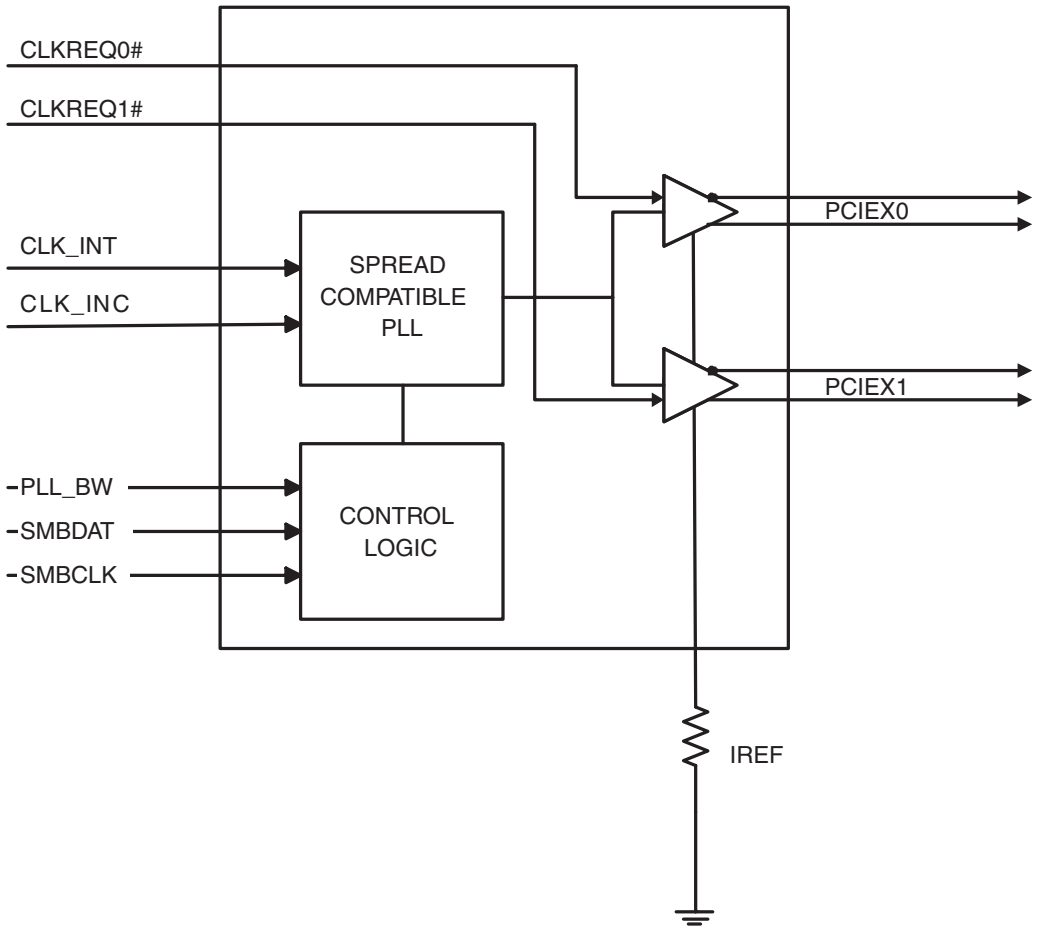
PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	PLL_BW	IN	3.3V input for selecting PLL Band Width 0 = low, 1= high
2	CLK_INT	IN	"True" reference clock input.
3	CLK_INC	IN	"Complementary" reference clock input.
4	**CLKREQ0#	IN	Output enable for SRC/PCI Express output pair '0' 0 = enabled, 1 = tri-stated
5	VDD	PWR	Power supply, nominal 3.3V
6	GND	PWR	Ground pin.
7	PCIEXT0	OUT	True clock of differential PCI_Express pair.
8	PCIEXC0	OUT	Complement clock of differential PCI_Express pair.
9	VDD	PWR	Power supply, nominal 3.3V
10	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
11	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
12	VDD	PWR	Power supply, nominal 3.3V
13	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
14	PCIEXT1	OUT	True clock of differential PCI_Express pair.
15	GND	PWR	Ground pin.
16	VDD	PWR	Power supply, nominal 3.3V
17	**CLKREQ1#	IN	Output enable for SRC/PCI Express output pair '1' 0 = enabled, 1 = tri-stated
18	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
19	GNDA	PWR	Ground pin for the PLL core.
20	VDDA	PWR	3.3V power for the PLL core.

Note:
Pins preceeded by '**' have internal 120K ohm pull down resistors

General Description

The **ICS9DB102** zero-delay buffer supports PCI Express clocking requirements. The **ICS9DB102** is driven by a differential SRC output pair from an ICS CK409/CK410-compliant main clock generator such as the ICS952601 or ICS954101. It attenuates jitter on the input clock and has a selectable PLL Band Width to maximize performance in systems with or without Spread-Spectrum clocking. An SMBus interface allows control of the PLL bandwidth and bypass options, while 2 clock request (OE#) pins make the **ICS9DB102** suitable for Express Card applications.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
5,9,12,16	6,15	PCI Express Outputs
9	6	SMBUS
20	19	IREF
20	19	Analog VDD & GND for PLL core

Absolute Max

Symbol	Parameter	Min	Max	Units
VDDA	3.3V Core Supply Voltage		V_{DD} + 0.5V	V
VDD	3.3V Output Supply Voltage	GND - 0.5	V_{DD} + 0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;		75	100	mA	1
		all differential pairs tri-stated		27	50	mA	1
Input Frequency[3]	F_i	V_{DD} = 3.3 V	99	100	101	MHz	1
Pin Inductance[1]	L_{pin}				7	nH	1
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			4.5	pF	1
Clk Stabilization[1,2]	T_{STAB}	From V_{DD} Power-Up to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Spread Spectrum Modulation Frequency	f_{MOD}	Lexmark Modulation	25		45	KHz	1
PLL Bandwidth	BW	PLL Bandwidth when PLL_BW=0		400		KHz	1
		PLL Bandwidth when PLL_BW=1		1.2		MHz	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	$V_{OLSMBUS}$	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}	SMBus SDATA pin	4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - PCIEX 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1,3
Min Voltage	Vuds		-300				1,3
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1,3
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1,3
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r			30	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Input to Output Delay	t_{pd}	PLL Mode.	135		185	ps	1
	t_{pdbyp}	Bypass mode	3.2		3.7	ns	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Output-to-Output Skew	t_{sk3}	V_T = 50%			25	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode. Measurement from differential wavefrom			35	ps	1
	$t_{jcyc-cycbyp}$	Additve Jitter in Bypass Mode			30	ps	1

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that the input clock complies with CK409/CK410 accuracy requirements

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

SMBus Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SW_EN	Enables SMBus Control	RW	Functions controlled by SMBus registers	Functions controlled by device pins	1
Bit 6	-	RESERVED		RW	-		X
Bit 5	-	RESERVED		RW	-		X
Bit 4	-	RESERVED		RW	-		X
Bit 3	-	RESERVED		RW	-		X
Bit 2	-	RESERVED		RW	-		X
Bit 1	-	PLL BW #adjust	Selects PLL Bandwidth	RW	Low BW	High BW	1
Bit 0	-	PLL Enable	Bypasses PLL for board test	RW	PLL bypassed (fan out mode)	PLL enabled (ZDB mode)	1

SMBus Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RESERVED		RW	-		X
Bit 6	-	RESERVED		RW	-		X
Bit 5	-	RESERVED		RW	-		X
Bit 4	-	RESERVED		RW	-		X
Bit 3	-	RESERVED		RW	-		X
Bit 2	-	RESERVED		RW	-		X
Bit 1	-	RESERVED		RW	-		X
Bit 0	-	RESERVED		RW	-		X

SMBus Table: Function Select Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED		RW	-		X
Bit 6		RESERVED		RW	-		X
Bit 5	-	RESERVED		RW	-		X
Bit 4	-	RESERVED		RW	-		X
Bit 3	-	RESERVED		RW	-		X
Bit 2	-	RESERVED		RW	-		X
Bit 1	-	RESERVED		RW	-		X
Bit 0	-	RESERVED		RW	-		X

SMBus Table: Vendor & Revision ID Register

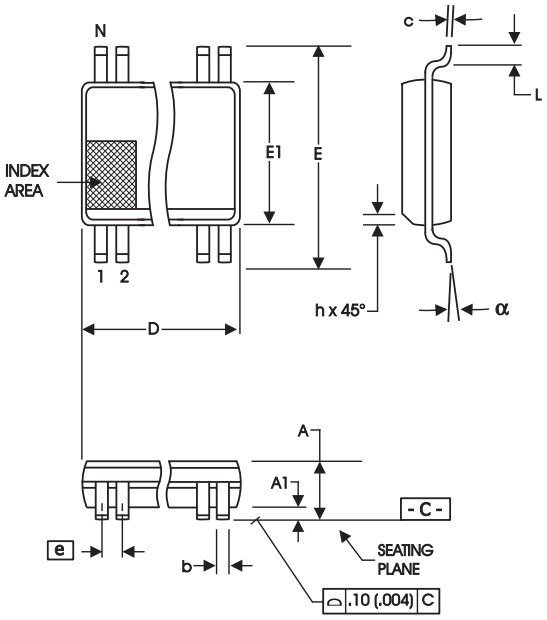
Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Device ID = 06 Hex	R	-		0
Bit 6	-			R	-		0
Bit 5	-			R	-		0
Bit 4	-			R	-		0
Bit 3	-			R	-		0
Bit 2	-			R	-		1
Bit 1	-			R	-		1
Bit 0	-			R	-		0

SMBus Table: Byte Count Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 06 = 6 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	0



20-Lead, 150 mil SSOP (QSOP)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.053	.069
A1	0.10	0.25	.004	.010
A2	--	1.50	--	.059
b	0.20	0.30	.008	.012
c	0.18	0.25	.007	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 BASIC		0.025 BASIC	
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
ZD	SEE VARIATIONS		SEE VARIATIONS	

VARIATIONS

N	D mm.		ZD	D (inch)		ZD
	MIN	MAX	(Ref)	MIN	MAX	(Ref)
20	8.55	8.75	1.47	.337	.344	.058

Reference Doc.: JEDEC Publication 95, MO-137

10-0032

Ordering Information

ICS9DB102yFLFT

Example:

ICS XXXX y F LF T

Designation for tape and reel packaging

Lead Free, RoHS Compliant (Optional)

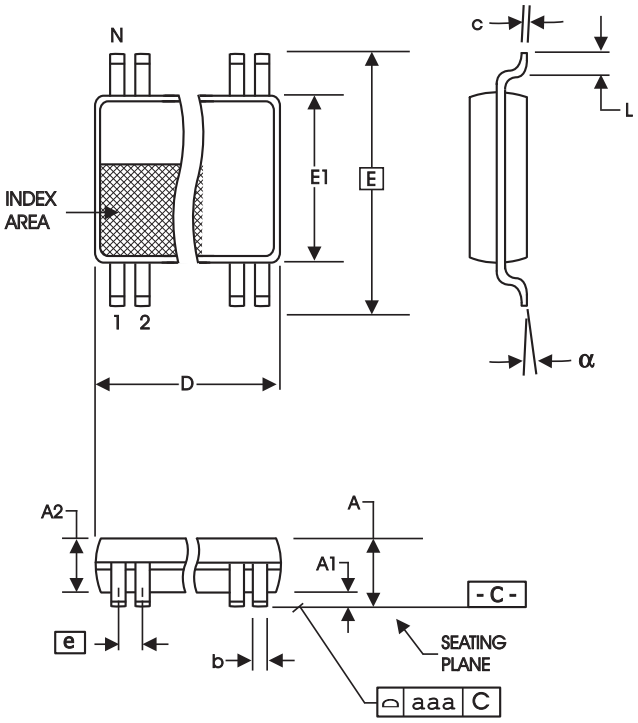
Package Type
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 to 7 digit numbers)

Prefix
ICS, AV = Standard Device

0852C—09/12/05



20-Lead, 4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
20	6.40	6.60	.252	.260

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

ICS9DB102yGLFT

Example:

ICS XXXX yG LF T

Designation for tape and reel packaging
Lead Free, RoHS Compliant (Optional)
Package Type
G = TSSOP
Revision Designator (will not correlate with datasheet revision)
Device Type (consists of 3 to 7 digit numbers)
Prefix
ICS, AV = Standard Device

0852C—09/12/05

Revision History

Rev.	Issue Date	Description	Page #
C	9/12/2005	1. Changed PLL mode jitter from 40ps to 35ps. 2. Changed Bypass mode addictive jitter from 25ps to 30ps. 3. Updated LF Ordering Information. 4. Finla Release.	5, 8-9