

General Description

The AAT8543 is a low threshold P-channel MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech's ultra-high-density MOSFET process and space-saving, small-outline, J-lead package, performance superior to that normally found in a TSOP-6 footprint has been squeezed into the footprint of an SC70JW-8 package.

Applications

- Battery Packs
- Battery-Powered Portable Equipment
- Cellular and Cordless Telephones

Absolute Maximum Ratings

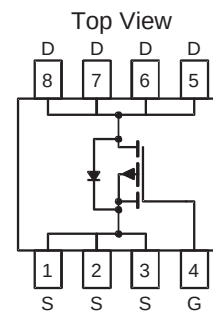
$T_A = 25^\circ\text{C}$, unless otherwise noted.

Symbol	Description	Value	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	
I_D	Continuous Drain Current @ $T_J = 150^\circ\text{C}^1$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
I_{DM}	Pulsed Drain Current ²	± 20	
I_S	Continuous Source Current (Source-Drain Diode) ¹	-1.2	
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Features

- Drain-Source Voltage (max): -20V
- Continuous Drain Current¹ (max):
-4.2A @ 25°C
- Low On-Resistance:
 - $57\text{m}\Omega$ @ $V_{GS} = -4.5\text{V}$
 - $104\text{m}\Omega$ @ $V_{GS} = -2.5\text{V}$

SC70JW-8 Package



Thermal Characteristics¹

Symbol	Description	Typ	Max	Units
$R_{\theta JA}$	Typical Junction-to-Ambient Steady State	100	124	$^\circ\text{C}/\text{W}$
$R_{\theta JA2}$	Maximum Junction-to-Ambient $t \leq 5$ Seconds	62	76	$^\circ\text{C}/\text{W}$
$R_{\theta JF}$	Typical Junction-to-Foot	35	42	$^\circ\text{C}/\text{W}$
P_D	Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	1.6	W
		$T_A = 70^\circ\text{C}$	1.0	

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

2. Pulse test: Pulse Width = 300 μs .

Electrical Characteristics

$T_J = 25^\circ\text{C}$, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
DC Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-20			V
R _{DS(ON)}	Drain-Source On-Resistance ¹	V _{GS} = -4.5V, I _D = -4.2A		45	57	mΩ
		V _{GS} = -2.5V, I _D = -3.1A		80	104	
I _{D(ON)}	On-State Drain Current ¹	V _{GS} = -4.5V, V _{DS} = -5V (pulsed)	-20			A
V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = -250μA	-0.6			V
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±12V, V _{DS} = 0V			±100	nA
I _{DSS}	Drain Source Leakage Current	V _{GS} = 0V, V _{DS} = -20V			-1	μA
		V _{GS} = 0V, V _{DS} = -16V, T _J = 70°C ²			-5	
g _{fs}	Forward Transconductance ¹	V _{DS} = -5V, I _D = -4.2A		7		S
Dynamic Characteristics ²						
Q _G	Total Gate Charge	V _{DS} = -10V, R _D = 2.4Ω, V _{GS} = -4.5V		8.5		nC
Q _{GS}	Gate-Source Charge	V _{DS} = -10V, R _D = 2.4Ω, V _{GS} = -4.5V		1.5		
Q _{GD}	Gate-Drain Charge	V _{DS} = -10V, R _D = 2.4Ω, V _{GS} = -4.5V		2.8		
t _{D(ON)}	Turn-On Delay	V _{DS} = -10V, R _D = 2.4Ω, V _{GS} = -4.5V, R _G = 6Ω		10		ns
t _R	Turn-On Rise Time	V _{DS} = -10V, R _D = 2.4Ω, V _{GS} = -4.5V, R _G = 6Ω		32		
t _{D(OFF)}	Turn-Off Delay	V _{DS} = -10V, R _D = 2.4Ω, V _{GS} = -4.5V, R _G = 6Ω		61		
t _F	Turn-Off Fall Time	V _{DS} = -10V, R _D = 2.4Ω, V _{GS} = -4.5V, R _G = 6Ω		38		
Source-Drain Diode Characteristics						
V _{SD}	Source-Drain Forward Voltage ¹	V _{GS} = 0, I _S = -4.2A			-1.3	V
I _S	Continuous Diode Current ³				-1.2	A

1. Pulse test: Pulse Width = 300 μs .

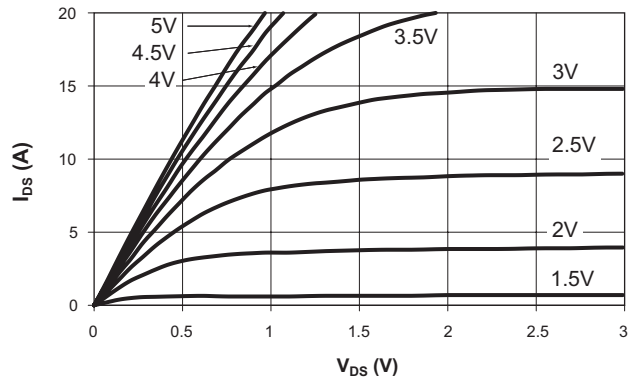
2. Guaranteed by design. Not subject to production testing.

3. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

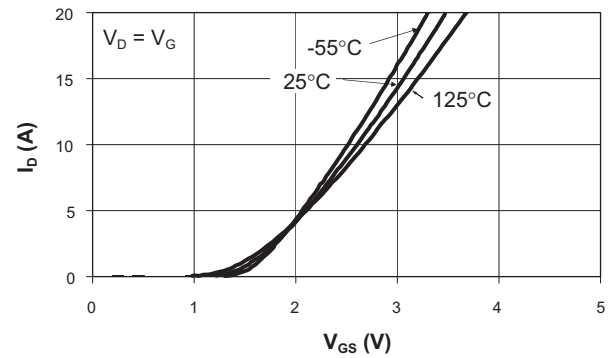
Typical Characteristics

$T_J = 25^\circ\text{C}$, unless otherwise noted.

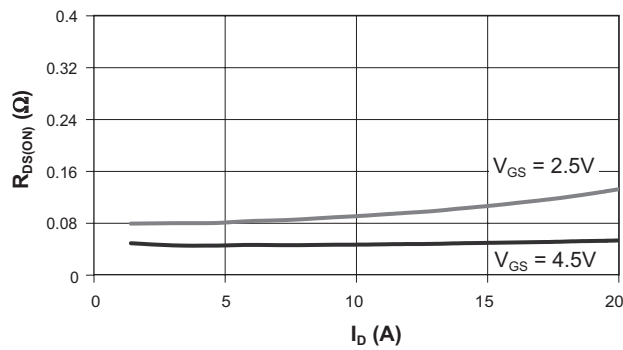
Output Characteristics



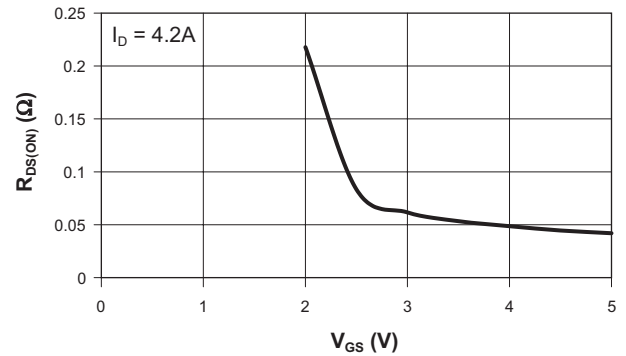
Transfer Characteristics



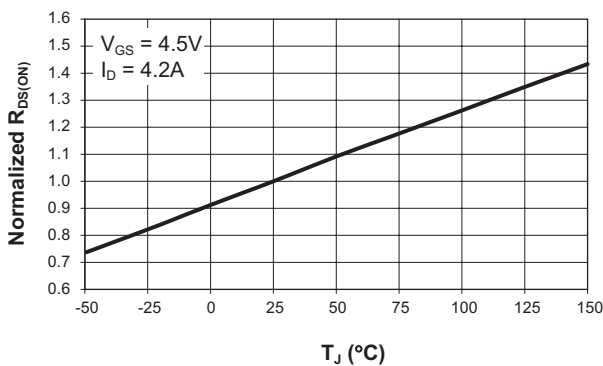
On-Resistance vs. Drain Current



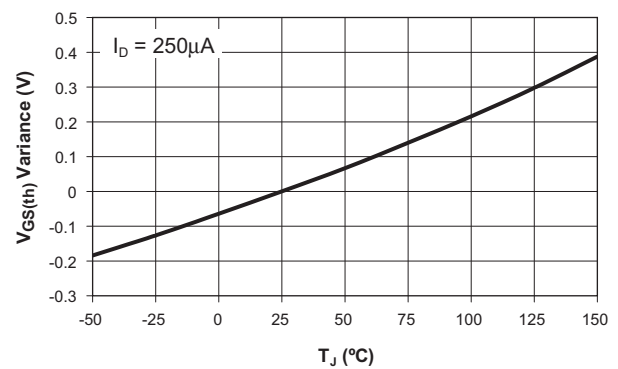
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature



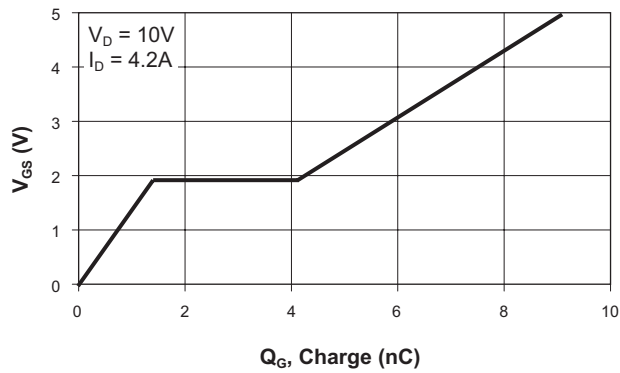
Threshold Voltage



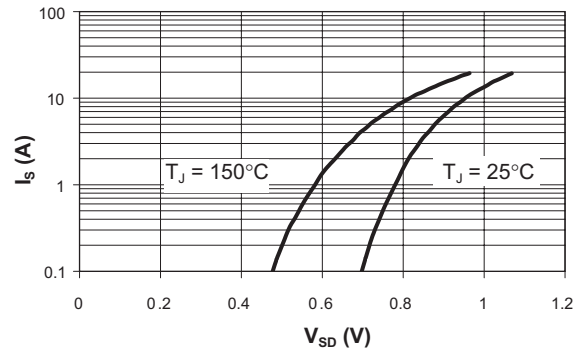
Typical Characteristics

$T_J = 25^\circ\text{C}$, unless otherwise noted.

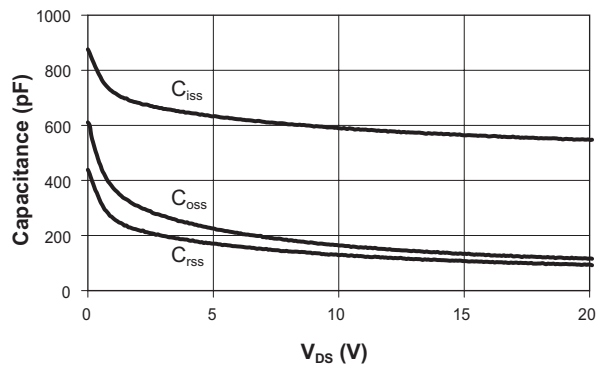
Gate Charge



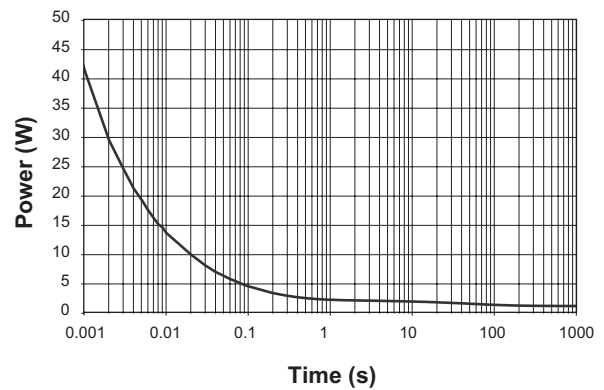
Source-Drain Diode Forward Voltage



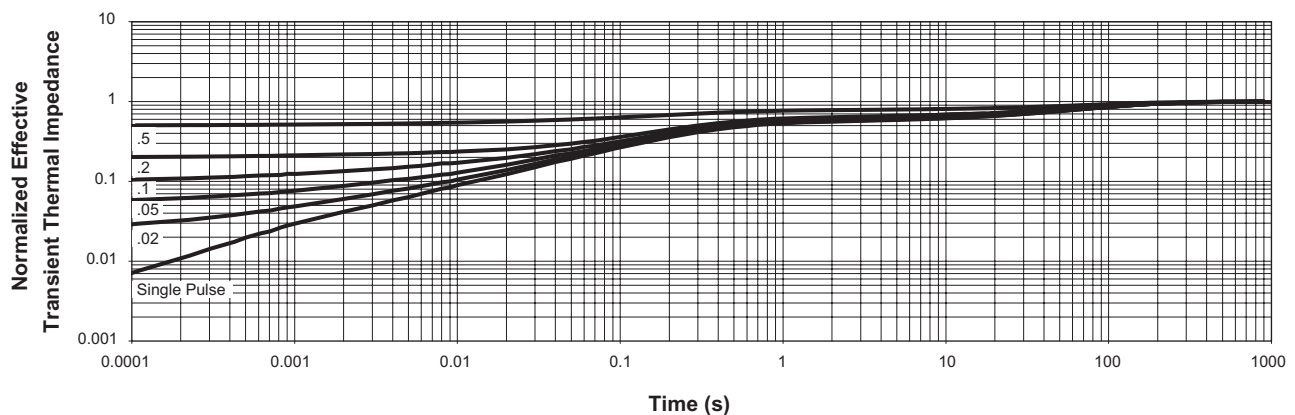
Capacitance



Single Pulse Power, Junction to Ambient



Transient Thermal Response, Junction to Ambient

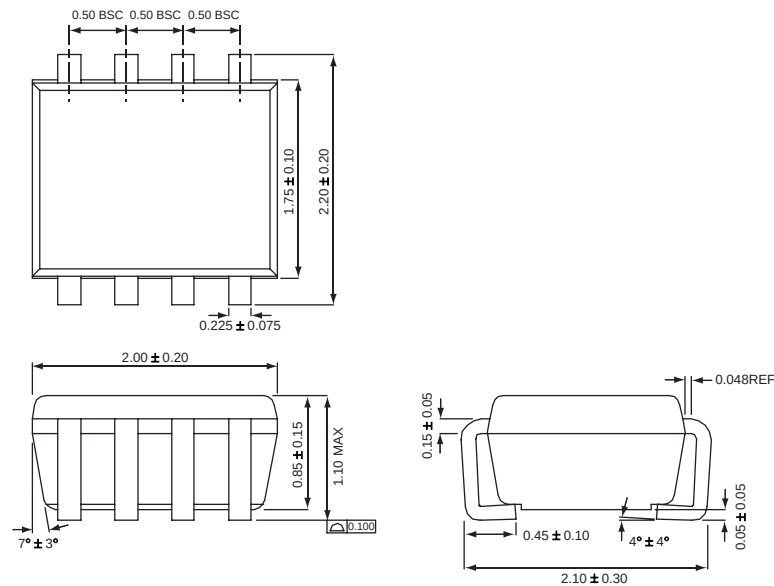


Ordering Information

Package	Marking ¹	Part Number (Tape and Reel) ²
SC70JW-8	JTXY	AAT8543IJS-T1

Package Information

SC70JW-8



All dimensions in millimeters.

1. XYY = assembly and date code.
 2. Sample stock is generally held on part numbers listed in **BOLD**.

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