SONY

5-channel 3-LD Driver for Optical Disk Drive

# CXA2765ER

## Description

The CXA2765ER is a laser driver IC that can drive optical disk lasers capable of writing the three formats of CD, DVD and BD.
(Applications: Writable 3-wavelength optical disk drive)

## Features

- ◆ Supports power save mode with register setting LDOFF
- ◆ LD drivers
  - ◆ Three LD drivers for CD, DVD and BD
  - ◆ Maximum driving current
    - OUTBD: Total = 450mA (Each channel: 150mA, 200mA, 150mA, 50mA, 150mA)
    - OUT1, OUT2: Total = 800mA (Each channel: 180mA, 400mA, 300mA, 150mA, 180mA)
  - ◆ Driver current noise: 0.4nA/$\sqrt{\text{Hz}}$ (Read)
  - ◆ 5-channel control allows generation of a 5-value recording waveform
  - ◆ Register setting of high-frequency modulator (HFM) frequency and amplitude
    - Frequency: 200MHz to 600MHz, 8 bits
    - Amplitude: 0mAp-p to 100mAp-p, 8 bits
  - ◆ IOP monitor using the VIOPMON pin (BD only)
  - ◆ VOP monitor using the VIOPMON pin
  - ◆ Register setting of HFM spectrum diffusion function (Modulation frequency: 2 bits, diffusion frequency: 2 bits)

## Package

32-pin VQFN (Plastic)

## Structure

CMOS IC

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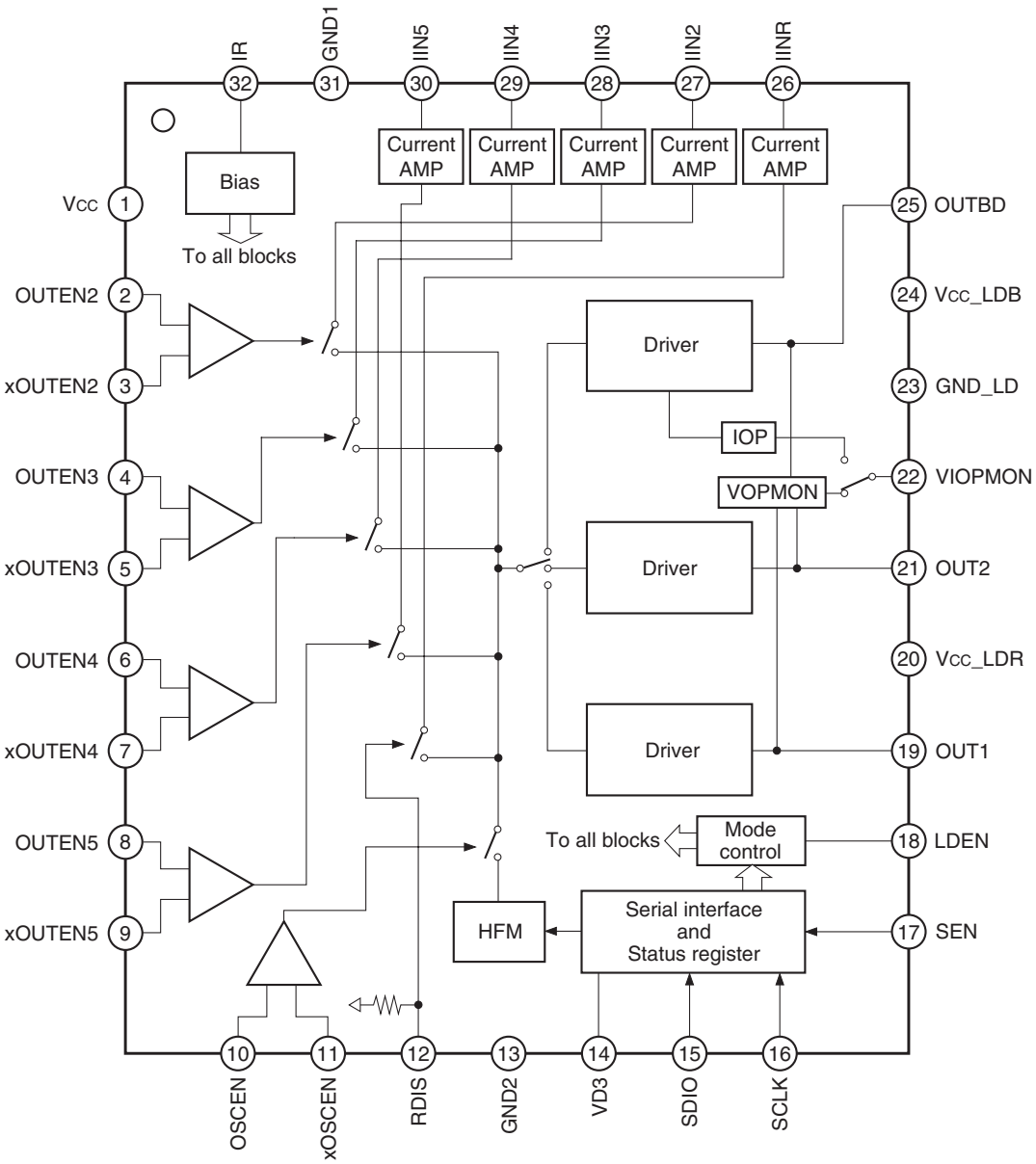
## Absolute Maximum Ratings

| | | | | |
|---|---|---|---|---|
| ◆ Supply voltage | $V_{CC}$ | 6 | V | |
| | $V_{CC}$_LDR | 6 | V | |
| | $V_{CC}$_LDB | 10.0 | V | (When BD_LD is OFF) |
| ◆ Storage temperature | Tstg | –65 to +150 | ˚C | |
| ◆ Junction temperature | Tjmax | 150 | ˚C | |
| ◆ OUTBD pin voltage | OUTBD_OFF | < 7 | V | (When BD_LD is OFF) |

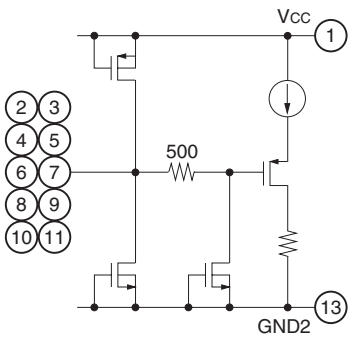
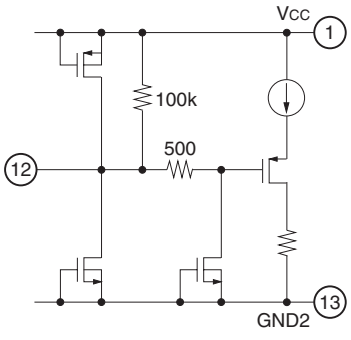
## Operating Conditions

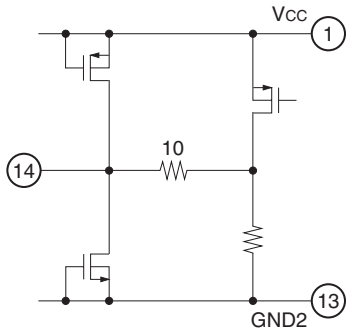
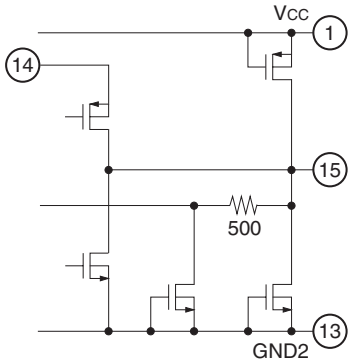
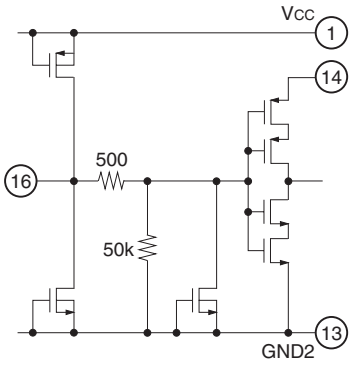
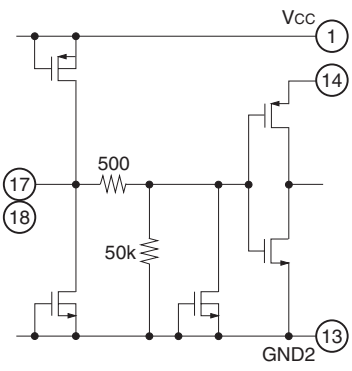
| | | | | |
|---|---|---|---|---|
| ◆ Supply voltage | $V_{CC}$ | 4.5 to 6 | V | |
| | $V_{CC}$_LDR | 4.5 to 6 | V | |
| | $V_{CC}$_LDB | 5 to 9 | V | (When BD_LD is ON) |
| ◆ Operating temperature | Topr | $-10 \leq Topr \leq 150 - \Delta Tj$ | ˚C | |
| ◆ OUTBD pin voltage | OUTBD_ON | < 5 | V | (When BD_LD is ON) |

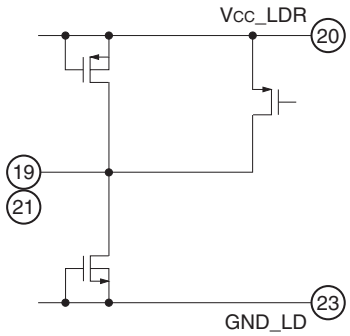
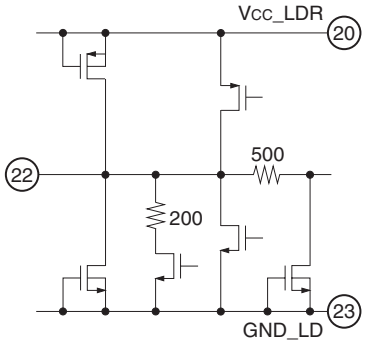
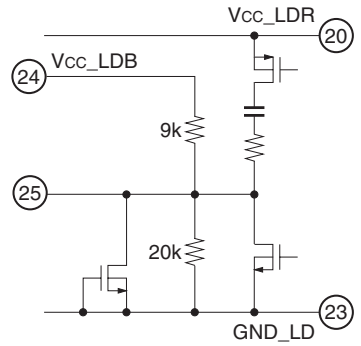
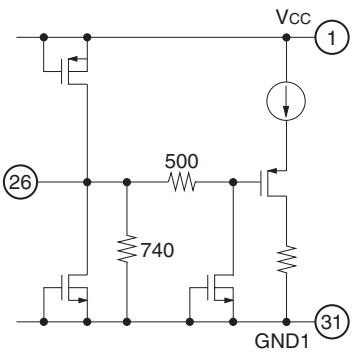
## Block Diagram and Pin Configuration

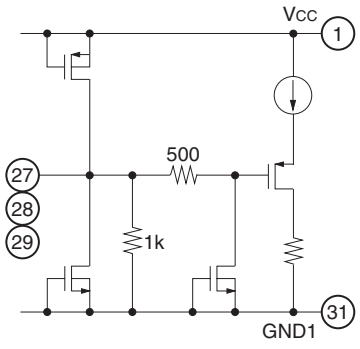
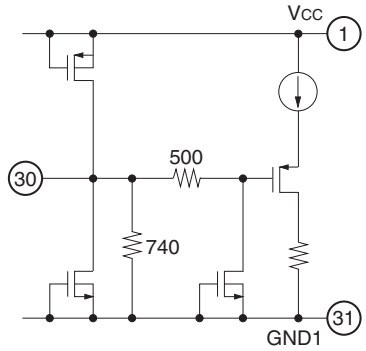
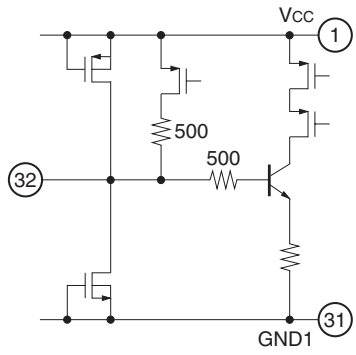


## Pin Description

| Pin No. | Symbol | I/O | Pin voltage [V] | Equivalent circuit | Description |
|---|---|---|---|---|---|
| 1 | VCC | — | 4.5 to 6.0 | — | Supply voltage for input signal, bias and timing blocks |
| 2 | OUTEN2 | I | — |  | IIN2 setting current control signal input (positive logic): LVDS/CMOS<br>Fix to GND when not used. |
| 3 | xOUTEN2 | I | — | | IIN2 setting current control signal input (negative logic): LVDS<br>Not used in single input mode.<br>Fix to VCC when not used. |
| 4 | OUTEN3 | I | — | | IIN3 setting current control signal input (positive logic): LVDS/CMOS<br>Fix to GND when not used. |
| 5 | xOUTEN3 | I | — | | IIN3 setting current control signal input (negative logic): LVDS<br>Not used in single input mode.<br>Fix to VCC when not used. |
| 6 | OUTEN4 | I | — | | IIN4 setting current control signal input (positive logic): LVDS/CMOS<br>Fix to GND when not used. |
| 7 | xOUTEN4 | I | — | | IIN4 setting current control signal input (negative logic): LVDS<br>Not used in single input mode.<br>Fix to VCC when not used. |
| 8 | OUTEN5 | I | — | | IIN5 setting current control signal input (positive logic): LVDS/CMOS<br>Fix to GND when not used. |
| 9 | xOUTEN5 | I | — | | IIN5 setting current control signal input (negative logic): LVDS<br>Not used in single input mode.<br>Fix to VCC when not used. |
| 10 | OSCEN | I | — | | HFM control signal input (positive logic): LVDS<br>Not used in single input mode.<br>Fix to GND when not used. |
| 11 | xOSCEN | I | — | | HFM control signal input (negative logic): LVDS/CMOS<br>Fix to VCC when not used. |
| 12 | RDIS | I | — |  | IINR setting current control signal input (negative logic)<br>(with pull-up resistor) |

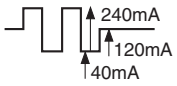
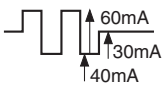
| Pin No. | Symbol | I/O | Pin voltage [V] | Equivalent circuit | Description |
|---|---|---|---|---|---|
| 13 | GND2 | — | — | — | Timing block GND |
| 14 | VD3 | — | 3.3 |  | Voltage decoupling for serial register circuit (Connect to GND through 0.1μF.) |
| 15 | SDIO | I/O | — |  | Serial register data I/O |
| 16 | SCLK | I | — |  | Serial register clock input (with pull-down resistor) |
| 17 | SEN | I | — |  | Serial register chip select input (with pull-down resistor) |
| 18 | LDEN | I | — | | LDEN control (with pull-down resistor)<br>High: LD enabled<br>Low: Power save |

| Pin No. | Symbol | I/O | Pin voltage [V] | Equivalent circuit | Description |
|---|---|---|---|---|---|
| 19 | OUT1 | O | — |  | Laser driving output 1 |
| 20 | Vcc_LDR | — | 4.5 to 6.0 | | Supply voltage for output stage |
| 21 | OUT2 | O | — | | Laser driving output 2 |
| 22 | VIOPMON | O | — |  | Monitor output |
| 23 | GND_LD | — | — |  | Output stage GND |
| 24 | Vcc_LDB | — | 5 to 9 | | Supply voltage for blue-violet LD |
| 25 | OUTBD | O | — | | Laser driving output (for BD) |
| 26 | IINR | I | — |  | Current setting R |

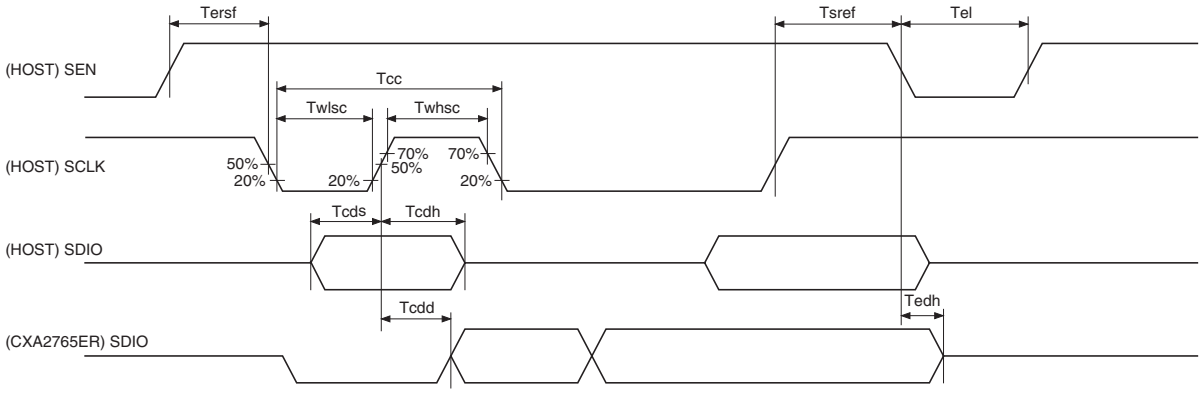
| Pin No. | Symbol | I/O | Pin voltage [V] | Equivalent circuit | Description |
|---|---|---|---|---|---|
| 27 | IIN2 | I | — |  | Current setting 2 |
| 28 | IIN3 | I | — | | Current setting 3 |
| 29 | IIN4 | I | — | | Current setting 4 |
| 30 | IIN5 | I | — |  | Current setting 5 |
| 31 | GND1 | — | — | — | Input signal block and bias block GND |
| 32 | IR | — | 1.25 |  | Reference current setting resistor connection<br>(Connect to GND through 22kΩ.) |

## Electrical Characteristics

(Vcc = Vcc_LDR = 5V, Vcc_LDB = 8V, Ta = 25℃)

| TEST No. | Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **<Current Consumption>** | | | | | | | |
| 1 | Current consumption 1 (LDOFF) | Icc1 | 1.2 | 2.1 | 3.0 | mA | LDEN = Low or LDM = 00 |
| 2 | Current consumption 2 (CD, DVD_STANDBY) | Icc2 | 5 | 12 | 19 | mA | LDEN = High and LDM = 01 or 02<br>IINR, 2, 3, 4, 5 = 0<br>RDIS = OSCEN = OUTEN2, 3, 4, 5 = Disable |
| 3 | Current consumption 3 (CD, DVD_Read) | Icc3 | 21 | 31 | 41 | mA | RDIS, OSCEN = Enable<br>OUT1 or OUT2 = 40mA,<br>modulation amplitude = 20mAp-p<br>Current consumption excluding the OUT1 and OUT2 pin current. |
| 4 | Current consumption 4 (CD, DVD_Write) | Icc4 | 26 | 38 | 50 | mA | RDIS, OUTEN2, OUTEN3 = Enable (IOUTR, IOUT2, IOUT3)<br>IOUTR = 40mA (Duty = 100%)<br>IOUT2 = 240mA (Duty = 25%)<br>IOUT3 = 120mA (Duty = 50%)<br>Current consumption excluding the OUT1 and OUT2 pin current.<br> |
| 5 | Current consumption 5 (BD_STANDBY) | Icc5 | 7 | 10 | 13 | mA | LDEN = High and LDM = 03<br>IINR, 2, 3, 4, 5 = 0<br>RDIS = OSCEN = OUTEN2, 3, 4, 5 = Disable |
| 6 | Current consumption 6 (BD_Read) | Icc6 | 14 | 20 | 26 | mA | RDIS, OSCEN = Enable<br>OUTBD = 40mA,<br>modulation amplitude = 20mAp-p<br>Current consumption excluding the OUTBD pin current. |
| 7 | Current consumption 7 (BD_Write) | Icc7 | 16 | 23 | 30 | mA | RDIS, OUTEN2, OUTEN3 = Enable (IOUTR, IOUT2, IOUT3)<br>IOUTR = 40mA (Duty = 100%)<br>IOUT2 = 60mA (Duty = 25%)<br>IOUT3 = 30mA (Duty = 50%)<br>Current consumption excluding the OUTBD pin current.<br> |

| TEST No. | Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **<Serial Interface AC Characteristics>** | | | | | | | |
| 8 | SCLK operating range | Fser | — | — | 20 | MHz | |
| 9 | SCLK “H” pulse width | Twhsc | 13 | — | — | ns | |
| 10 | SCLK “L” pulse width | Twlsc | 13 | — | — | ns | |
| 11 | SEN “L” time | Tel | 26 | — | — | ns | |
| 12 | SEN rising edge to the first SCLK falling edge | Tersf | 15 | — | — | ns | |
| 13 | SDIO set up time | Tcds | 15 | — | — | ns | |
| 14 | SDIO hold time | Tcdh | 15 | — | — | ns | |
| 15 | Last SCLK rising edge to SEN falling edge | Tsref | 1/Fser | — | — | s | |
| 16 | SCLK cycle time1 | Tcc | 50 | — | — | ns | |
| 17 | SDIO output delay | Tcdd | — | — | 15 | ns | |
| 18 | SDIO output hold time | Tedh | — | 5.1 | — | ns | |




**Serial Interface Timing**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **<CMOS Logic Input>** | | | | | | | |
| 19 | Input voltage High level | VSH | 2.1 | — | 3.6 | V | Pins 2, 4, 6, 8, 11, 12 and 15 to 18 |
| 20 | Input voltage Low level | VSL | 0 | — | 0.6 | V | Pins 2, 4, 6, 8, 11, 12 and 15 to 18 |
| 21 | Input current 1 (High level) | ISH1 | 51 | 72 | 120 | μA | Pins 16 to 18 (VSH = 3.6V) |
| 22 | Input current 1 (Low level) | ISL1 | –10 | — | 10 | μA | Pins 16 to 18 (VSL = 0V) |
| 23 | Input current 2 | IS2 | –10 | — | 10 | μA | Pins 2, 4, 6, 8, 11 |
| 24 | Input current 3 (High level) | ISH3 | –24 | –14 | –9 | μA | Pin 12 (VSH = 3.6V) |
| 25 | Input current 3 (Low level) | ISL3 | –84 | –50 | –35 | μA | Pin 12 (VSL = 0V) |
| **<CMOS Logic Output>** | | | | | | | |
| 26 | Output voltage High level | VOSH | 2.8 | — | 3.3 | V | Pin 15 (IOH = 3mA) |
| 27 | Output voltage Low level | VOSL | 0 | — | 0.4 | V | Pin 15 (IOL = 3mA) |
| 28 | VD3 voltage variance | VVD3 | 3.1 | — | 3.5 | V | Pin 14 |
| **<Differential Input>** | | | | | | | |
| 29 | Input voltage range | VDR | 0 | — | 3 | V | Pins 2 to 11 |
| 30 | Differential input amplitude | VDTH | 0.2 | — | 1 | V | Pins 2 to 11 |
| 31 | Input current | ID | –10 | — | 10 | μA | Pins 2 to 11 |

| TEST No. | Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **<LD Driver DC Characteristics>** | | | | | | | |
| 32 | Total maximum driving current (CD, DVD) | IMAX | 800 | — | — | mA | OUT1, 2 = 3.5V |
| 33 | IINR CH maximum driving current (CD, DVD) | IMAXR | 180 | — | — | mA | OUT1, 2 = 3.5V |
| 34 | IIN2 CH maximum driving current (CD, DVD) | IMAX2 | 400 | — | — | mA | OUT1, 2 = 3.5V |
| 35 | IIN3 CH maximum driving current (CD, DVD) | IMAX3 | 300 | — | — | mA | OUT1, 2 = 3.5V |
| 36 | IIN4 CH maximum driving current (CD, DVD) | IMAX4 | 150 | — | — | mA | OUT1, 2 = 3.5V |
| 37 | IIN5 CH maximum driving current (CD, DVD) | IMAX5 | 180 | — | — | mA | OUT1, 2 = 3.5V |
| 38 | Total minimum driving current (CD, DVD) | IMIN | — | — | 10 | mA | OUT1, 2 = 3.5V |
| 39 | IINR CH minimum driving current (CD, DVD) | IMINR | — | — | 4.3 | mA | OUT1, 2 = 3.5V |
| 40 | IIN2 CH minimum driving current (CD, DVD) | IMIN2 | — | — | 5.1 | mA | OUT1, 2 = 3.5V |
| 41 | IIN3 CH minimum driving current (CD, DVD) | IMIN3 | — | — | 4.0 | mA | OUT1, 2 = 3.5V |
| 42 | IIN4 CH minimum driving current (CD, DVD) | IMIN4 | — | — | 1.9 | mA | OUT1, 2 = 3.5V |
| 43 | IIN5 CH minimum driving current (CD, DVD) | IMIN5 | — | — | 3.6 | mA | OUT1, 2 = 3.5V |
| 44 | Total maximum driving current (BD) | IMAX_BD | 450 | — | — | mA | OUTBD = 1.5V |
| 45 | IINR CH maximum driving current (BD) | IMAXR_BD | 150 | — | — | mA | OUTBD = 1.5V |
| 46 | IIN2 CH maximum driving current (BD) | IMAX2_BD | 200 | — | — | mA | OUTBD = 1.5V |
| 47 | IIN3 CH maximum driving current (BD) | IMAX3_BD | 150 | — | — | mA | OUTBD = 1.5V |
| 48 | IIN4 CH maximum driving current (BD) | IMAX4_BD | 50 | — | — | mA | OUTBD = 1.5V |
| 49 | IIN5 CH maximum driving current (BD) | IMAX5_BD | 150 | — | — | mA | OUTBD = 1.5V |
| 50 | Total minimum driving current (BD) | IMIN_BD | –1.1 | — | 6.0 | mA | OUTBD = 1.5V |
| 51 | IINR CH minimum driving current (BD) | IMINR_BD | 0 | — | 2.3 | mA | OUTBD = 1.5V, measured value – ($I_{OP}$ when RDIS = OUTENx = Disable) |
| 52 | IIN2 CH minimum driving current (BD) | IMIN2_BD | 0 | — | 2.7 | mA | OUTBD = 1.5V, measured value – ($I_{OP}$ when RDIS = OUTENx = Disable) |
| 53 | IIN3 CH minimum driving current (BD) | IMIN3_BD | 0 | — | 2.0 | mA | OUTBD = 1.5V, measured value – ($I_{OP}$ when RDIS = OUTENx = Disable) |
| 54 | IIN4 CH minimum driving current (BD) | IMIN4_BD | 0 | — | 0.7 | mA | OUTBD = 1.5V, measured value – ($I_{OP}$ when RDIS = OUTENx = Disable) |
| 55 | IIN5 CH minimum driving current (BD) | IMIN5_BD | 0 | — | 3.0 | mA | OUTBD = 1.5V, measured value – ($I_{OP}$ when RDIS = OUTENx = Disable) |
| 56 | Read noise 1 (CD, DVD) | RNS1 | — | 0.31 | — | nA/$\sqrt{Hz}$ | OUT1, 2 = 40mA, OSCEN = Disable 16.5MHz noise, HFMP = 32d |

| TEST No. | Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| 57 | Read noise 2 (CD, DVD) | RNS2 | — | 0.42 | — | nA/$\sqrt{Hz}$ | OUT1, 2 = 40mA, OSCEN = Enable (20mAp-p, 350MHz) 16.5MHz noise, HFMP = 32d |
| 58 | Write noise 1 (CD, DVD) | WNS1 | — | 2.4 | — | nA/$\sqrt{Hz}$ | RDIS, OUTEN2 = Enable IOUTR = 40mA (Duty = 100%) IOUT2 = 40mA (Duty = 50%) 16.5MHz noise |
| 59 | Write noise 2 (CD, DVD) | WNS2 | — | 2.8 | — | nA/$\sqrt{Hz}$ | OUTEN5, OUTEN2 = Enable IOUT5 = 40mA (Duty = 100%) IOUT2 = 40mA (Duty = 50%) 16.5MHz noise |
| 60 | Read noise 1 (BD) | RNS1_BD | — | 0.46 | — | nA/$\sqrt{Hz}$ | OUTBD = 40mA, OSCEN = Disable 16.5MHz noise, HFMP = 79d |
| 61 | Read noise 2 (BD) | RNS2_BD | — | 0.47 | — | nA/$\sqrt{Hz}$ | OUTBD = 40mA, OSCEN = Enable (20mAp-p, 350MHz) 16.5MHz noise, HFMP = 79d |
| 62 | Write noise 1 (BD) | WNS1_BD | — | 1.8 | — | nA/$\sqrt{Hz}$ | RDIS, OUTEN2 = Enable IOUTR = 40mA (Duty = 100%) IOUT2 = 40mA (Duty = 50%) 16.5MHz noise |
| 63 | Write noise 2 (BD) | WNS2_BD | — | 2.4 | — | nA/$\sqrt{Hz}$ | OUTEN5, OUTEN2 = Enable IOUT5 = 40mA (Duty = 100%) IOUT2 = 40mA (Duty = 50%) 16.5MHz noise |
| **<LD Driver AC Characteristics>** | | | | | | | |
| 64 | Rise time (CD, DVD resistance load) | Tr | — | 0.5 | — | ns | 50mA to 100mA pulse, settling 10% to 90% Load = 5Ω//10pF |
| 65 | Fall time (CD, DVD resistance load) | Tf | — | 0.5 | — | ns | |
| 66 | Overshoot (CD, DVD resistance load) | OVS+ | — | 10 | — | % | |
| 67 | Propagation delay 1 (CD, DVD resistance load) | DELAY1 | — | 5.6 | — | ns | OUT1/2 output ON response time from OUTEN2/3/4/5 differential input |
| 68 | Propagation delay 2 (CD, DVD resistance load) | DELAY2 | — | 5.3 | — | ns | OUT1/2 output OFF response time from OUTEN2/3/4/5 differential input |
| 69 | Rise time (BD resistance load) | Tr_BD | — | 0.5 | — | ns | 50mA to 100mA pulse, settling 10% to 90% Load = 10Ω//10pF |
| 70 | Fall time (BD resistance load) | Tf_BD | — | 0.5 | — | ns | |
| 71 | Overshoot (BD resistance load) | OVS+_BD | — | 10 | — | % | |
| 72 | Propagation delay 1 (BD resistance load) | DELAY1_BD | — | 4.6 | — | ns | OUTBD output ON response time from OUTEN2/3/4/5 differential input |
| 73 | Propagation delay 2 (BD resistance load) | DELAY2_BD | — | 4 | — | ns | OUTBD output OFF response time from OUTEN2/3/4/5 differential input |

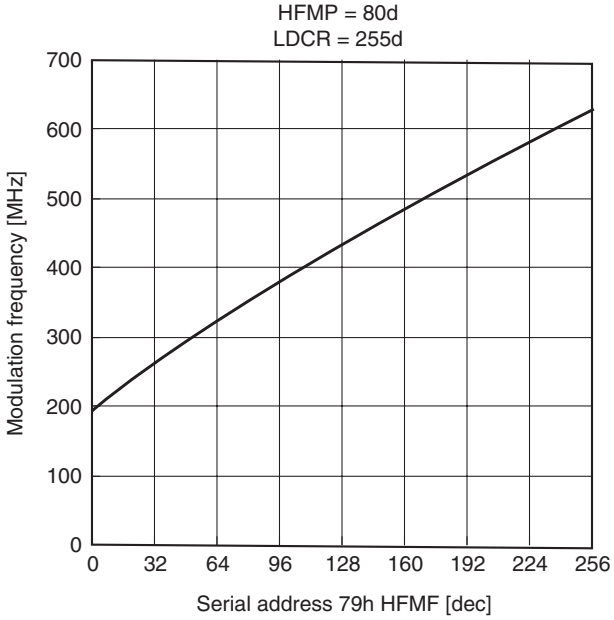
| TEST No. | Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **<I/O Characteristics>** | | | | | | | |
| 74 | Input resistance R, 5 | ZINR | 518 | 740 | 962 | Ω | IINR/5 input resistance |
| 75 | Input resistance 2, 3, 4 | ZINW | 700 | 1000 | 1300 | Ω | IIN2/3/4 input resistance |
| 76 | Input current R, 2, 3, 4, 5 | IIN | 0 | — | 1 | mA | IINR/2/3/4/5 input current |
| 77 | I/O band R | FBANDR | — | 370 | — | kHz | IINR = 200μA input |
| 78 | I/O band 2, 3, 4, 5 | FBANDW | — | 2.35 | — | MHz | IIN2/3/4/5 = 400μA input |
| 79 | I/O gain R (CD, DVD) | GAINR | 235 | 262 | 289 | A/A | Gain from IINR input to OUT1/2 output (IINR = 100μA to 200μA, OUT1/2 = 2.5V) |
| 80 | I/O gain 5 (CD, DVD) | GAIN5 | 235 | 262 | 289 | A/A | Gain from IIN5 input to OUT1/2 output (IIN5 = 100μA to 200μA, OUT1/2 = 2.5V) |
| 81 | I/O gain 2 (CD, DVD) | GAIN2 | 504 | 560 | 616 | A/A | Gain from IIN2 input to OUT1/2 output (IINR = 200μA, IIN2 = 100μA to 200μA, OUT1/2 = 2.5V) |
| 82 | I/O gain 3 (CD, DVD) | GAIN3 | 405 | 450 | 495 | A/A | Gain from IIN3 input to OUT1/2 output (IINR = 200μA, IIN3 = 100μA to 200μA, OUT1/2 = 2.5V) |
| 83 | I/O gain 4 (CD, DVD) | GAIN4 | 202 | 225 | 248 | A/A | Gain from IIN4 input to OUT1/2 output (IINR = 200μA, IIN4 = 100μA to 200μA, OUT1/2 = 2.5V) |
| 84 | I/O linearity 2, 3, 4 (CD, DVD) | LINE | –3 | — | 3 | % | Fix IINR to 200μA, and measure the offset at IIN2/3/4 = 600μA in reference to IIN2/3/4 = 100μA to 200μA, respectively. OUT1/2 = 2.5V |
| 85 | I/O gain ratio 1 (CD, DVD) | GaRa1 | 0.9 | 1 | 1.1 | — | IIN5/IINR gain ratio |
| 86 | I/O gain ratio 2 (CD, DVD) | GaRa2 | 0.72 | 0.8 | 0.88 | — | IIN3/IIN2 gain ratio |
| 87 | I/O gain ratio 3 (CD, DVD) | GaRa3 | 0.36 | 0.4 | 0.44 | — | IIN4/IIN2 gain ratio |
| 88 | I/O gain R (BD) | GAINR_BD | 180 | 200 | 221 | A/A | Gain from IINR input to OUTBD output (IINR = 100μA to 200μA, OUTBD = 2.5V) |
| 89 | I/O gain 5 (BD) | GAIN5_BD | 180 | 200 | 221 | A/A | Gain from IIN5 input to OUTBD output (IIN5 = 100μA to 200μA, OUTBD = 2.5V) |
| 90 | I/O gain 2 (BD) | GAIN2_BD | 238 | 265 | 291 | A/A | Gain from IIN2 input to OUTBD output (IINR = 200μA, IIN2 = 100μA to 200μA, OUTBD = 2.5V) |
| 91 | I/O gain 3 (BD) | GAIN3_BD | 180 | 200 | 220 | A/A | Gain from IIN3 input to OUTBD output (IINR = 200μA, IIN3 = 100μA to 200μA, OUTBD = 2.5V) |
| 92 | I/O gain 4 (BD) | GAIN4_BD | 59 | 66 | 73 | A/A | Gain from IIN4 input to OUTBD output (IINR = 200μA, IIN4 = 100μA to 200μA, OUTBD = 2.5V) |
| 93 | I/O linearity 2, 3, 4 (BD) | LINE_BD | –3 | — | 3 | % | Fix IINR to 200μA, and measure the offset at IIN2/3/4 = 600μA in reference to IIN2/3/4 = 100μA to 200μA, respectively. OUTBD = 2.5V |
| 94 | I/O gain ratio 1 (BD) | GaRa1_BD | 0.91 | 1 | 1.12 | — | IIN5/IINR gain ratio |
| 95 | I/O gain ratio 2 (BD) | GaRa2_BD | 0.67 | 0.75 | 0.83 | — | IIN3/IIN2 gain ratio |
| 96 | I/O gain ratio 3 (BD) | GaRa3_BD | 0.22 | 0.25 | 0.28 | — | IIN4/IIN2 gain ratio |

| TEST No. | Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| **<High-frequency Modulation (HFM)>** | | | | | | | |
| 97 | Frequency variable range | VARIF | 200 | — | 600 | MHz | HFMF = 0 to 255dec |
| 98 | Frequency variance | FREQ | –10 | — | 10 | % | HFMF = 80dec (@350MHz) |
| 99 | Frequency temperature coefficient | TFREQ | — | –0.0035 | — | %/°C | HFMF = 80dec (@350MHz) |
| 100 | Amplitude setting range (CD, DVD) | VARIA | 0 | — | 100 | mAp-p | HFMF = 80dec (@350MHz), HFMP = 0 to 255dec Load = 5Ω |
| 101 | Amplitude setting range (BD) | VARIA_BD | 0 | — | 70 | mAp-p | HFMF = 80dec (@350MHz), HFMP = 31 to 255dec, LDCR2 = 00 Load = 10Ω |
| 102 | OSCEN response time – ON | OSCRES1 | — | — | 11 | ns | OSCEN Disable → Enable |
| 103 | OSCEN response time – OFF | OSCRES2 | — | — | 11 | ns | OSCEN Enable → Disable |
| **<LDOFF>** | | | | | | | |
| 104 | LDOFF response time | LDOFFRES | — | — | 10 | ns | Time for the output current to fall to 10% when LDEN is changed from High to Low. |
| 105 | Power supply monitor circuit – LDOFF | EMON | 3.1 | 3.5 | — | V | Vcc and Vcc_LDR voltages at which LDOFF results. |
| 106 | Power supply monitor circuit – LDON | EMOFF | — | 3.75 | 4.15 | V | Vcc and Vcc_LDR voltages at which LDOFF is canceled. |
| **<VIMON>** | | | | | | | |
| 107 | VOP monitor upper limit (CD, DVD) | VmoMax | 4.90 | 5 | 5.05 | V | VIMON = 001 VIMON voltage when 5V is applied to OUT1/2. |
| 108 | VOP monitor lower limit (CD, DVD) | VmoMin | 0 | 0.7 | 1.1 | V | VIMON = 001 VIMON voltage when 0V is applied to OUT1/2. |
| 109 | VOP monitor DC accuracy (CD, DVD) | VmoDC | 3.9 | 4 | 4.1 | V | VIMON = 001 VIMON voltage when 4V is applied to OUT1/2. |
| 110 | VOP monitor pulse accuracy (CD, DVD) | VmoPls | 3.8 | 4 | 4.1 | V | VIMON output voltage when a 3V to 4V, duty 50%, 6ns pulse is input to OUT1/2. (Peak hold accuracy) |
| 111 | VOP monitor hold capability (CD, DVD) | VmoHd | –72 | –53.5 | –25 | mV/μs | VIMON = 001 |
| 112 | VOP monitor upper limit (BD) | VmoMax_BD | 2.4 | 2.5 | 2.6 | V | VIMON = 001 VIMON voltage when 5V is applied to OUTBD. |
| 113 | VOP monitor lower limit (BD) | VmoMin_BD | 0 | — | 0.15 | V | VIMON = 001 VIMON voltage when 0V is applied to OUTBD. |
| 114 | VOP monitor DC accuracy (BD) | VmoDC_BD | 0.4 | 0.5 | 0.6 | V | VIMON = 001 VIMON voltage when 1V is applied to OUTBD. |
| 115 | VOP monitor pulse accuracy (BD) | VmoPls_BD | 0.4 | 0.5 | 0.7 | V | VIMON output voltage when a 1V to 2V, duty 50%, 6ns pulse is input to OUTBD. (Bottom hold accuracy) |
| 116 | VOP monitor hold capability (BD) | VmoHd_BD | 23 | 54 | 73 | mV/μs | VIMON = 001 |
| 117 | Temperature monitor output voltage | TmoVout | — | 1.34 | — | V | VIMON = 010, Tj = 70°C |
| 118 | Temperature monitor temperature coefficient | Tmotemp | — | 3.5 | — | mV/°C | VIMON = 010 |
| 119 | IOP monitor current efficiency (BD only) | Iratio_BD | 0.914 | 1 | 1.053 | % | VIMON = 100, IMON/IOUTBD current ratio when OUTBD = 40mA. VIOPMON = 2V |

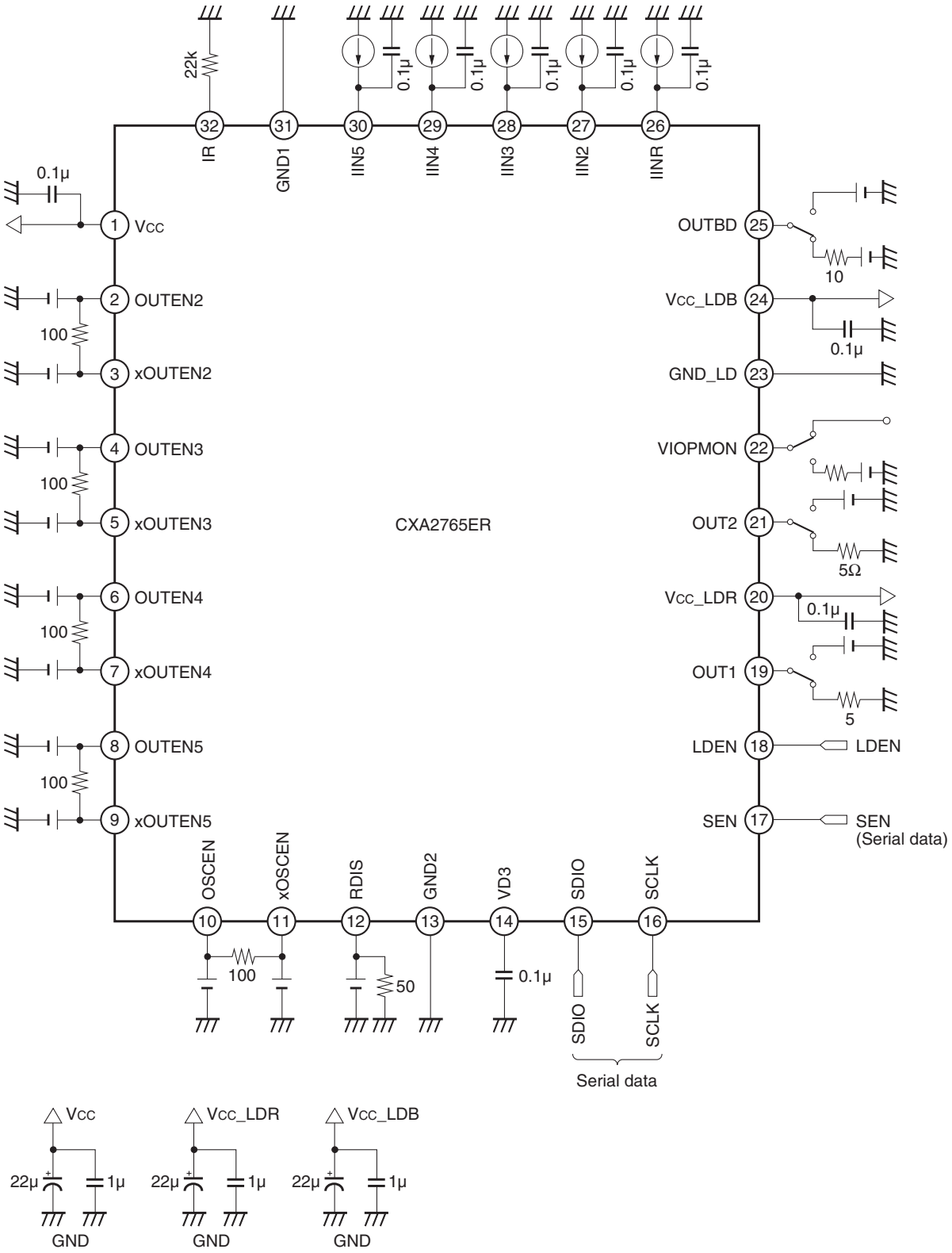
## Example of Representative Characteristics

### ◆ High-frequency Modulation Characteristics

**Control characteristics of HFMF and modulation frequency**



## Electrical Characteristics Measurement Circuit



## Serial Interface

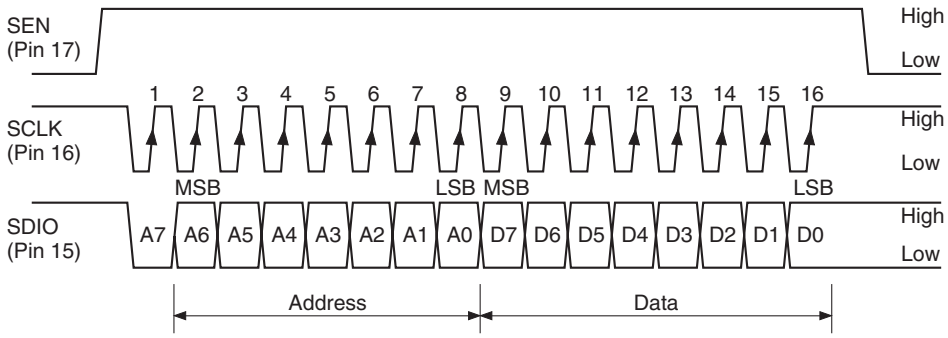
The CXA2765ER performs IC control via the serial interface. The serial interface specifications are shown below.

### Serial Address Bit Definition

| Bit | Bit definition |
|---|---|
| A7 | Read/write select bit<br>0: Serial interface write mode<br>1: Serial interface read mode |
| A6 to 0 | Register address select bit |

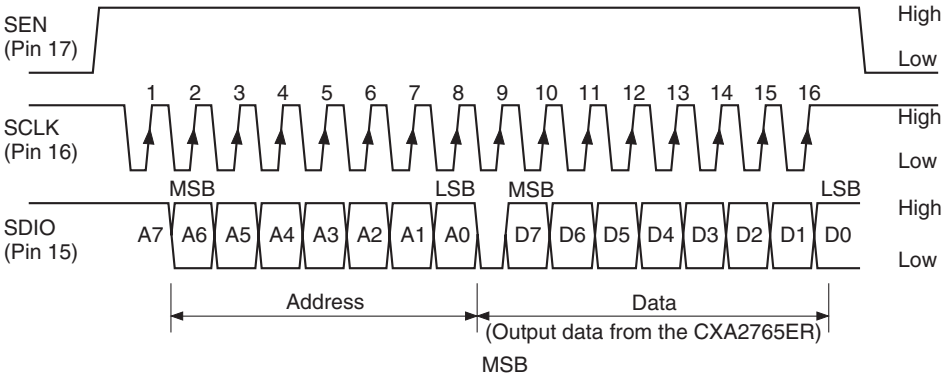
Transmission and reception are performed in 16-bit units consisting of 8 address bits and 8 data bits. Both the address and data are MSB first. In the address, the A[7] bit switches between read and write mode, and the A[6:0] bits are the register address. The read/write timing charts are shown below.

### Timing Chart in Write Mode




The data written in the register is reflected to the various IC internal functions at the rising edge of the 16th (last) SCLK signal.

### Timing Chart in Read Mode




Note) Depending on the flexible PC board condition, when the SDIO line and the SEN line use adjacent wiring, SDIO signal fluctuations may be transmitted to the SEN line and make the control status unstable, with the result that correct data cannot be read and written during serial transfer.

## Address Map

(SDIO/SEN/SCLK)

| Address | Name | Definition |
|---|---|---|
| 78 | MODELDD | LDD status (LDOFF/CD/DVD/BD)<br>Transfer skew check, input logic selection, and power supply monitor circuit control |
| 79 | HFMP | Modulation amplitude setting (CD/DVD: 0 to 100mAp-p, BD: 0 to 70mAp-p) |
| 7A | HFMF | Modulation frequency setting (200MHz to 600MHz) |
| 7B | EMISEL | HFM spectrum diffusion setting, monitor control |
| 7C | LDCR | Output waveform adjustment |
| 7D | CHSEL | Channel control method selection |

## Bit Map

**Serial Address 78h**

| Bit | Symbol | Bit definition |
|---|---|---|
| 7 | — | Don't care |
| 6 | EMVCCDIS | Power supply monitor circuit disable<br>0: Enable<br>1: Disable |
| 5 | SEL_CH5 | CH5 input logic level selection<br>0: Differential input<br>1: Single input |
| 4 | SEL_CH2-4 | CH2 to CH4 input logic level selection<br>0: Differential input<br>1: Single input |
| 3 | SEL_OSC | OSC CH input logic level selection<br>0: Differential input<br>1: Single input |
| 2 | SKEW | Skew check function<br>0: Normal operation<br>1: Transfer skew check mode |
| 1-0 | LDM | LDD output selection<br>00: LDOFF (Power save)<br>01: LD1<br>10: LD2<br>11: BD |

**Serial Address 79h**

| Bit | Symbol | Bit definition | |
|---|---|---|---|
| | | HFM amplitude setting | |
| | | CD/DVD | BD |
| 7-0 | HFMP | Resolution = 0.4mAp-p<br>0d: 0mAp-p<br>to<br>128d: 50mAp-p<br>to<br>255d: 100mAp-p | Resolution = 0.3mAp-p<br>31d: 0mAp-p<br>to<br>128d: 30mAp-p<br>to<br>255d: 70mAp-p |

**Serial Address 7Ah**

| Bit | Symbol | Bit definition |
|---|---|---|
| 7-0 | HFMF | HFM frequency setting<br>0d: 200MHz<br>to<br>255d: 600MHz |

**Serial Address 7Bh**

| Bit | Symbol | Bit definition |
|---|---|---|
| 7-5 | VIMON | V/I monitor output selection<br>000: OFF (monitor circuit power save)<br>001: VOP monitor output in accordance with LDM<br>010: Temperature sensor output<br>011: EMI countermeasure circuit period measurement mode<br>100: IOP output (BD_Read + MOD only)<br>101: MODFDAC measurement mode<br>110: MODADAC measurement mode<br>111: EMI countermeasure circuit spread measurement mode |
| 4 | EMIEN | HFM spectrum diffusion circuit enable<br>0: Disable<br>1: Enable |
| 3-2 | EMIP | HFM spectrum diffusion – modulation frequency<br>00: 0.01% (350MHz conversion = 35kHz)<br>01: 0.02% (350MHz conversion = 70kHz)<br>10: 0.04% (350MHz conversion = 140kHz)<br>11: 0.08% (350MHz conversion = 280kHz) |
| 1-0 | EMIS | HFM spectrum diffusion – diffusion frequency<br>00: 0.2% (350MHz conversion = 0.7MHz)<br>01: 0.4% (350MHz conversion = 1.4MHz)<br>10: 0.8% (350MHz conversion = 2.8MHz)<br>11: 1.6% (350MHz conversion = 5.6MHz) |

**Serial Address 7Ch**

| Bit | Symbol | Bit definition (BD) | Bit definition (DVD/CD) |
|---|---|---|---|
| 7 | LDCR5 | LDD buffer current<br>0: Small current<br>1: Large current (fast waveform) | Ringing adjustment (Tr only)<br>0: Small<br>1: Large (fast waveform) |
| 6 | LDCR4 | LDD buffer signal current ratio<br>0: 1:4<br>1: 2:4 (fast waveform) | — |
| 5 | LDCR3 | LDD buffer bias current<br>0: Small bias current<br>1: Large bias current (fast waveform) | — |
| 4-3 | LDCR2 | Snubber 2 (both Tr and Tf)<br>00: Slow waveform<br>01: ↓<br>10: ↓<br>11: Fast waveform | — |
| 2-0 | LDCR1 | Snubber 1 (Tr only)<br>000: Slow waveform<br>001: ↓<br>010: ↓<br>011: ↓<br>100: ↓<br>101: ↓<br>110: ↓<br>111: Fast waveform | Overshoot adjustment (Tr only)<br>000: Small<br>001: ↓<br>010: ↓<br>011: ↓<br>100: ↓<br>101: ↓<br>110: ↓<br>111: Large (fast waveform) |

**Serial Address 7Dh**

| Bit | Symbol | Bit definition |
|---|---|---|
| 7 | — | — |
| 6 | CH5EN | Channel 5 register control<br>0: OFF<br>1: ON |
| 5 | CH4EN | Channel 4 register control<br>0: OFF<br>1: ON |
| 4 | CH3EN | Channel 3 register control<br>0: OFF<br>1: ON |
| 3 | CH2EN | Channel 2 register control<br>0: OFF<br>1: ON |
| 2 | REN | Read channel register control<br>0: OFF<br>1: ON |
| 1 | OSCEN | Channel OSC register control<br>0: OFF<br>1: ON |
| 0 | CH_CONT | Channel control method selection<br>0: Normal (pin control)<br>1: Register control mode |

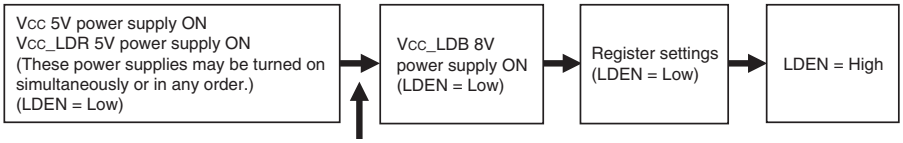
Note) When data is not written to address 78h to 7Dh after power-on, the registers at addresses 78h to 7Dh are undetermined.

## Description of Operation

### 1. Power-on and power-off sequences

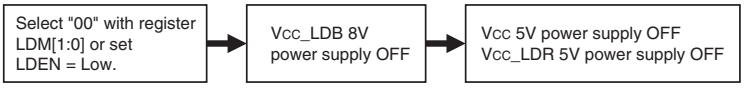
The following sequences are recommended to protect the laser when turning the power on and off.

#### Power-on sequence




Turn on the VCC_LDB 8V power supply after the VCC 5V and VCC_LDR 5V power supplies have risen to 1V or more. The IC control status is unstable when the VCC 5V and VCC_LDR 5V power supplies are less than 1V, so if the VCC_LDB 8V power supply rises to 7V or more in this condition, current of approximately 10mA may flow to the laser.

#### Power-off sequence




When LDEN is Low, current does not flow to the laser for any power-off sequence, but the above sequence is recommended.

Note) When the power is forcibly turned off during laser emission, current of the set level or more may flow to the laser.
The conditions for current of the set level or more flowing to the laser are $V_{CC} < 3/5 \times V_{CC_LDR}$ and $V_{CC_LDR} \geq 2V$ (shaded area in the figure below).
To avoid problems, VCC_LDR should be turned off first, or VCC and VCC_LDR should be turned off at approximately the same time.
In addition, current of the set level or more does not flow to the laser regardless of the VCC_LDB 8V power-off order.

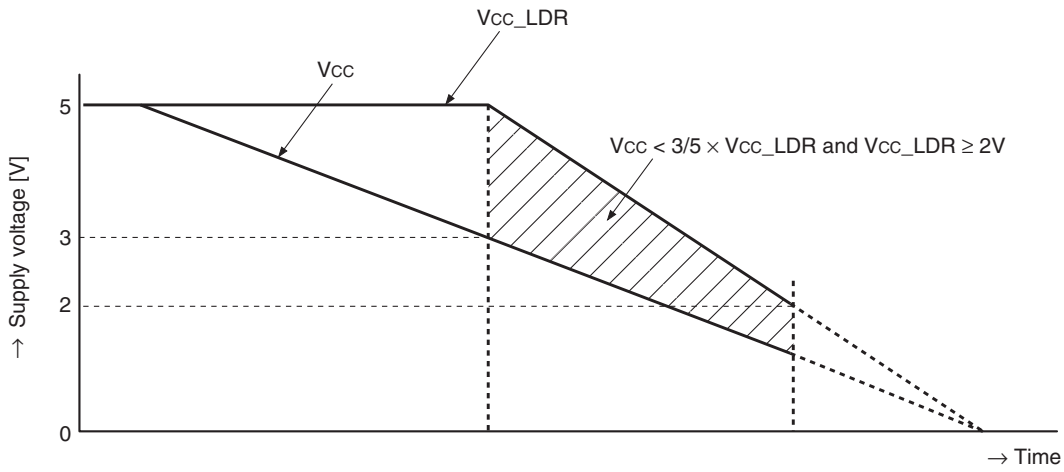



**Fig. 1. VCC and VCC_LDR Power-off**

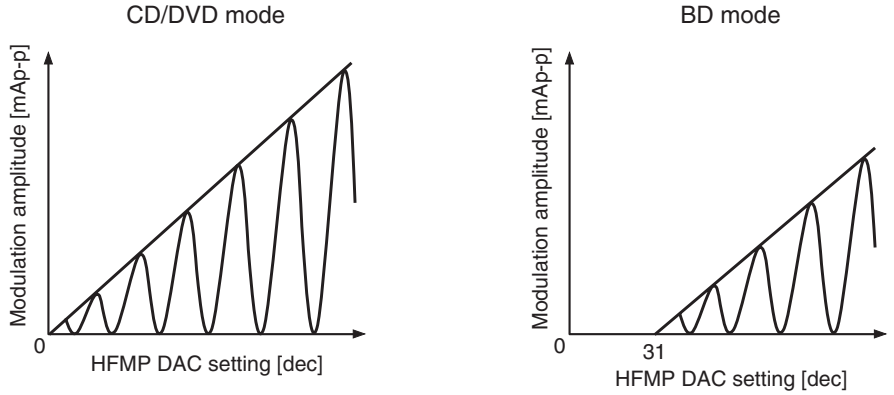
### 2. LD driving current setting

The currents controlled by the current setting pins IINR, IIN2, IIN3, IIN4 and IIN5 are output from the OUT1, OUT2 and OUTBD pins.
The output driving currents from the OUT pins can be set independently for IINR, IIN2, IIN3, IIN4 and IIN5 by RDIS, OUTEN and xOUTEN.
Note that output switching for OUT1 (Pin 19), OUT2 (Pin 21) and OUTBD (Pin 25) is performed by serial address 78h bit[1:0] LDM.

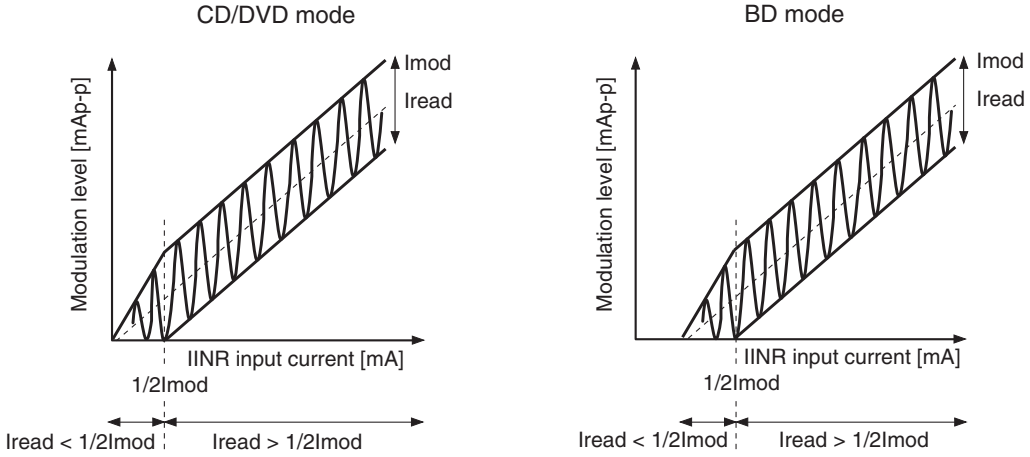
### 3. Modulator circuit

Output modulation is turned on and off by the OSCEN and xOSCEN pins.
The modulation frequency can be varied by serial address 7Ah bit[7:0] HFMF, and the modulation amplitude can be varied by serial address 79h bit[7:0] HFMP.

**Modulation Amplitude Setting**




**Modulation Level Adjustment**




### 4. IR pin

The IR pin external resistor should be fixed to 22kΩ.
The IR pin aims to reduce variance in the modulation frequency that depends on the internal resistance, and is designed based on fixed resistance of 22kΩ.

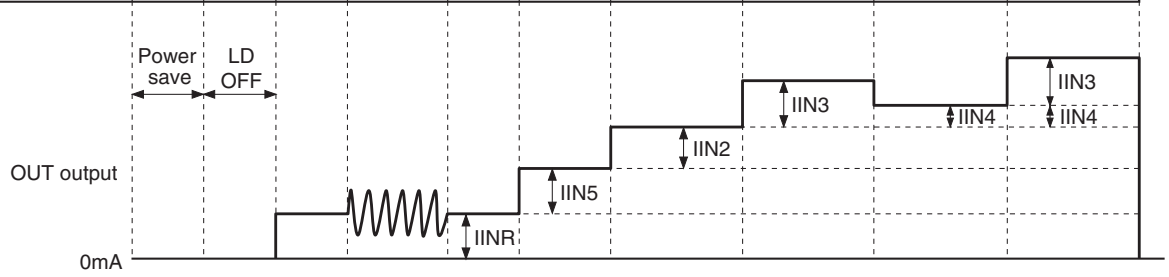
## Description of Functions

### Logic Tables

#### Output control (Differential input)

(X: Don't care)

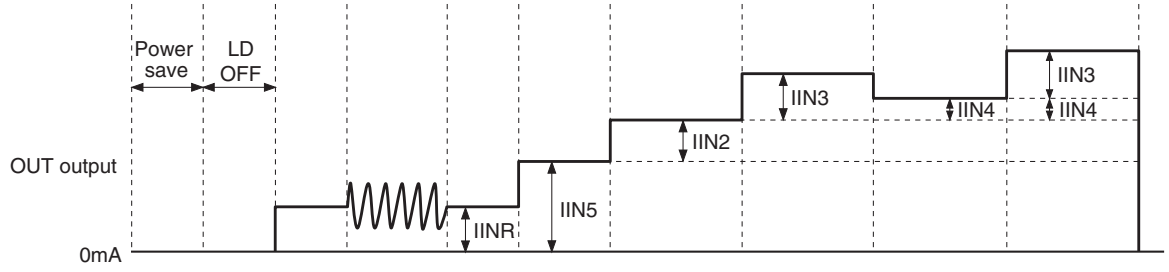
| LDEN | L | H | H | H | H | H | H | H | H | H |
|---|---|---|---|---|---|---|---|---|---|---|
| RDIS | X | H | L | L | L | L | L | L | L | L |
| OUTEN2 | X | L | L | L | L | L | H | H | H | H |
| OUTEN3 | X | L | L | L | L | L | L | H | L | H |
| OUTEN4 | X | L | L | L | L | L | L | L | H | H |
| OUTEN5 | X | L | L | L | L | H | H | H | H | H |
| XOSCEN | X | H | H | L | H | H | H | H | H | H |
| OUT output (OUT1/OUT2 /OUTBD) | PS | OFF | IINR | IINR (Modulation ON) | IINR | IINR + IIN5 | IINR + IIN5 + IIN2 | IINR + IIN5 + IIN2 + IIN3 | IINR + IIN5 + IIN2 + IIN4 | IINR + IIN5 + IIN2 + IIN3 + IIN4 |




#### Output control (Single input)

(X: Don't care)

| LDEN | L | H | H | H | H | H | H | H | H | H |
|---|---|---|---|---|---|---|---|---|---|---|
| RDIS | X | H | L | L | L | H | H | H | H | H |
| OUTEN2 | X | L | L | L | L | L | H | H | H | H |
| OUTEN3 | X | L | L | L | L | L | L | H | L | H |
| OUTEN4 | X | L | L | L | L | L | L | L | H | H |
| OUTEN5 | X | L | X | X | X | H | H | H | H | H |
| XOSCEN | X | H | H | L | H | H | H | H | H | H |
| OUT output (OUT1/OUT2 /OUTBD) | PS | OFF | IINR | IINR (Modulation ON) | IINR | IIN5 | IIN5 + IIN2 | IIN5 + IIN2 + IIN3 | IIN5 + IIN2 + IIN4 | IIN5 + IIN2 + IIN3 + IIN4 |




Note) When serial address 78h bit[5] SEL_CH5 is set High (single input), the IINR channel and the IIN5 channel cannot be added to prevent glitches.

## Modulation control

DVD/CD mode

(X: Don't care)

| LDEN | L | H | H | H | H | H | H | H | H |
|---|---|---|---|---|---|---|---|---|---|
| RDIS | X | L | L | H | H | H | H | L | H |
| OUTEN2 | X | H | L | H | L | L | L | H | H |
| OUTEN3 | X | H | L | L | H | L | L | L | H |
| OUTEN4 | X | H | L | L | L | H | L | L | L |
| OUTEN5 | X | H | L | L | L | L | H | L | L |
| XOSCEN | X | H | L | L | L | L | L | L | L |
| Modulation output (OUT1/OUT2) | PS | Modulation OFF | Modulation ON (IINR) | Modulation ON (IIN2) | Modulation ON (IIN3) | Modulation ON (IIN4) | Modulation ON (IIN5) | Modulation ON (IINR, IIN2) | Modulation ON (IIN2, IIN3) |

Note) 1. Modulation control is independent of the data timing signal.
2. Modulation is not output from the OUT pin without the input current to IINR.

BD mode

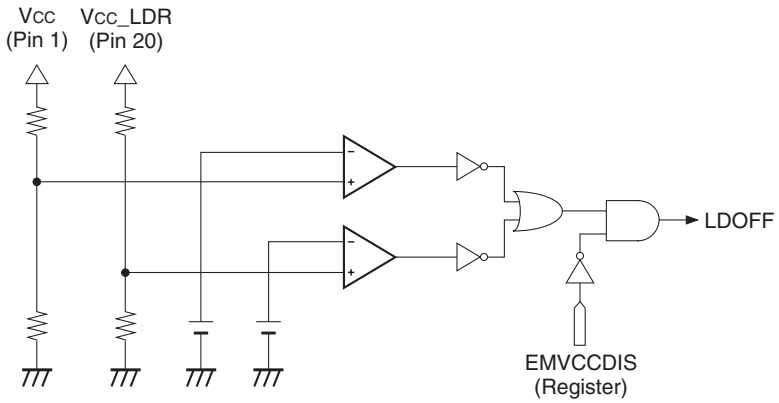
(X: Don't care)

| LDEN | L | H | H |
|---|---|---|---|
| RDIS | X | X | L |
| OUTEN2 | X | X | X |
| OUTEN3 | X | X | X |
| OUTEN4 | X | X | X |
| OUTEN5 | X | X | X |
| XOSCEN | X | H | L |
| Modulation output (OUTBD) | PS | Modulation OFF | Modulation ON (IINR) |

Note) Modulation is not output from the OUT pin without the input current to IINR.

### Power Supply Monitor Circuit

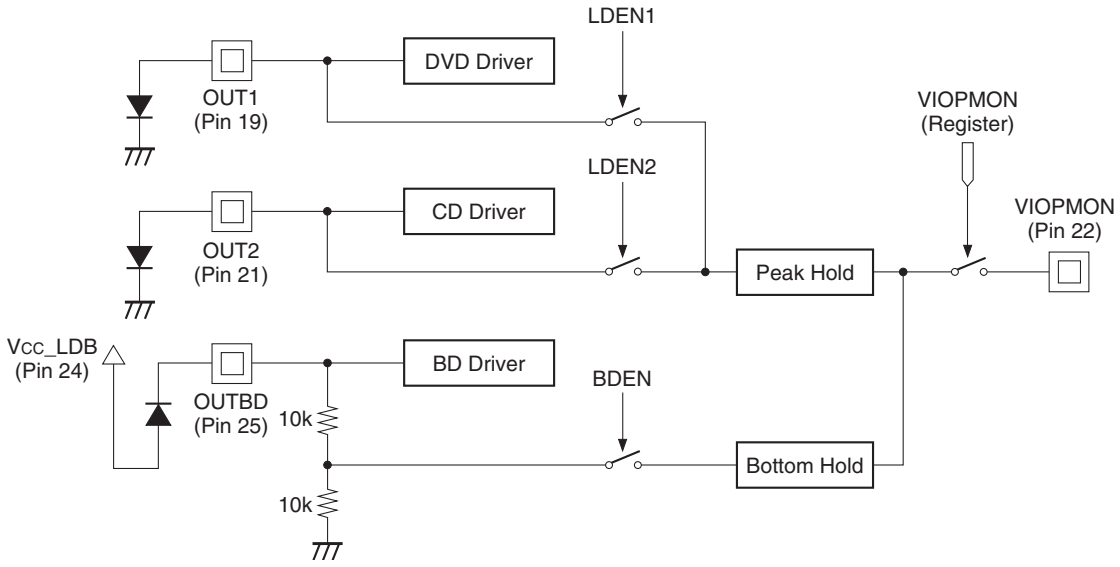
The CXA2765ER has a built-in power supply monitor circuit to ensure safe laser emission. This function monitors the two supply voltages VCC (Pin 1) and VCC_LDR (Pin 20). See the “Electrical Characteristics” table for the respective threshold values. When this function detects that either of these power supplies has dropped, it outputs the LDOFF (power save) signal and turns off the laser driving current.
The power supply monitor circuit function can be enabled or disabled by serial address 78h bit[6] EMVCCDIS.




**Power Supply Monitor Circuit Block Diagram**

### VOP Monitor Function

The VOP voltage at the laser end can be monitored.
When serial address 7Bh bit[7:5] are set to “001”, the peak hold voltage (CD/DVD) or the bottom hold voltage (BD) is output from VIOPMON (Pin 22).

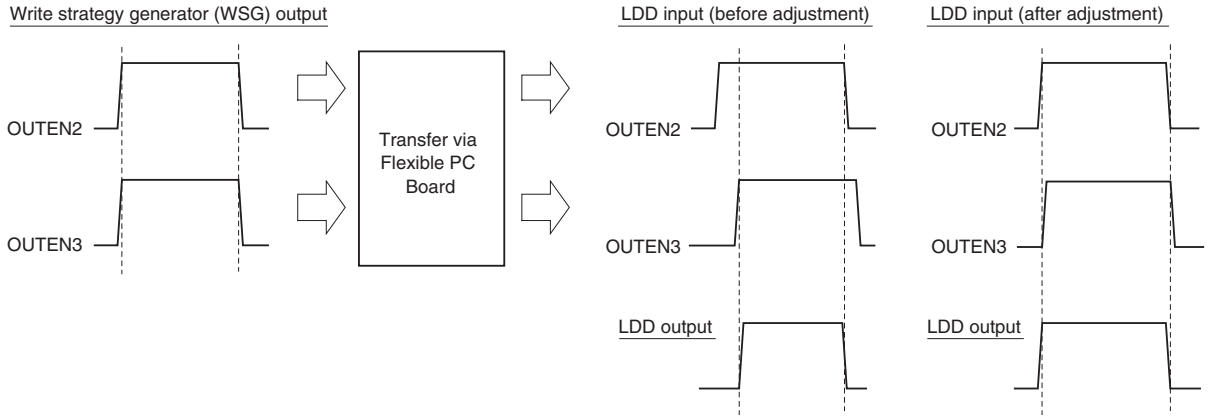


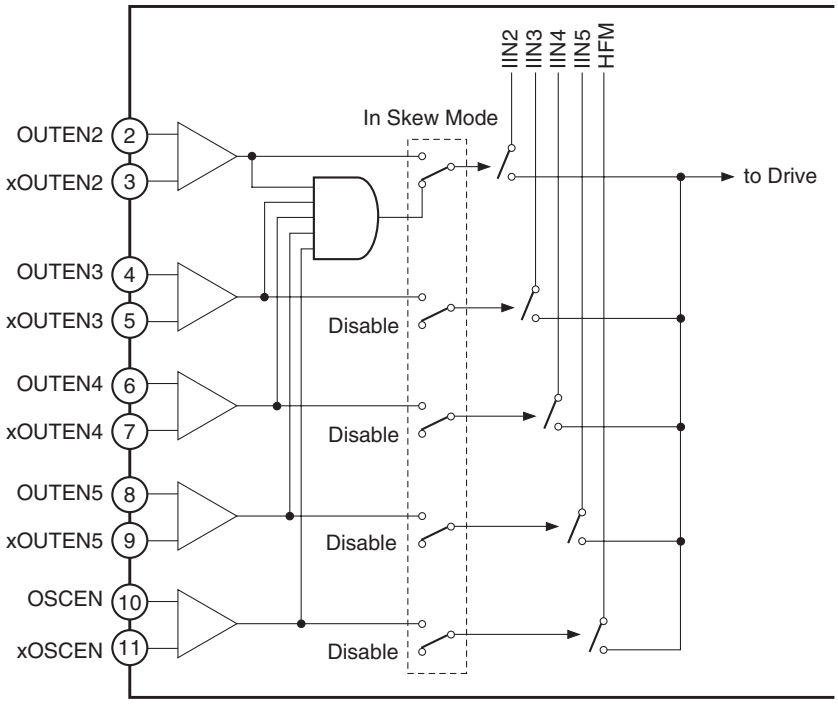

**VOP Monitor Block Diagram**

### Skew Check Function

Normal mode or skew check mode can be selected by serial address 78h bit[2] SKEW.
The skew check mode is the function that detects the timing offset of recording signals input to the CXA2765ER that occurs between channels due to the effects of the flexible PC board and other factors.
It can detect the timing offset between a total of 5 channels (4 write channels and one OSC channel).

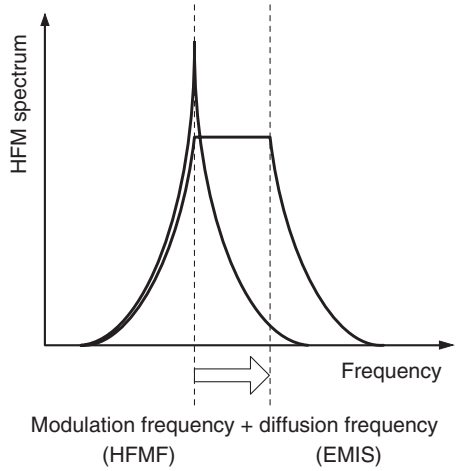
The AND of the recording signals for each channel input to the CXA2765ER is output from the IIN2 channel path. The AND is output, so when the timing is offset between channels, the recording waveform pulse width narrows and the output recording power drops. Adjust the timing of the recording signal for each channel to maximize the output recording power.



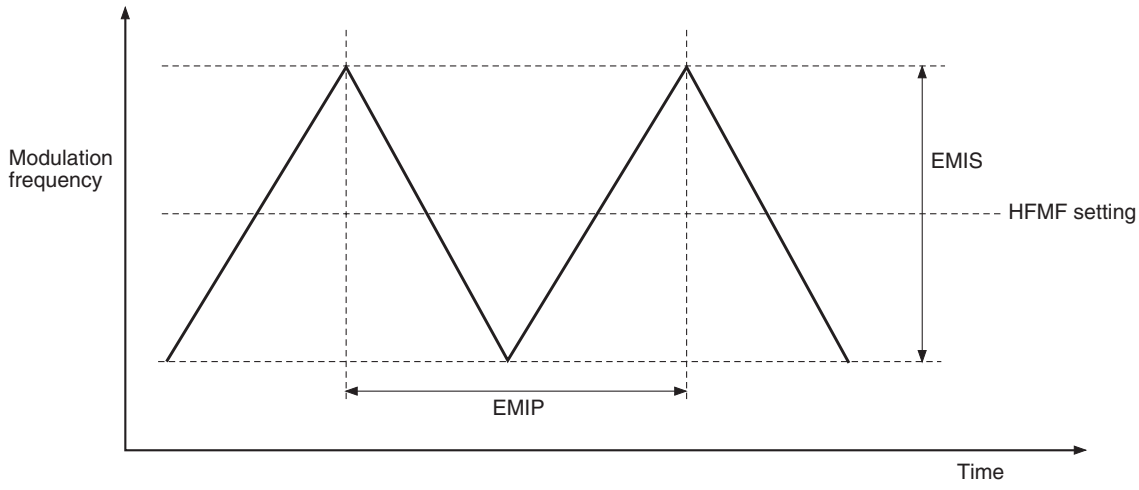
### HFM Spectrum Diffusion Function

The HFM spectrum diffusion function is enabled by selecting “1” at Bit4 EMIEN of serial address 7Bh, and the HFM frequency is diffused as shown in the figure below.



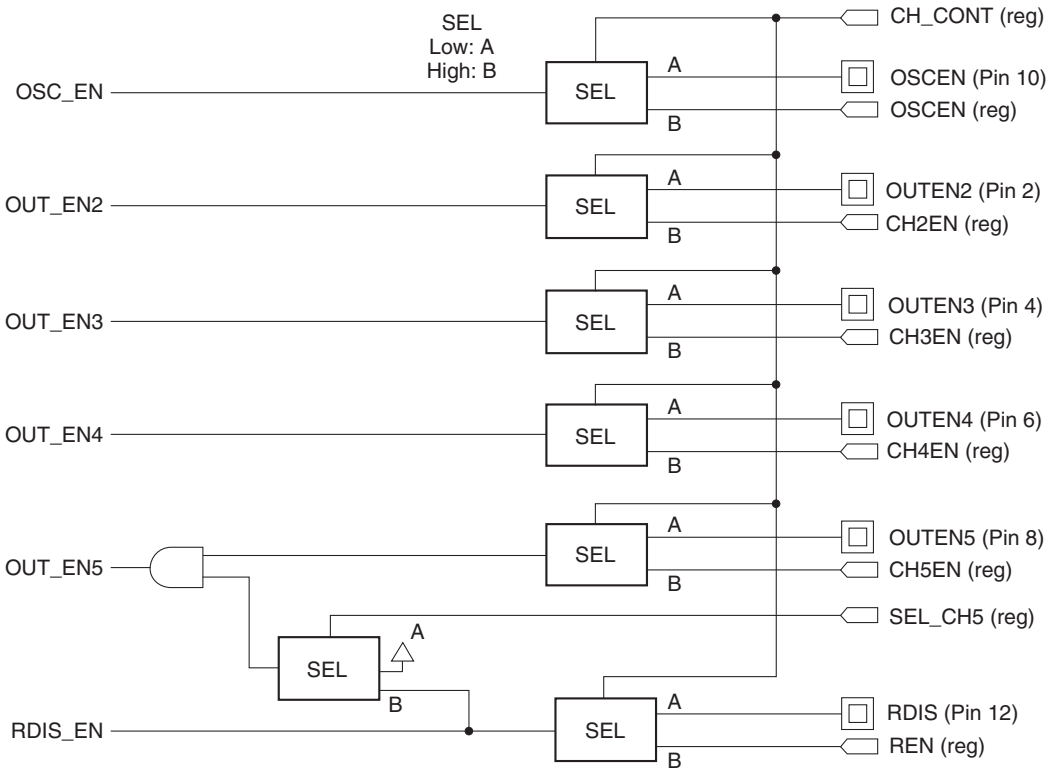

### HFM Spectrum Diffusion Frequency Measurement

When serial address 7Bh bit[7:5] are set to “011” or “111”, the HFM spectrum diffusion modulation frequency (EMIP) and diffusion frequency (EMIS) can be measured at VIOPMON (Pin 22).



### Channel control

Pin control or bit[6:1] register control can be selected by serial address 7Dh bit[0] CH_CONT.



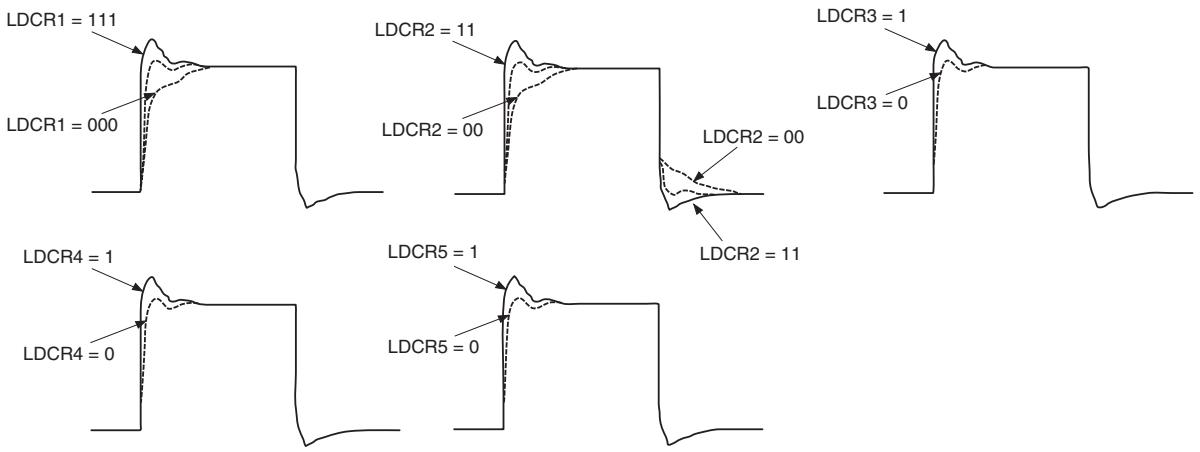

### Read channel and cool channel glitch countermeasures in single input mode

When serial address 78h bit[5] SEL_CH5 is set High (single input), a timing signal which has had glitch countermeasures applied by the read channel and cool channel is output on OUT_EN5. Therefore, the read channel and cool channel cannot be added in single input mode. When set Low (differential input (LVDS)), the cool channel can be added to the read channel to generate the write power.

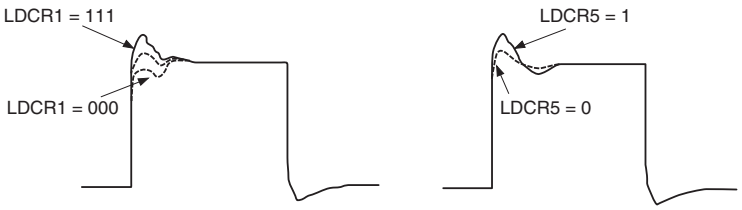
### Changes in the output waveform characteristics by the register settings

The waveform characteristics (rise time (tr), fall time (tf), overshoot (OVS+), undershoot (OVS–)) of the output LD driving current change greatly according to the LDD, the LD and the LD load (in the mounted condition) connected to each output pin OUT1 (Pin 19), OUT2 (Pin 21) and OUTBD (Pin 25).
The CXA2765ER can adjust the LDD output waveform characteristics by the register settings. These controls are performed by Serial Address 7Ch. However, in BD mode the current consumption of the 5V block increases as the LDCR5, LDCR4 and LDCR3 settings are increased (faster waveform). In addition, take care in LDCR2 setting because it affects high-frequency modulation amplitude. Modulation amplitude will be larger as LDCR2 setting changes from 00 to 11. In DVD/CD mode the current consumption of the 5 V block increases as the LDCR5 and LDCR1 settings are increased (faster waveform).

**<BD waveform adjustment>**




**<DVD/CD waveform adjustment>**



## Notes on Operation

- Make the wiring as short as possible between the output OUT pins (Pins 19, 21 and 25) and the laser diode, and between the $V_{CC}$_LDR pin and the external decoupling capacitor. As the wiring length increases, the effects of the wiring inductance cause the output waveform overshoot and undershoot to increase.
- The $V_{CC}$_LDR pin's external decoupling capacitance ground can be grounded to the GND grounding the load from the OUT pin. This reverses the phase of the drive waveform at the OUT and $V_{CC}$_LDR and moves in the direction that suppresses overshoots and undershoots.
- Place the external resistor connected to the IR pin as close to the IC as possible.
  As the wiring length between the IR pin and the external resistor increases, external disturbance easily enters the reference current generated by the IR pin, and may cause noise to worsen or other problems. In addition, when capacitance is applied to the IR pin, the phase margin with the internal circuits is reduced and oscillation easily occurs.
- Temperature guarantee
  Thermal resistance ($\theta$j-a) when the CXA2765ER is mounted on PWB varies according to the set (PWB) and because it is difficult to predict along with the tendency for higher power for power consumption ($P_O$), the following points should be considered when using.

  Use in a range that the junction temperature (Tj) does not exceed 150℃ (Tjmax). Also, Use with the thermal resistance ($\theta$j-a) of the PWB mounting lowered so that power consumption (PO) is below allowable power dissipation (PD).

  It is possible to lower the thermal resistance ($\theta$j-a) when mounted on PWB by widening the GND region with the set PWB or releasing heat to the set chassis, etc.

  Find the thermal resistance ($\theta$j-a) when mounted on PWB and power consumption ($P_O$) using the following method.

  $P_O = (I_{CC} \times V_{CC}) - (I_{OP} \times V_{OP})$: DVD/CD mode
  $P_O = (I_{CC} \times V_{CC}) + (I_{OP} \times V_{OP})$: BD mode

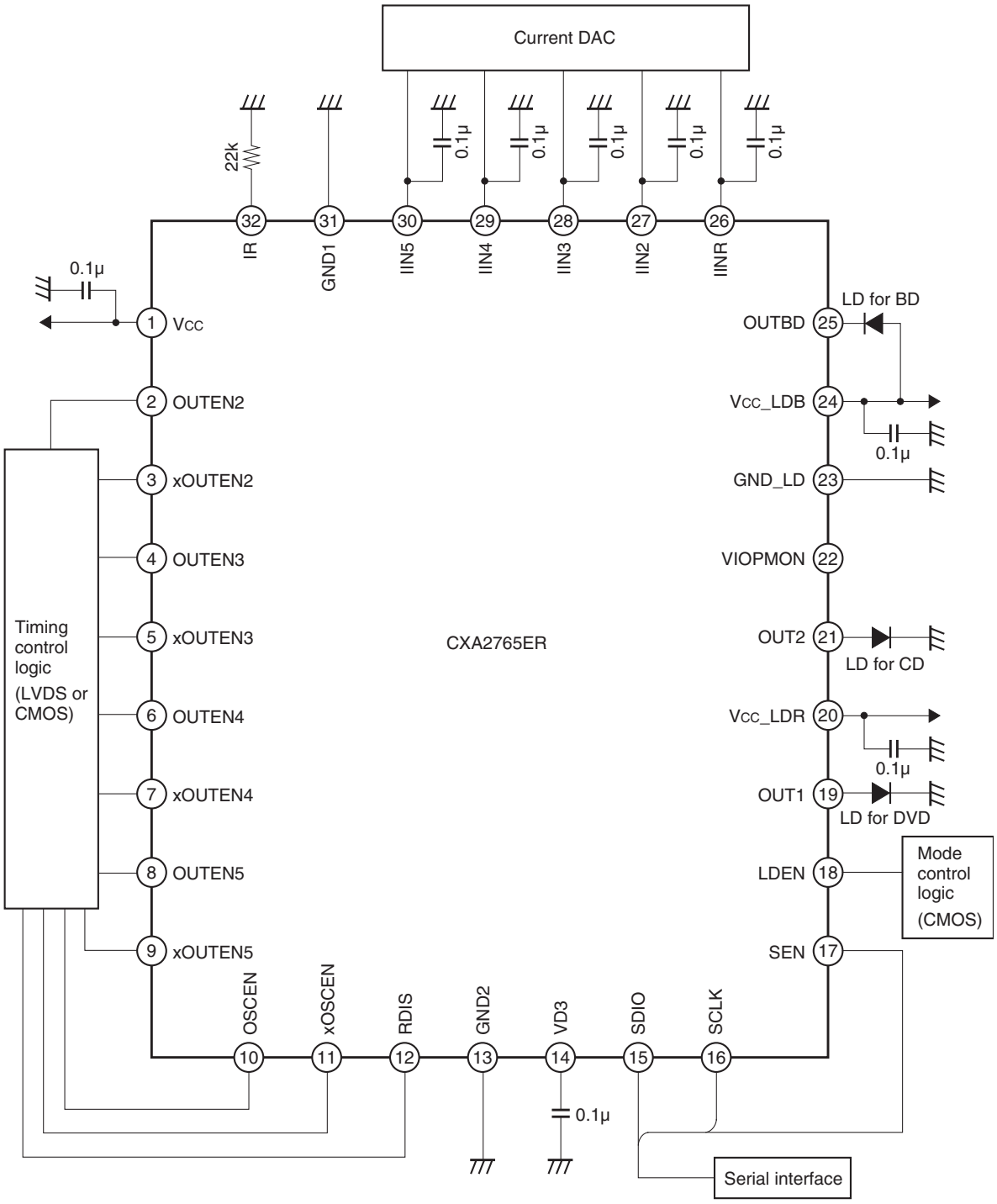
  $I_{CC}$: IC current consumption when operating (including $I_{OP}$ in DVD/CD mode)
  $I_{OP}$: Output drive current flowed from the OUT pin to the laser diode
  $V_{OP}$: Operating voltage of the laser diode

  **Thermal resistance ($\theta$j-a) when mounted on PWB**

  The thermal resistance ($\theta$c-a) is easily obtained by measuring the package surface temperature using a thermo couple or a radiation thermometer.
  In order to improve the precision of measurement, it is desired to calculate by the following formula.
  $\Delta$Package surface temperature when $I_{OP}$ is variable/$\Delta P_O$
  Assume the thermal resistance ($\theta$j-c) to be approximately 2℃/W.

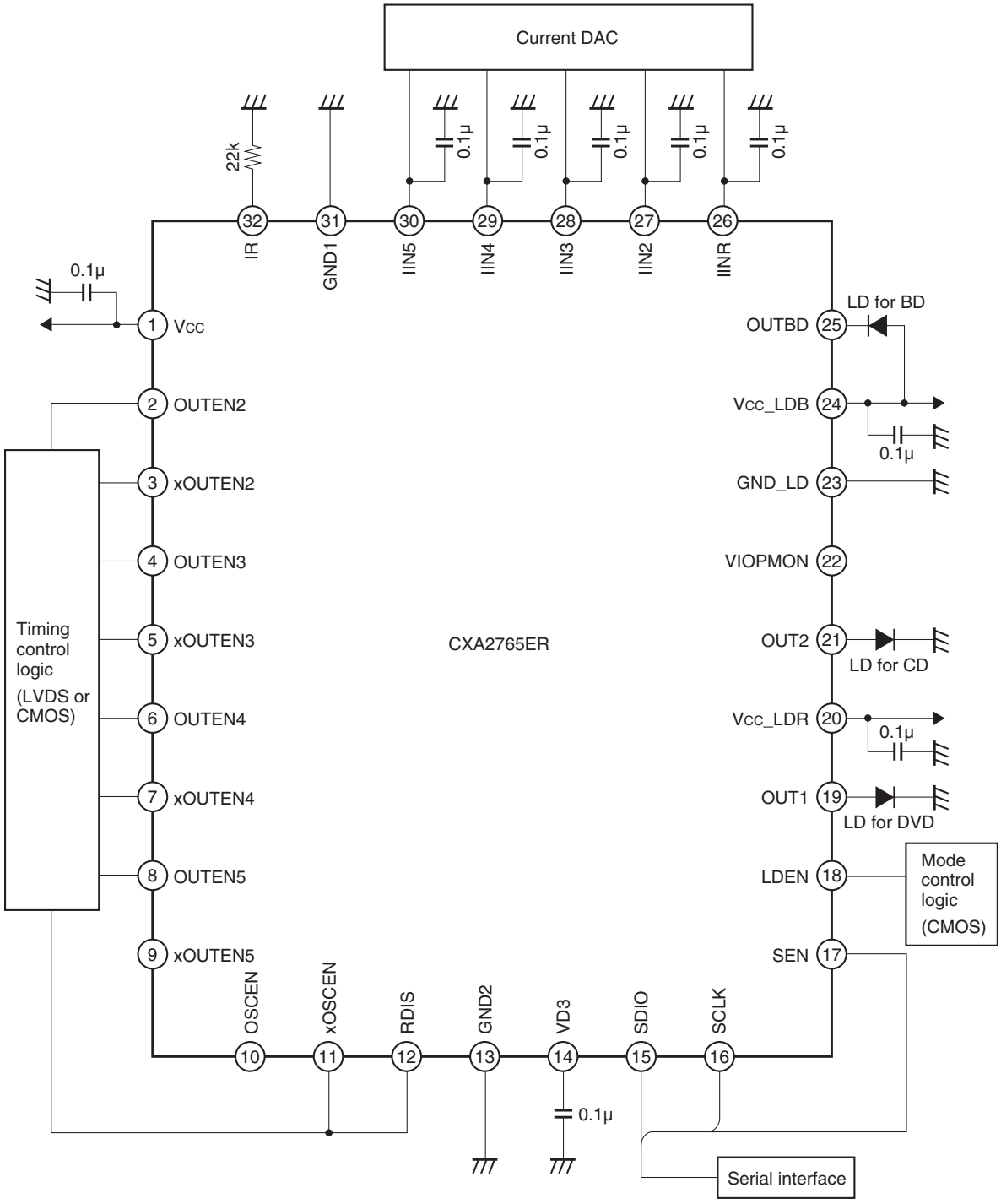
  - Thermal resistance ($\theta$j-a) is
    $\theta$j-a = $\theta$j-c + $\theta$c-a
  - Allowable power dissipation ($P_D$) $\geq P_O$ [W]
    $P_D$ = (150℃ – Ambient temperature)/$\theta$j-a

## Application Circuit 1




Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

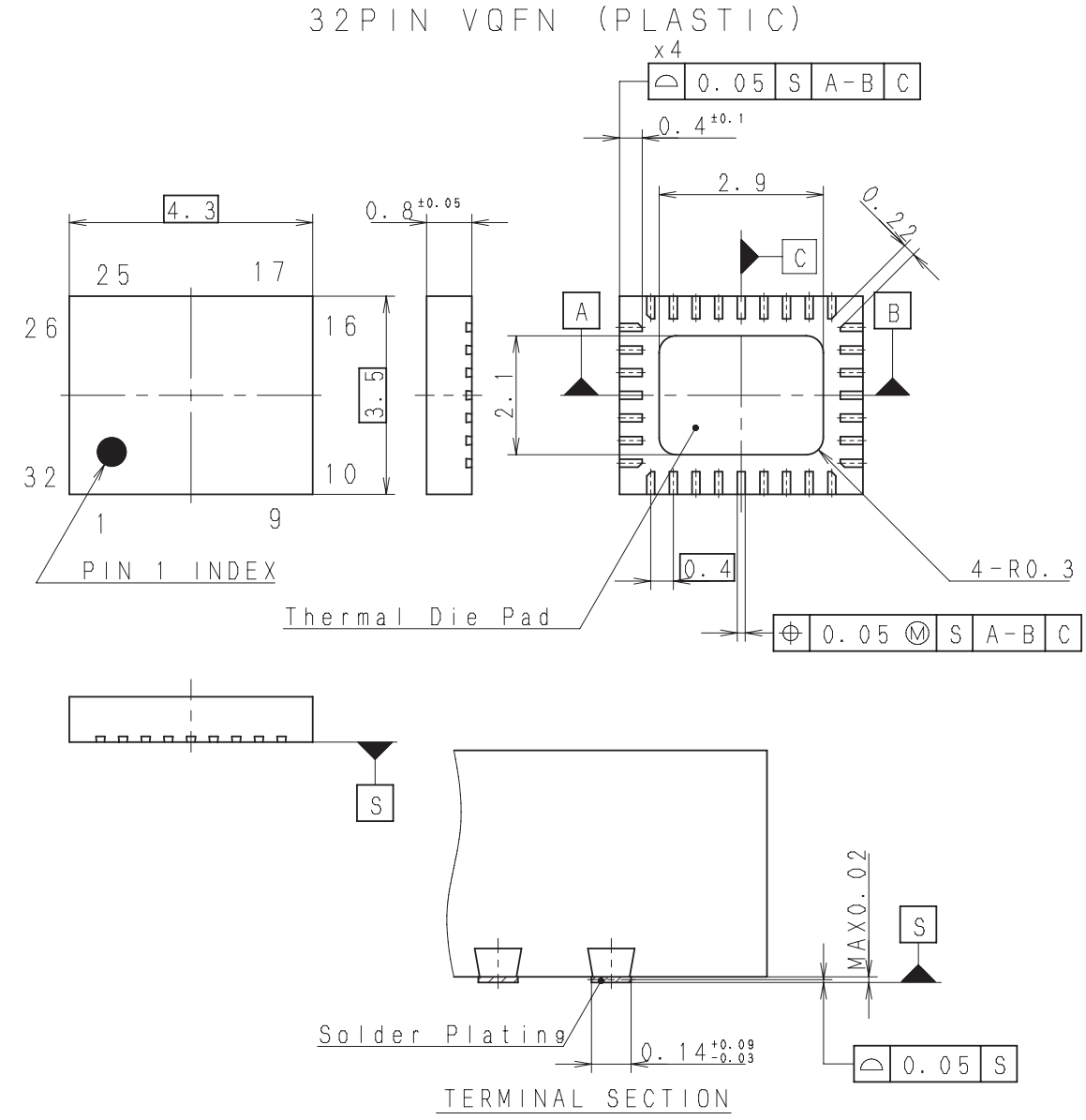
## Application Circuit 2




Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

## Package Outline

(Unit: mm)




Note:Cutting burr of lead are 0.05mm MAX.

| | |
|---|---|
| SONY CODE | VQFN-32P-09 |
| JEITA CODE | ———— |
| JEDEC CODE | ———— |

AP-4000-32030S Rev. 0

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 0.04g |

**LEAD PLATING SPECIFICATIONS**

| ITEM | SPEC. |
|---|---|
| LEAD MATERIAL | COPPER ALLOY |
| SOLDER COMPOSITION | Sn-Bi Bi:1-4wt% |
| PLATING THICKNESS | 5-18μm |