IF Digitizing Subsystem

Data Sheet

AD9864

FEATURES

10 MHz to 300 MHz input frequency
6.8 kHz to 270 kHz output signal bandwidth
7.5 dB single sideband noise figure (SSB NF)
–7.0 dBm input third-order intercept (IIP3)
AGC free range up to –34 dBm
12 dB continuous AGC range
16 dB front-end attenuator
Baseband I/Q 16-bit (or 24-bit) serial digital output
LO and sampling clock synthesizers
Programmable decimation factor, output format, AGC, and synthesizer settings
370 Ω input impedance
2.7 V to 3.6 V supply voltage
Low current consumption: 17 mA
48-lead LFCSP package

APPLICATIONS

Multimode narrow-band radio products
Analog/digital UHF/VHF FDMA receivers
TETRA, APCO25, GSM/EDGE
Portable and mobile radio products
SATCOM terminals

GENERAL DESCRIPTION

The AD9864[1] is a general-purpose IF subsystem that digitizes a low level, 10 MHz to 300 MHz IF input with a signal bandwidth ranging from 6.8 kHz to 270 kHz. The signal chain of the AD9864 consists of a low noise amplifier (LNA), a mixer, a band-pass Σ-Δ analog-to-digital converter (ADC), and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit gives the AD9864 12 dB of continuous gain adjustment. Auxiliary blocks include both clock and local oscillator (LO) synthesizers.

The high dynamic range of the AD9864 and inherent antialiasing provided by the band-pass Σ-Δ converter allow the device to cope with blocking signals up to 95 dB stronger than the desired signal. This attribute often reduces the cost of a radio by reducing IF filtering requirements. Also, it enables multimode radios of varying channel bandwidths, allowing the IF filter to be specified for the largest channel bandwidth.

The SPI port programs numerous parameters of the AD9864, allowing the device to be optimized for any given application. Programmable parameters include synthesizer divide ratios, AGC attenuation and attack/decay time, received signal strength level, decimation factor, output data format, 16 dB attenuator, and the selected bias currents.

The AD9864 is available in a 48-lead LFCSP package and operates from a single 2.7 V to 3.6 V supply. The total power consumption is typically 56 mW and a power-down mode is provided via serial interfacing.

FUNCTIONAL BLOCK DIAGRAM

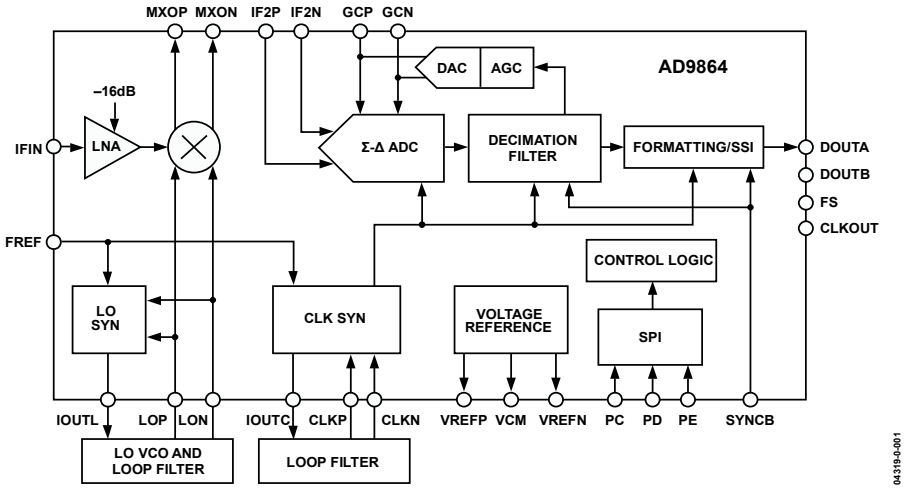

Figure 1.

[1] Protected by U.S. Patent No. 5,969,657; other patents pending.

Rev. A **Document Feedback**

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Evaluation Board for AD9864 and AD9874

DOCUMENTATION

Data Sheet

- AD9864: IF Digitizing Subsystem Data Sheet

TOOLS AND SIMULATIONS

- AD9864 IBIS Models

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC
- MS-2735: Maximizing the Dynamic Range of Software-Defined Radio

DESIGN RESOURCES

- AD9864 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Digital Specifications ... 5
Absolute Maximum Ratings ... 6
Thermal Resistance ... 6
ESD Caution ... 6
Pin Configuration and Functional Descriptions ... 7
Typical Performance Characteristics ... 9
Terminology ... 14
Serial Peripheral Interface (SPI) ... 15
Theory of Operation ... 17
Introduction ... 17
Serial Port Interface (SPI) ... 18
Power-On Reset ... 19
Synchronous Serial Interface (SSI) ... 19
SSI Control Registers ... 21
Synchronization Using SYNCB ... 24
Interfacing to DSPs ... 24
Power Control ... 24
LO Synthesizer ... 25
Clock Synthesizer ... 26
IF LNA/Mixer ... 28
Band-Pass Σ-Δ ADC ... 29
Decimation Filter ... 32
Variable Gain Amplifier Operation with Automatic Gain Control ... 33
Applications Considerations ... 38
External Passive Component Requirements ... 40
Applications ... 40
Layout Example, Evaluation Board, and Software ... 45
SPI Initialization Example ... 45
Device SPI Initialization ... 46
Outline Dimensions ... 47
Ordering Guide ... 47

REVISION HISTORY

2/16—Rev. 0 to Rev. A

Changes to Figure 2 ... 7
Changes to Typical Performance Characteristics Section ... 9
Changes to Figure 19 ... 11
Changes to Table 6 ... 16
Changed General Description Section to Introduction Section ... 17
Changes to Serial Port Interface (SPI) Section ... 18
Added Figure 31; Renumbered Sequentially ... 19
Added Power-On Reset Section ... 19
Deleted Table 9; Renumbered Sequentially ... 19
Added SSI Control Registers Section and Table 8 to Table 13 ... 21
Changes to Synchronization Using SYNCB Section and Figure 38 ... 24
Changes to Clock Synthesizer Section ... 26
Changes to Band-Pass Σ-Δ ADC Section and Table 20 ... 30
Changes to Table 21 ... 31
Changes to Variable Gain Control Section ... 34
Deleted Table 17 ... 34
Added Figure 64 ... 36
Changes to Figure 72 ... 40
Changes to Layout Example, Evaluation Board, and Software Section ... 45
Added Figure 77 and SPI Initialization Example Section ... 45
Added Device SPI Initialization Section and Table 24 ... 46
Updated Outline Dimensions ... 47
Changes to Ordering Guide ... 47

8/03—Revision 0: Initial Version

SPECIFICATIONS

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 2.7 V to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted. Standard operating mode: VGA at minimum attenuation setting, synthesizers in normal (not fast acquire) mode, decimation factor = 900, 16-bit digital output, and 10 pF load on SSI output pins.

Table 1.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
SYSTEM DYNAMIC PERFORMANCE[1]						
SSB Noise Figure at Minimum VGA Attenuation[2, 3]	Full	IV		7.5	9.5	dB
SSB Noise Figure at Maximum VGA Attenuation[2, 3]	Full	IV		13		dB
Dynamic Range with AGC Enabled[2, 3]	Full	IV	91	95		dB
IF Input Clip Point at Maximum VGA Attenuation[3]	Full	IV	−20	−19		dBm
IF Input Clip Point at Minimum VGA Attenuation[3]	Full	IV	−32	−31		dBm
Input Third-Order Intercept (IIP3)	Full	IV	−12	−7.0		dBm
Gain Variation over Temperature	Full	IV		0.7	2	dB
LNA + MIXER						
Maximum RF and LO Frequency Range	Full	IV	300	500		MHz
LNA Input Impedance	25°C	V		370‖1.4		Ω‖pF
Mixer LO Input Resistance	25°C	V		1		kΩ
LO SYNTHESIZER						
LO Input Frequency	Full	IV	7.75		300	MHz
LO Input Amplitude	Full	IV	0.3		2.0	V p-p
FREF Frequency (for Sinusoidal Input Only)	Full	IV	8		26	MHz
FREF Input Amplitude	Full	IV	0.3		3	V p-p
FREF Slew Rate	Full	IV	7.5			V/µs
Minimum Charge Pump Current at 5 V[4]	Full	VI		0.67		mA
Maximum Charge Pump Current at 5 V[4]	Full	VI		5.3		mA
Charge Pump Output Compliance[5]	Full	VI	0.4		VDDP − 0.4	V
Synthesizer Resolution	Full	IV	6.25			kHz
CLOCK SYNTHESIZER						
CLK Input Frequency	Full	IV	13		26	MHz
CLK Input Amplitude	Full	IV	0.3		VDDC	V p-p
Minimum Charge Pump Output Current[4]	Full	VI		0.67		mA
Maximum Charge Pump Output Current[4]	Full	VI		5.3		mA
Charge Pump Output Compliance[5]	Full	VI	0.4		VDDQ − 0.4	V
Synthesizer Resolution	Full	VI	2.2			kHz
Σ-Δ ADC						
Resolution	Full	IV	16		24	Bits
Clock Frequency (f_{CLK})	Full	IV	13		26	MHz
Center Frequency	Full	V		$f_{CLK}/8$		MHz
Pass-Band Gain Variation	Full	IV			1.0	dB
Alias Attenuation	Full	IV	80			dB
GAIN CONTROL						
Programmable Gain Step	Full	V		16		dB
AGC Gain Range	Full	V		12		dB
GCP Output Resistance	Full	IV	50	72.5	95	kΩ

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
OVERALL						
Analog Supply Voltage (VDDA, VDDF, VDDI)	Full	VI	2.7	3.0	3.6	V
Digital Supply Voltage (VDDD, VDDC, VDDL)	Full	VI	2.7	3.0	3.6	V
Interface Supply Voltage (VDDH)[6]	Full	VI	1.8		3.6	V
Charge Pump Supply Voltage (VDDP, VDDQ)	Full	VI	2.7	5.0	5.5	V
Total Current						
Operation Mode[7]	Full	VI		17		mA
Standby	Full	VI		0.01		mA
OPERATING TEMPERATURE RANGE			−40		+85	°C

[1] This includes 0.9 dB loss of matching network.
[2] AGC with DVGA enabled.
[3] Measured in 10 kHz bandwidth.
[4] Programmable in 0.67 mA steps.
[5] Voltage span in which LO (or CLK) charge pump output current is maintained within 5% of nominal value of VDDP/2 (or VDDQ/2).
[6] VDDH must be less than VDDD + 0.5 V.
[7] Clock VCO off and additional 0.7 mA with VGA at maximum attenuation.

DIGITAL SPECIFICATIONS

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 2.7 V to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted. Standard operating mode: VGA at minimum attenuation setting, synthesizers in normal (not fast acquire) mode, decimation factor = 900, 16-bit digital output, and 10 pF load on SSI output pins.

Table 2.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
DECIMATOR						
Decimation Factor[1]	Full	IV	48		960	
Pass-Band Width	Full	V		50%		f_{CLKOUT}
Pass-Band Gain Variation	Full	IV			1.2	dB
Alias Attenuation	Full	IV	88			dBm
SPI READ OPERATION (See Figure 30)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock High (t_{HI})	Full	IV	45			ns
PC Clock Low (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
PE to PC Setup Time (t_S)	Full	IV	5			ns
PC to PE Hold Time (t_H)	Full	IV	5			ns
SPI WRITE OPERATION[2] (See Figure 29)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock High (t_{HI})	Full	IV	45			ns
PC Clock Low (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
PC to PD (or DOUTB) Data Valid Time (t_{DV})	Full	IV	3			ns
PE to PD Output Valid to High-Z (t_{EZ})	Full	IV		8		ns
SSI[2] (See Figure 33)						
CLKOUT Frequency	Full	IV	0.867		26	MHz
CLKOUT Period (t_{CLK})	Full	IV	38.4		1153	ns
CLKOUT Duty Cycle (t_{HI}, t_{LOW})	Full	IV	33	50	67	ns
CLKOUT to FS Valid Time (t_V)	Full	IV	−1		+1	ns
CLKOUT to DOUT Data Valid Time (t_{DV})	Full	IV	−1		+1	ns
CMOS LOGIC INPUTS[3]						
Logic 1 Voltage (V_{IH})	Full	IV	0.7 × VDDH			V
Logic 0 Voltage (V_{IL})	Full	IV			0.3 × VDDH	V
Logic 1 Current (I_{IH})	Full	IV		10		µA
Logic 0 Current (I_{IL})	Full	IV		10		µA
Input Capacitance	Full	IV		3		pF
CMOS LOGIC OUTPUTS[2, 3, 4]						
Logic 1 Voltage (V_{OH})	Full	IV	VDDH − 0.2			V
Logic 0 Voltage (V_{OL})	Full	IV			0.2	V

[1] Programmable in steps of 48 or 60.
[2] CMOS output mode with C_{LOAD} = 10 pF and drive strength = 7.
[3] Absolute maximum and minimum input/output levels are VDDH + 0.3 V and −0.3 V.
[4] I_{OL} = 1 mA; specification is also dependent on drive strength setting.

ABSOLUTE MAXIMUM RATINGS

Table 3. AD9864 Absolute Maximum Ratings

Parameter	With Respect To	Rating
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDS	−0.3 to +4.0
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	VDDR, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	−4.0 V to +4.0 V
VDDP, VDDQ	GNDP, GNDQ	−0.3 V to +6.0 V
GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	−0.3 V to +0.3 V
MXOP, MXON, LOP, LON, IFIN, CXIF, CXVL, CXVM	GNDH	−0.3 V to VDDI + 0.3 V
PC, PD, PE, CLKOUT, DOUTA, DOUTB, FS, SYNCB	GNDH	−0.3 V to VDDH + 0.3 V
IF2N, IF2P, GCP, GCN	GNDF	−0.3 V to VDDF + 0.3 V
VFEFP, VREGN, RREF	GNDA	−0.3 V to VDDA + 0.3 V
IOUTC	GNDQ	−0.3 V to VDDQ + 0.3 V
IOUTL	GNDP	−0.3 V to VDDP + 0.3 V
CLKP, CLKN	GNDC	−0.3 V to VDDC + 0.3 V
FREF	GNDL	−0.3 V to VDDL + 0.3 V
Maximum Junction Temperature		150°C
Storage Temperature		−65°C to +150°C
Maximum Lead Temperature		300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

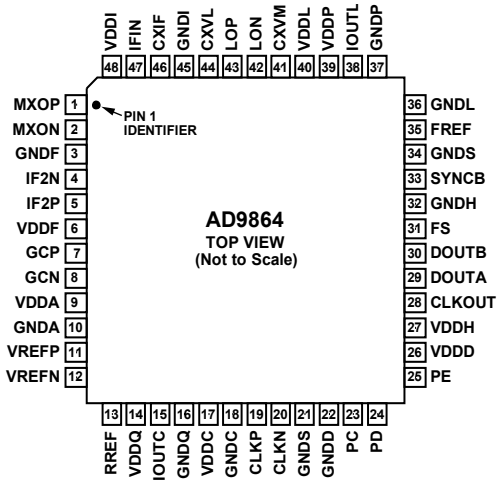
Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
48-Lead LFCSP	29.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE BACKSIDE PADDLE CONTACT IS NOT CONNECTED TO GROUND. A PCB GROUND PAD IS OPTIONAL.

04319-0-002

Figure 2. 48-Lead LFCSP Pin Configuration

Table 5. 48-Lead Lead Frame Chip Scale Package (LFCSP) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MXOP	Mixer Output, Positive.
2	MXON	Mixer Output, Negative.
3	GNDF	Ground for Front End of ADC.
4	IF2N	Second IF Input (to ADC), Negative.
5	IF2P	Second IF Input (to ADC), Positive.
6	VDDF	Positive Supply for Front End of ADC.
7	GCP	Filter Capacitor for ADC Full-Scale Control.
8	GCN	Full-Scale Control Ground.
9	VDDA	Positive Supply for ADC Back End.
10	GNDA	Ground for ADC Back End.
11	VREFP	Voltage Reference, Positive.
12	VREFN	Voltage Reference, Negative.
13	RREF	Reference Resistor: Requires 100 kΩ to GNDA.
14	VDDQ	Positive Supply for Clock Synthesizer.
15	IOUTC	Clock Synth Charge Pump Out Current.
16	GNDQ	Ground for Clock Synthesizer Charge Pump.
17	VDDC	Positive Supply for Clock Synthesizer.
18	GNDC	Ground for Clock Synthesizer.
19	CLKP	Sampling Clock Input/Clock VCO Tank, Positive.
20	CLKN	Sampling Clock Input/Clock VCO Tank, Negative.
21	GNDS	Substrate Ground.
22	GNDD	Ground for Digital Functions.
23	PC	Clock Input for SPI Port.
24	PD	Data I/O for SPI Port.
25	PE	Enable Input for SPI Port.
26	VDDD	Positive Supply for Internal Digital.
27	VDDH	Positive Supply for Digital Interface.
28	CLKOUT	Clock Output for SSI Port.
29	DOUTA	Data Output for SSI Port.
30	DOUTB	Data Output for SSI Port (Inverted) or SPI Port.
31	FS	Frame Sync for SSI Port.

Pin No.	Mnemonic	Description
32	GNDH	Ground for Digital Interface.
33	SYNCB	Resets SSI and Decimator Counters; Active Low. Connect to VDDH if unused.
34	GNDS	Substrate Ground.
35	FREF	Reference Frequency Input for Both Synthesizers.
36	GNDL	Ground for LO Synthesizer.
37	GNDP	Ground for LO Synthesizer Charge Pump.
38	IOUTL	LO Synthesizer Charge Pump Out Current.
39	VDDP	Positive Supply for LO Synthesizer Charge Pump.
40	VDDL	Positive Supply for LO Synthesizer.
41	CXVM	External Filter Capacitor; DC Output of LNA.
42	LON	LO Input to Mixer and LO Synthesizer, Negative.
43	LOP	LO Input to Mixer and LO Synthesizer, Positive.
44	CXVL	External Bypass Capacitor for LNA Power Supply.
45	GNDI	Ground for Mixer and LNA.
46	CXIF	External Capacitor for Mixer V-I Converter Bias.
47	IFIN	First IF Input (to LNA).
48	VDDI	Positive Supply for LNA and Mixer.
	EPAD	Exposed Pad. The backside paddle contact is not connected to ground. A PCB ground pad is optional.

TYPICAL PERFORMANCE CHARACTERISTICS

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = VDDx , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK synthesizer disabled, 16-bit data with AGC and DVGA enabled, unless otherwise noted.

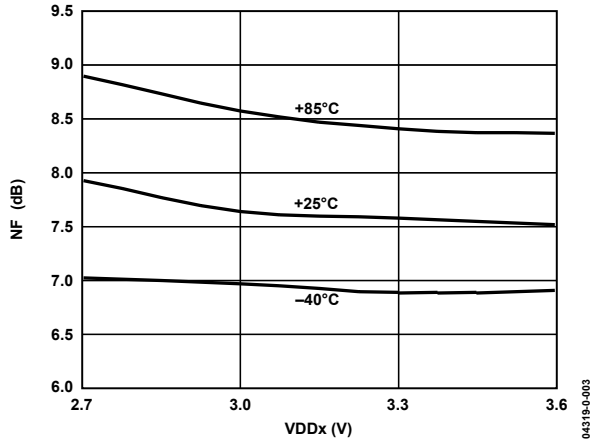


Figure 3. SSB Noise Figure vs. Supply

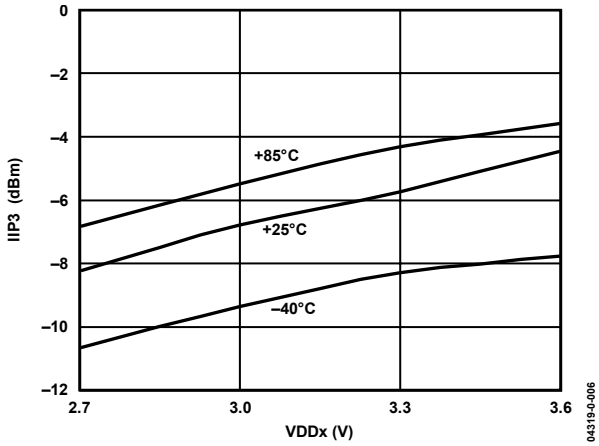


Figure 6. IIP3 vs. Supply

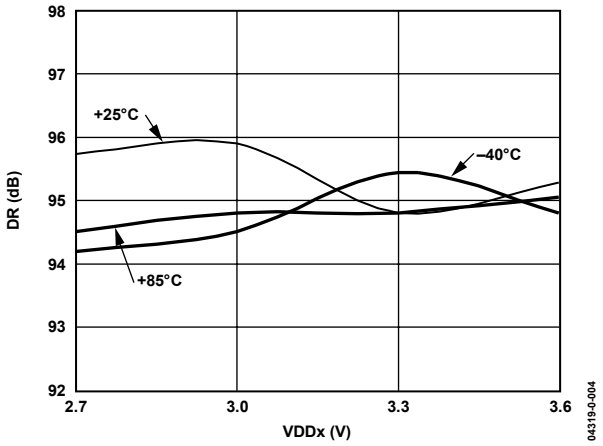


Figure 4. Dynamic Range (DR) vs. Supply

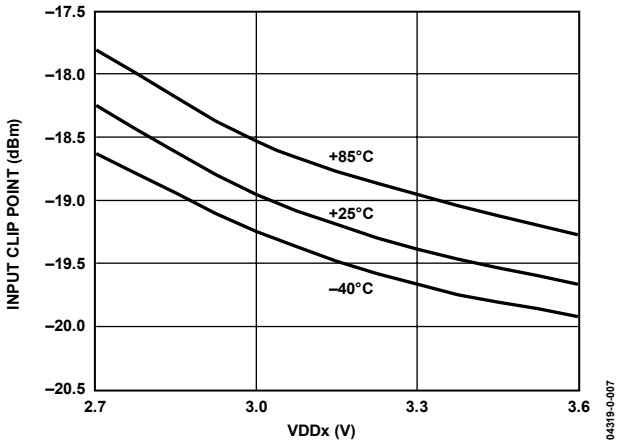


Figure 7. Maximum VGA Attenuation Clip Point vs. Supply

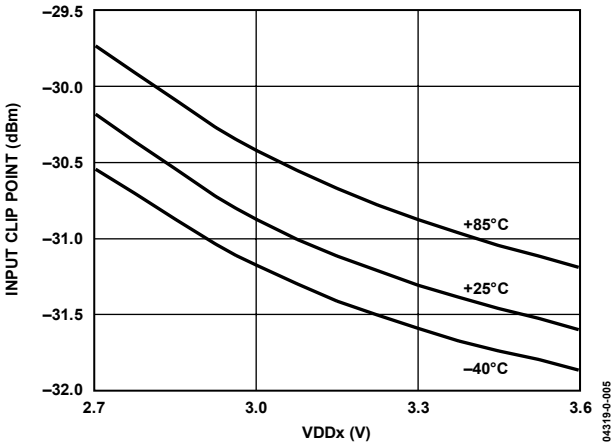


Figure 5. Minimum VGA Attenuation Clip Point vs. Supply

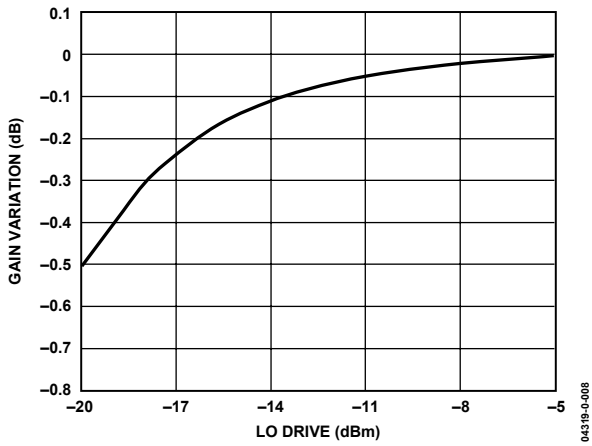


Figure 8. Normalized Gain Variation vs. LO Drive (VDDx = 3.0 V)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK synthesizer disabled, unless otherwise noted.

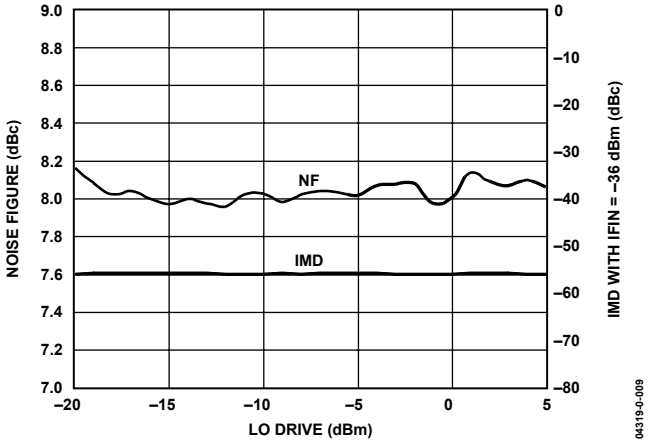


Figure 9. Noise Figure and IMD vs. LO Drive (VDDx = 3.0 V)

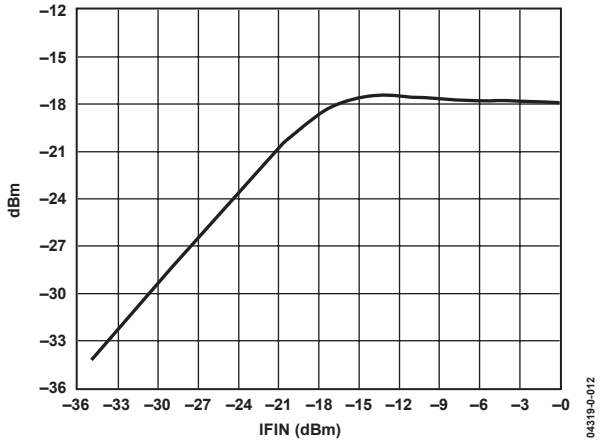


Figure 12. Gain Compression vs. IFIN with 16 dB LNA Attenuator Enabled

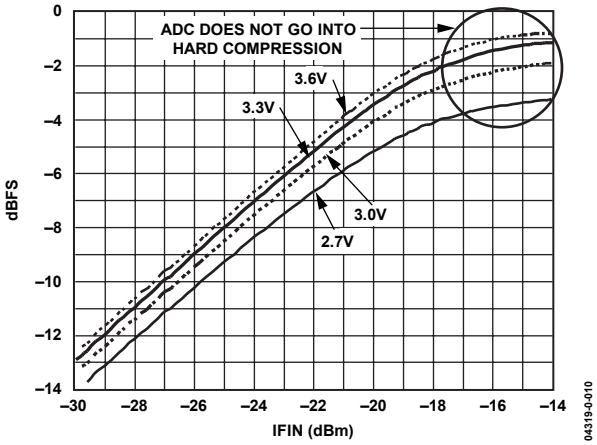


Figure 10. Gain Compression vs. IFIN

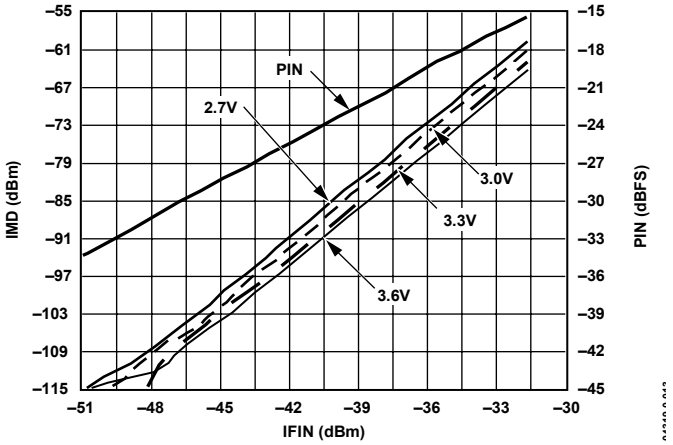


Figure 13. IMD vs. IFIN

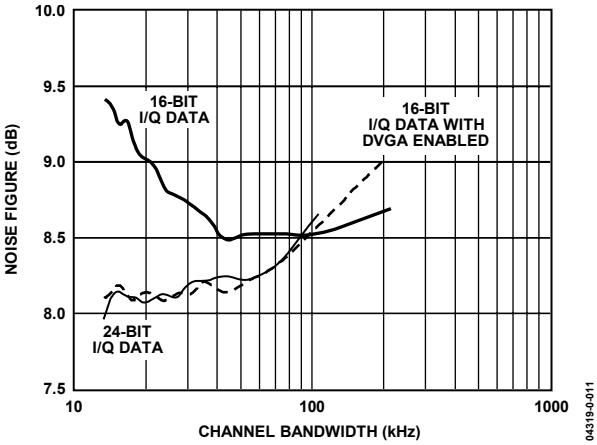


Figure 11. Noise Figure vs. Bandwidth (Minimum Attenuation, f_{CLK} = 13 MSPS)

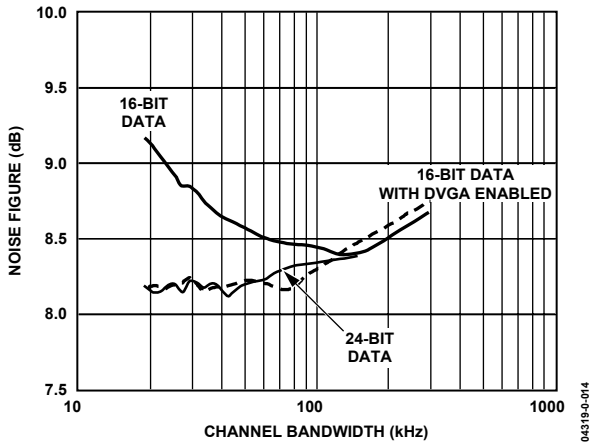


Figure 14. Noise Figure vs. Bandwidth (Minimum Attenuation, f_{CLK} = 18 MSPS)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK Synthesizer Disabled, unless otherwise noted.

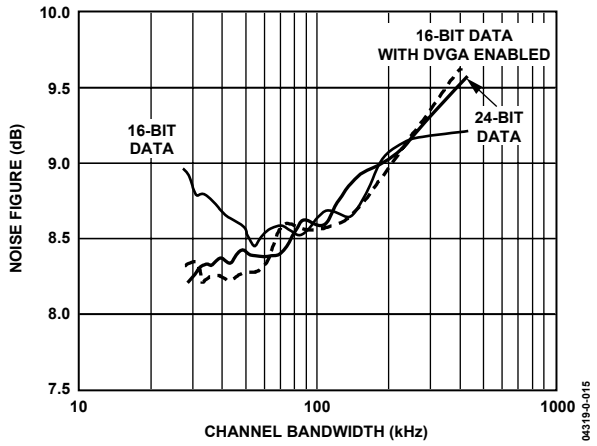


Figure 15. Noise Figure vs. Bandwidth (Minimum Attenuation, f_{CLK} = 26 MSPS)

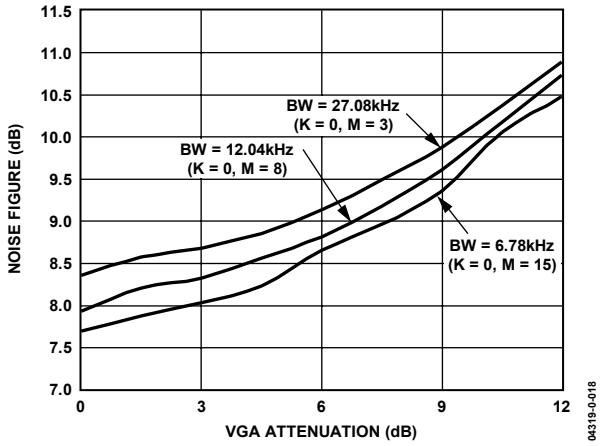


Figure 18. Noise Figure vs. VGA Attenuation (f_{CLK} = 13 MSPS)

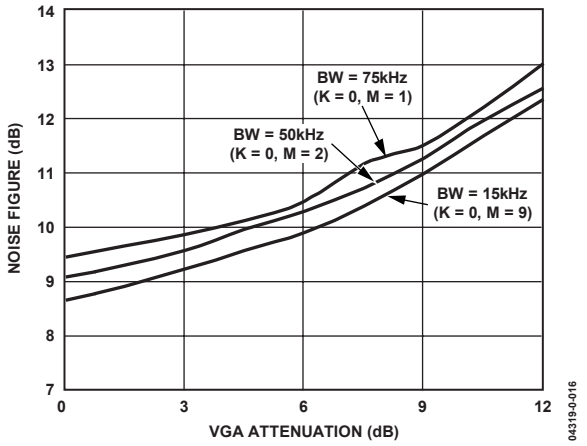


Figure 16. Noise Figure vs. VGA Attenuation (f_{CLK} = 18 MSPS)

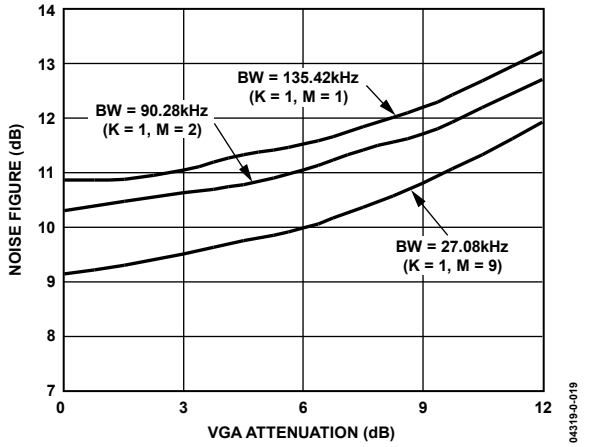


Figure 19. Noise Figure vs. VGA Attenuation (f_{CLK} = 26 MSPS)

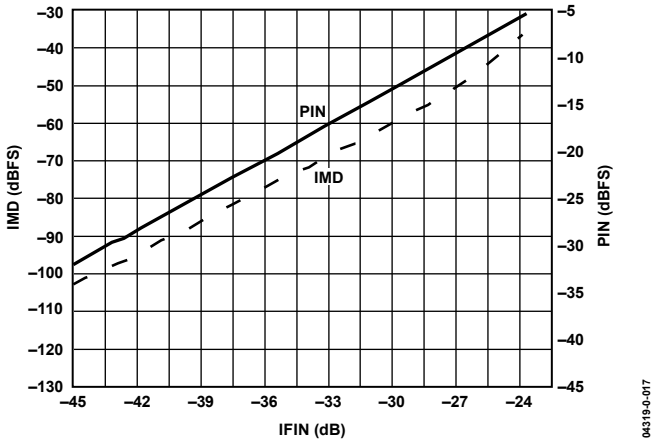


Figure 17. IMD vs. IFIN (f_{CLK} = 13 MSPS)

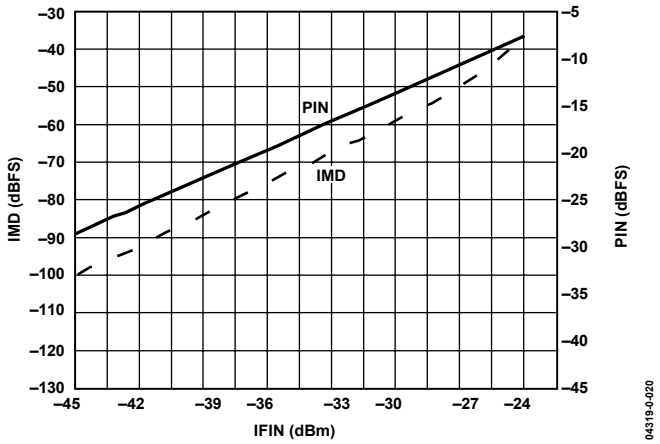


Figure 20. IMD vs. IFIN (f_{CLK} = 18 MSPS)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK synthesizer disabled, 16-bit data with AGC and DVGA enabled, unless otherwise noted.

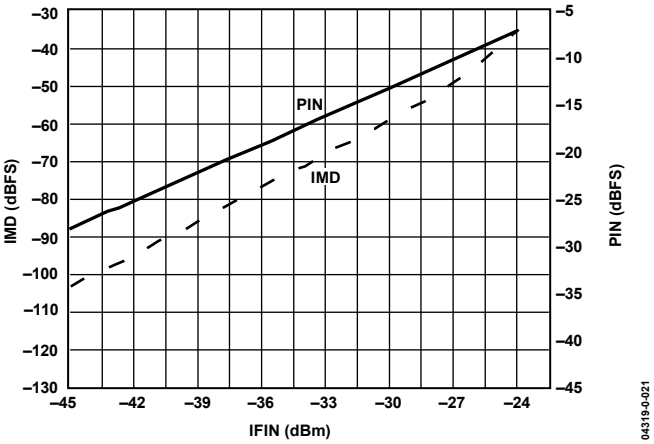


Figure 21. IMD vs. IFIN (f_{CLK} = 26 MSPS)

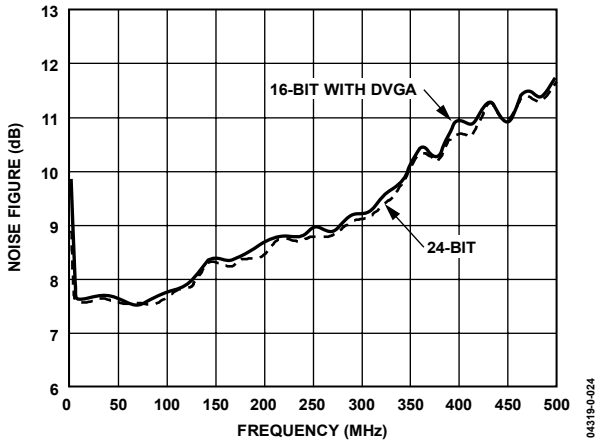


Figure 24. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 18 MSPS, BW = 10 kHz)

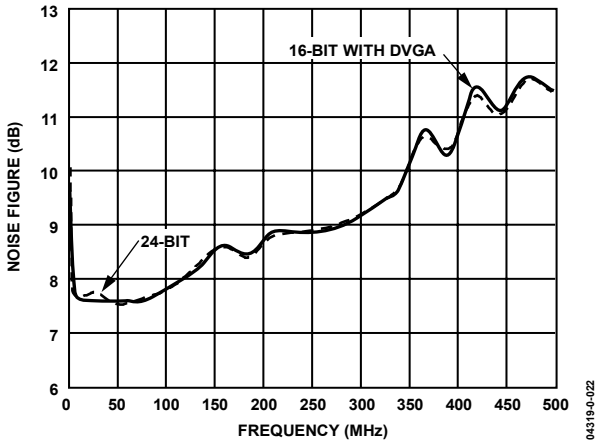


Figure 22. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 26 MSPS, BW = 10 kHz)

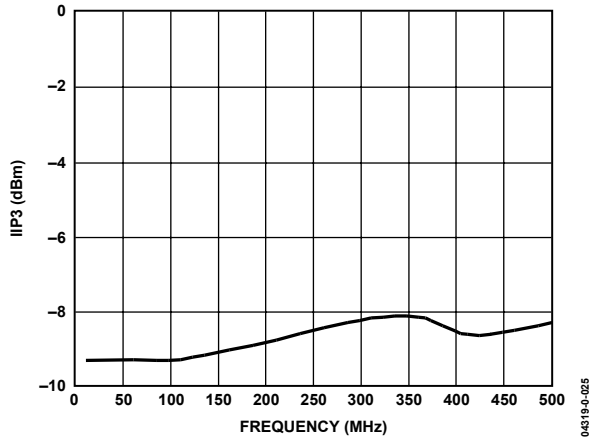


Figure 25. Input IIP3 vs. Frequency (f_{CLK} = 18 MSPS)

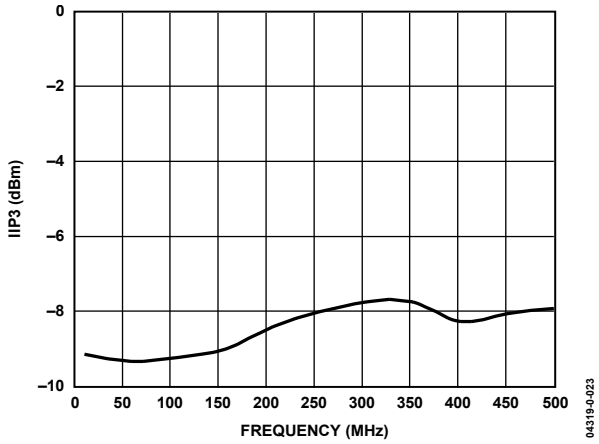


Figure 23. Input IIP3 vs. Frequency (f_{CLK} = 26 MSPS)

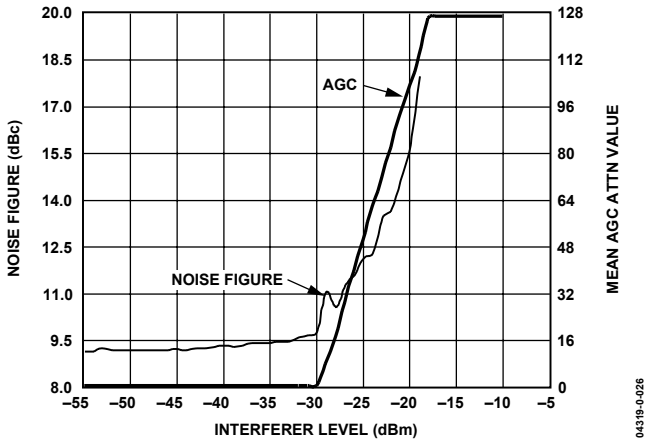


Figure 26. Noise Figure vs. Interferer Level (16-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER}$ = f_{IF} + 110 kHz)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK Synthesizer Disabled, AGC enabled, unless otherwise noted.

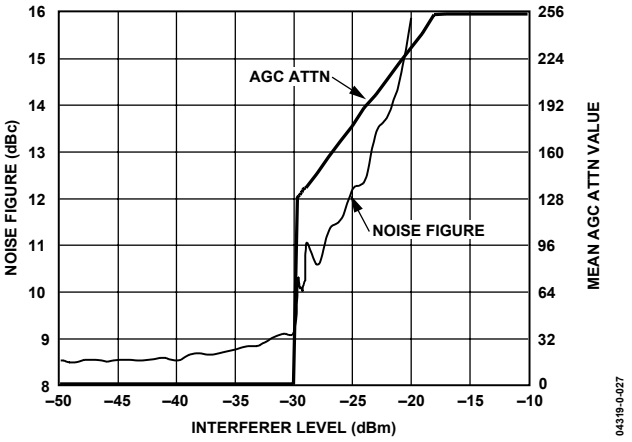


Figure 27. Noise Figure vs. Interferer Level (16-Bit Data with DVGA, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER}$ = f_{IF} + 110 kHz)

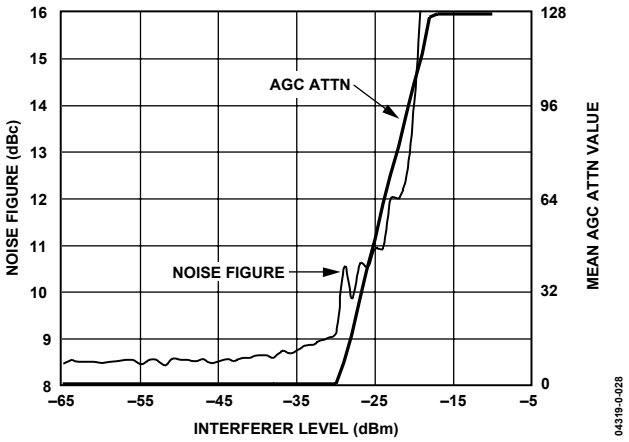


Figure 28. Noise Figure vs. Interferer Level (24-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER}$ = f_{IF} + 110 kHz)

TERMINOLOGY

Single Sideband Noise Figure (SSB NF)

Noise figure (NF) is defined as the degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system. It can be expressed with the equation

$$Noise\ Figure = 10 \times \log(SNR_{IN}/SNR_{OUT})$$

The term SSB is applicable for heterodyne systems containing a mixer. It indicates that the desired signal spectrum resides on only one side of the LO frequency (that is, single sideband); therefore, a noiseless mixer has a noise figure of 3 dB.

The SSB noise figure of the AD9864 is determined by the equation

$$SSB\ NF = P_{IN} - [10 \times \log(BW)] - (-174\ \text{dBm/Hz}) - SNR$$

where:
P_{IN} is the input power of an unmodulated carrier.
BW is the noise measurement bandwidth.
−174 dBm/Hz is the thermal noise floor at 293 K.
SNR is the measured signal-to-noise ratio in dB of the AD9864.

Note that P_{IN} is set to −85 dBm to minimize any degradation in measured SNR due to phase noise from the RF and LO signal generators. The IF frequency, CLK frequency, and decimation factors are selected to minimize any spurious components falling within the measurement bandwidth. Note also that a bandwidth of 10 kHz is used for the data sheet specification. All references to noise figures within this data sheet imply single sideband noise figure.

Input Third-Order Intercept (IIP3)

IIP3 is a figure of merit used to determine the susceptibility of a component or system to intermodulation distortion (IMD) from its third-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting third-order nonlinearities producing IMD components at 2f1 − f2 and 2f2 − f1. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third-order IMD component when plotted in dB. The difference in power (D in dBc) between the two carriers, and the resulting third-order IMD components can be determined from the equation

$$D = 2 \times (IIP3 - P_{IN})$$

Dynamic Range (DR)

Dynamic range is the measure of a small target input signal (P_{TARGET}) in the presence of a large unwanted interferer signal (P_{INTER}). Typically, the large signal causes some unwanted characteristic of the component or system to degrade, thus making it unable to detect the smaller target signal correctly. For the AD9864, it is often a degradation in noise figure at increased VGA attenuation settings that limits its dynamic range.

The test method for the AD9864 is as follows. The small target signal (an unmodulated carrier) is input at the center of the IF frequency, and its power level (P_{TARGET}) is adjusted to achieve an SNR_{TARGET} of 6 dB. The power of the signal is then increased by 3 dB prior to injecting the interferer signal. The offset frequency of the interferer signal is selected so that aliases produced by the response of the decimation filter, as well as phase noise from the LO (due to reciprocal mixing), do not fall back within the measurement bandwidth. For this reason, an offset of 110 kHz was selected. The interferer signal (also an unmodulated carrier) is then injected into the input and its power level is increased to the point (P_{INTER}) where the target signal SNR is reduced to 6 dB. The dynamic range is determined with the equation

$$DR = P_{INTER} - P_{TARGET} + SNR_{TARGET}$$

Note that the AGC of the AD9864 is enabled for this test.

IF Input Clip Point

The IF input clip point is defined as the input power that results in a digital output level 2 dB below full scale. Unlike other linear components that typically exhibit a soft compression (characterized by its 1 dB compression point), an ADC exhibits a hard compression when its input signal exceeds its rated maximum input signal range. For the AD9864, which contains a Σ-Δ ADC, hard compression must be avoided because it causes severe SNR degradation.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI is a bidirectional serial port. It is used to load the configuration information into the registers listed in Table 6, as well as to read back their contents. Table 6 provides a list of the registers that can be programmed through the SPI port. Addresses and default values are given in hexadecimal form.

Table 6. SPI Address Map

Address (Hex)	Bit(s)	Width	Default Value	Name	Description
Power Control Registers					
0x00	[7:0]	8	0xFF	STBY	Standby control bits (REF, LO, CKO, CK, GC, LNAMX, unused, and ADC). Default is power-up condition of standby.
0x01	[3:2]	2	0x00	CKOB	CK oscillator bias (0 = 0.25 mA, 1 = 0.35 mA, 2 = 0.40 mA, 3 = 0.65 mA).
	[1:0]	2	0x00	ADCB	Do not use.
0x02	[7:0]	8	0x00	TEST	Factory test mode. Do not use.
AGC					
0x03	7	1	0	ATTEN	Apply 16 dB attenuation in the front end.
	[6:0]	7	0x00	AGCG [14:8]	AGC attenuation setting (7 MSBs of a 15-bit unsigned word).
0x04	[7:0]	8	0x00	AGCG [7:0]	AGC attenuation setting (8 LSBs of a 15-bit unsigned word).
0x05	[7:4]	4	0x00	AGCA	AGC attack bandwidth setting. Default yields 50 Hz loop bandwidth.
	[3:0]	4	0x00	AGCD	AGC decay time setting. Default is decay time = attack time.
0x06	7	1	0	AGCV	Enable digital VGA to increase AGC range by 12 dB.
	[6:4]	3	0x00	AGCO	AGC overload update setting. Default is slowest update.
	3	1	0	AGCF	Fast AGC (minimizes resistance seen between GCP and GCN).
	[2:0]	3	0x00	AGCR	AGC enable/reference level (disabled, 3 dB, 6 dB, 9 dB, 12 dB, 15 dB below clip).
Decimation Factor					
0x07	[7:5]	3		Unused	
	4	1	0	K	Decimation factor = 60 × (M + 1), if K = 0; 48 × (M + 1), if K = 1.
	[3:0]	4	0x04	M	Default is decimate-by-300.
LO Synthesizer					
0x08	[5:0]	6	0x00	LOR [13:8]	Reference frequency divider (6 MSBs of a 14-bit word).
0x09	[7:0]	8	0x38	LOR [7:0]	Reference frequency divisor (8 LSBs of a 14-bit word). Default (56) yields 300 kHz from f_{REF} = 16.8 MHz.
0x0A	[7:5]	3	0x05	LOA	A counter (prescaler control counter).
	[4:0]	5	0x00	LOB [12:8]	B counter MSB (5 MSB of a 13-bit word). Default LOA and LOB values yield 300 kHz from 73.35 MHz to 2.25 MHz.
0x0B	[7:0]	8	0x1D	LOB [7:0]	B counter LSB (8 LSB of a 13-bit word).
0x0C	6	1	0	LOF	Enable fast acquire.
	5	1	0	LOINV	Invert charge pump (0 = source current to increase VCO frequency).
	[4:2]	3	0x00	LOI	Charge pump current in normal operation. I_{PUMP} = (LOI +1) × 0.625 mA.
	[1:0]	2	0x03	LOTM	Manual control of LO charge pump (0 = off, 1 = up, 2 = down, and 3 = normal).
0x0D	[5:0]	6	0x00	LOFA [13:8]	LO fast acquire time unit (6 MSBs of a 14-bit word).
0x0E	[7:0]	8	0x04	LOFA [7:0]	LO fast acquire time unit (8 LSBs of a 14-bit word).
Clock Synthesizer					
0x10	[5:0]	6	0x00	CKR [13:8]	Reference frequency divisor (6 MSBs of a 14-bit word).
0x11	[7:0]	8	0x38	CKR [7:0]	Reference frequency divisor (8 LSBs of a 14-bit word). Default yields 300 kHz from f_{REF} = 16.8 MHz; minimum = 3, maximum = 16383.
0x12	[4:0]	5	0x00	CKN [12:8]	Synthesized frequency divisor (5 MSBs of a 13-bit word).
0x13	[7:0]	8	0x3C	CKN [7:0]	Synthesized frequency divisor (8 LSBs of a 13-bit word). Default yields 300 kHz from 18 MHz; minimum = 3, maximum = 8191.

Address (Hex)	Bit(s)	Width	Default Value	Name	Description
0x14	6	1	0	CKF	Enable fast acquire.
	5	1	0	CKINV	Invert charge pump (0 = source current to increase VCO frequency).
	[4:2]	3	0x00	CKI	Charge pump current in normal operation. I_{PUMP} = (CKI + 1) × 0.625 mA.
	[1:0]	2	0x03	CKTM	Manual control of CLK charge pump (0 = off, 1 = up, 2 = down, and 3 = normal).
0x15	[5:0]	6	0x00	CKFA [13:8]	CK fast acquire time unit (6 LSBs of a 14-bit word).
0x16	[7:0]	8	0x04	CKFA [7:0]	CK fast acquire time unit (8 LSBs of a 14-bit word).
SSI Control					
0x18	[7:0]	8	0x12	SSICRA	SSI Control Register A. See the SSI Control Registers section. Default is FS and CLKOUT three-stated.
0x19	[7:0]	8	0x07	SSICRB	SSI Control Register B. See the SSI Control Registers section (16-bit data, maximum drive strength).
0x1A	[3:0]	4	0x01	SSIORD	Output rate divisor. $f_{CLKOUT} = f_{CLK}$/SSIORD.
ADC Tuning					
0x1C	1	1	0	TUNE_LC	Perform tuning on LC portion of the ADC (cleared when done).
	0	1	0	TUNE_RC	Perform tuning on RC portion of the ADC (cleared when done).
0x1D	[3:0]	3	0x00	CAPL1 [2:0]	Coarse capacitance setting of LC tank (LSB is 25 pF, differential).
0x1E	[5:0]	6	0x00	CAPL0 [5:0]	Fine capacitance setting of LC tank (LSB is 0.4 pF, differential).
0x1F	[7:0]	8	0x00	CAPR	Capacitance setting for RC resonator (64 LSB of fixed capacitance).
Test Registers and SPI Port Read Enable					
0x37	[7:0]	8	0x00	TEST	Factory test mode. Do not use.
0x38	[7:1]	7	0x00	TEST	Factory test mode. Do not use.
	0	1	0	DACCR	Manual feedback DAC control
0x39	[7:0]	8	0x00	DACDATA	Feedback DAC data setting in manual mode.
0x3A	[7:4]	4	0x00	TEST	Factory test mode. Do not use.
	3	1	0	SPIREN	Enable read from SPI port.
	[2:0]	3	0x00	TEST	Factory test mode. Do not use.
0x3B	[7:4]	4	0x00	TEST	Factory test mode. Do not use.
	3	1	0	TRI	Three-state DOUTB.
	[2:0]	3	0x00	TEST	Factory test mode. Do not use.
0x3C to 0x3D	[7:0]	8	0x00	TEST	Factory test mode. Do not use.
0x3E	7	1	0	TEST	Factory test mode. Do not use.
	6	1	0	OVL	ADC overload detector.
	[5:3]	3	0	TEST	Factory test mode. Do not use.
	2	2	0	RC_Q	RC Q enhancement.
	1	1	0	RC_BYP	Bypass RC resonator.
	0	1	0	SC_BYP	Bypass SC resonators.
0x3F	[7:0]	8	Subject to change	ID	Revision ID (read-only). A write of 0x99 to this register is equivalent to a power-on reset.

THEORY OF OPERATION

INTRODUCTION

The AD9864 is a general-purpose, narrow-band IF subsystem that digitizes a low level, 10 MHz to 300 MHz IF input with a signal bandwidth ranging from 6.8 kHz to 270 kHz. The signal chain of the AD9864 consists of an LNA, a mixer, a band-pass Σ-Δ ADC, and a decimation filter with programmable decimation factor.

The input LNA is a fixed gain block with an input impedance of approximately 370 Ω||1.4 pF. The LNA input is single-ended and self biasing, allowing the input IF to be ac-coupled. The LNA can be disabled through the serial interface, providing a fixed 16 dB attenuation to the input signal.

The LNA drives the input port of a Gilbert-type active mixer. The mixer LO port is driven by the on-chip LO buffer, which can be driven externally, single-ended, or differential. The LO buffer inputs are self biasing and allow the LO input to be ac-coupled. The open-collector outputs of the mixer drive an external resonant tank consisting of a differential LC network tuned to the IF of the band-pass Σ-Δ ADC.

The external differential LC tank forms the resonator for the first stage of the band-pass Σ-Δ ADC. The tank LC values must be selected for a center frequency of $f_{CLK}/8$, where f_{CLK} is the sample rate of the ADC. The $f_{CLK}/8$ frequency is the IF digitized by the band-pass Σ-Δ ADC. On-chip calibration allows standard tolerance inductor and capacitor values. The calibration is typically performed once at power-up.

The ADC contains a sixth-order, multibit band-pass Σ-Δ modulator that achieves very high instantaneous dynamic range over a narrow frequency band centered at $f_{CLK}/8$. The modulator output is quadrature mixed to baseband and filtered by three cascaded linear phase FIR filters to remove out-of-band noise.

The first FIR filter is a fixed, decimate by 12, using a fourth-order comb filter. The second FIR filter also uses a fourth-order comb filter with programmable decimation from 1 to 16. The third FIR stage is programmable for decimation of either 4 or 5.

The cascaded decimation factor is programmable from 48 to 960. The decimation filter data is output via the synchronous serial interface (SSI) of the chip.

Additional functionality built into the AD9864 includes LO and clock synthesizers, programmable AGC, and a flexible synchronous serial interface for output data.

The LO synthesizer is a programmable phase-locked loop (PLL) consisting of a low noise phase frequency detector (PFD), a variable output current charge pump (CP), a 14-bit reference divider, A and B counters, and a dual modulus prescaler. The user only needs to add an appropriate loop filter and VCO for complete operation.

The clock synthesizer is equivalent to the LO synthesizer with the following differences:

- It does not include the prescaler or A counter.
- It includes a negative resistance core used for VCO generation.

The AD9864 contains both a variable gain amplifier (VGA) and a digital VGA (DVGA). Both of these can operate manually or automatically. In manual mode, the gain for each is programmed through the SPI. In automatic gain control mode, the gains are adjusted automatically to ensure that the ADC does not clip and that the rms output level of the ADC is equal to a programmable reference level.

The VGA has 12 dB of attenuation range and is implemented by adjusting the ADC full-scale reference level. The DVGA gain is implemented by scaling the output of the decimation filter. The DVGA is most useful in extending the dynamic range in narrow-band applications requiring 16-bit I and Q data format.

The SSI provides a programmable frame structure, allowing 24-bit or 16-bit I and Q data and flexibility by including attenuation and RSSI data if required.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9864 has 3-wire or 4-wire SPI capability, allowing read/write access to all registers that configure the internal parameters of the device. The default 3-wire serial communication port consists of a clock (PC), peripheral enable (PE), and bidirectional data (PD) signal. The inputs to PC, PE, and PD contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about the digital interface supply, that is, VDDH/2.

A 4-wire SPI interface can be enabled by setting the MSB of the SSICRB register (Register 0x19, Bit 7) and setting Register 0x3A to 0x00, resulting in the output data appearing on only the DOUTB pin with the PD pin functioning as an input pin only. Note that because the default power-up state sets DOUTB low, bus contention is possible for systems sharing the SPI output line. To avoid any bus contention, the DOUTB pin can be three-stated by setting the fourth control bit in the three-state bit (Register 0x3B, Bit 3). This bit can then be toggled to gain access to the shared SPI output line.

An 8-bit instruction header must accompany each read and write SPI operation. Only the write operation supports an auto-increment mode, which allows the entire chip to be configured in a single write operation. The instruction header is shown in Table 7. It includes a read/not-write indicator bit, six address bits, and a Don't Care bit. The data bits immediately follow the instruction header for both read and write operations. Note that the address and data are always given MSB first.

Table 7. Instruction Header Information

MSB							LSB
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/W	A5	A4	A3	A2	A1	A0	X[1]

[1] X = don't care.

Figure 29 illustrates the timing requirements for a write operation to the SPI port. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the data pin (PD) on the rising edges of the next eight clock cycles. PE stays low during the operation and goes high at the end of the transfer. If PE rises before the eight clock cycles have passed, the operation is aborted. If PE stays low for an additional eight clock cycles, the destination address is incremented and another eight bits of data are shifted in. Again, if PE rises early, the current byte is ignored. By using this implicit addressing mode, the chip can be configured with a single write operation. Registers identified as being subject to frequent updates, namely those associated with power control and AGC operation, have been assigned adjacent addresses to minimize the time required to update them. Note that multibyte registers are big endian (the most significant byte has the lower address) and are updated when a write to the least significant byte occurs.

Figure 30 and Figure 31 illustrates the timing for 3-wire and 4-wire SPI read operations. Although the AD9864 does not require read access for proper operation, it is often useful in the product development phase or for system authentication. Note that the readback enable bit (Register 0x3A, Bit 3) must be set for a read operation with a 3-wire SPI interface. For 4-wire SPI operation, this bit remains low (Register 0x3A = 0x00) but DOUTB is enabled via the SSICRB register (Register 0x19, Bit 7). Note that for the 4-wire SPI interface, the eight data bits appear on the DOUTB pin with the same timing relationship as those appearing at PD for 3-wire SPI interface case.

After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the data pin (PD) on the falling edges of the next eight clock cycles. After the last data bit is shifted out, the user must return PE high, causing PD to become three-stated (for 3-wire case) and return to its normal status as an input pin. Since the auto-increment mode is not supported for read operations, an instruction header is required for each register read operation and PE must return high before initiating the next read operation.

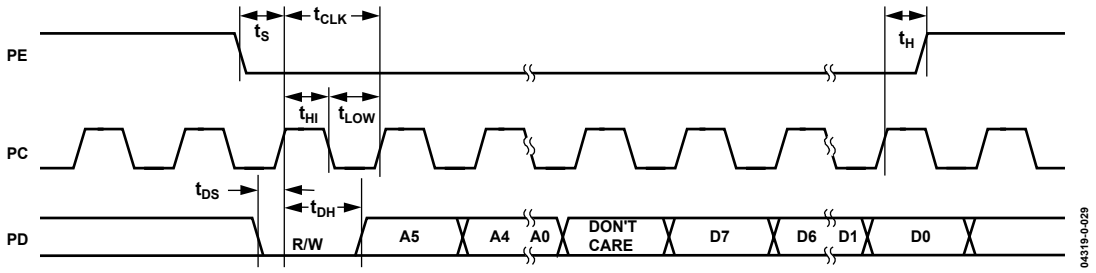


Figure 29. SPI Write Operation Timing

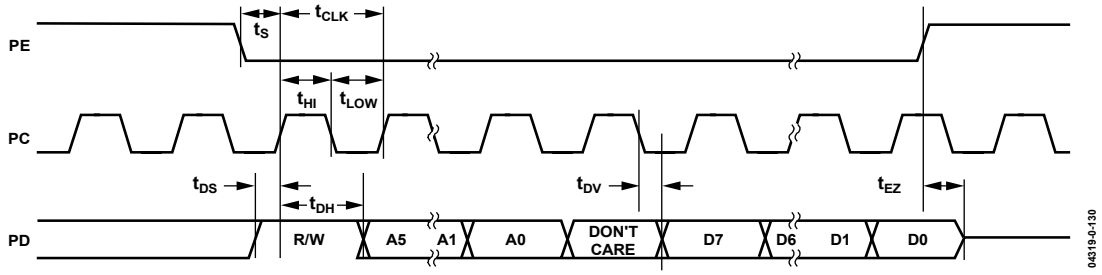


Figure 30. 3-Wire SPI Read Operation Timing

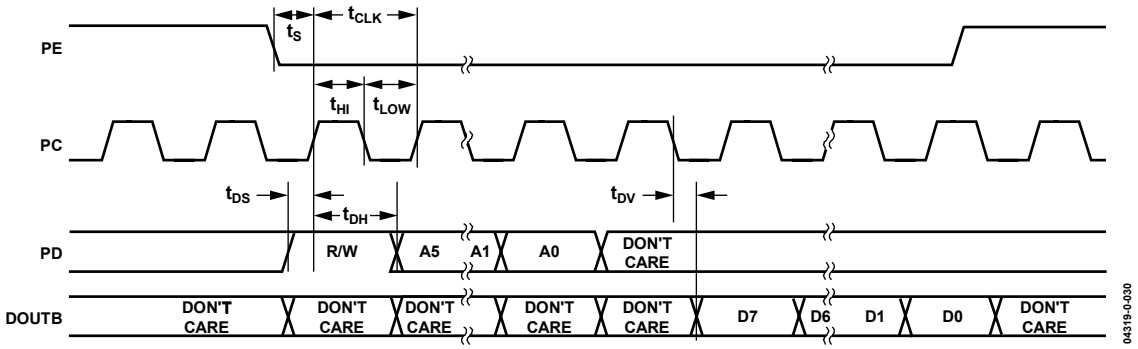


Figure 31. 4-Wire SPI Read Operation Timing

POWER-ON RESET

The SPI registers are automatically set to their default settings upon power-up when the VDDD supply crosses a threshold. This ensures that the AD9864 is in a known state and placed in standby for minimal power consumption. In the unlikely event that the SPI registers were not reset to their default settings, an equivalent software reset by writing 0x99 to Register 0x3F can be used as the first SPI write command to provide additional assurance.

SYNCHRONOUS SERIAL INTERFACE (SSI)

The AD9864 provides a high degree of programmability of its SSI output data format, control signals, and timing parameters to accommodate various digital interfaces. In a 3-wire digital interface, the AD9864 provides a frame sync signal (FS), a clock output (CLKOUT), and a serial data stream (DOUTA) signal to the host device. In a 2-wire interface, the frame sync information is embedded into the data stream, thus only CLKOUT and DOUTA output signals are provided to the host device. The SSI control registers are SSICRA, SSICRB, and SSIORD. Table 8 to Table 13 show the bit fields associated with these registers.

The primary output of the AD9864 is the converted I and Q demodulated signal available from the SSI port as a serial bit stream contained within a frame. The output frame rate is equal to the modulator clock frequency (f_{CLK}) divided by the digital filter's decimation factor that is programmed in the Decimator Register (0x07). The bit stream consists of an I word followed by a Q word, where each word is either 24 bits or 16 bits long and is given MSB first in twos complement form. Two optional bytes may also be included within the SSI frame following the Q word. One byte contains the AGC attenuation and the other byte contains both a count of modulator reset events and an estimate of the received signal amplitude (relative to full scale of the AD9864 ADC). Figure 32 illustrates the structure of the SSI data frames in a number of SSI modes.

The two optional bytes are output if the EAGC bit of SSICRA is set. The first byte contains the 8-bit attenuation setting (0 = no attenuation, 255 = 24 dB of attenuation), whereas the second byte contains a 2-bit reset field and 6-bit received signal strength field. The reset field contains the number of modulator reset events since the last report, saturating at 3. The received signal strength (RSSI) field is a linear estimate of the signal strength at the output of the first decimation stage; 60 corresponds to a full-scale signal.

The two optional bytes follow the I and Q data as a 16-bit word provided that the AAGC bit of SSICRA is not set. If the AAGC bit is set, the two bytes follow the I and Q data in an alternating fashion. In this alternate AGC data mode, the LSB of the byte containing the AGC attenuation is a 0, whereas the LSB of the byte containing reset and RSSI information is always a 1.

In a 2-wire interface, the embedded frame sync bit (EFS) within the SSICRA register is set to 1. In this mode, the framing information is embedded in the data stream, with each eight bits of data surrounded by a start bit (low) and a stop bit (high), and each frame ends with at least 10 high bits. FS remains either low or three-stated (default), depending on the state of the SFST bit. Other control bits can be used to invert the frame sync (SFSI), to delay the frame sync pulse by one clock period (SLFS), to invert the clock (SCKI), or to three-state the clock (SCKT). Note that if EFS is set, SLFS is a don't care bit.

The SSIORD register controls the output bit rate (f_{CLKOUT}) of the serial bit stream. f_{CLKOUT} can be set equal to the modulator clock frequency (f_{CLK}) or an integer fraction of it. It is equal to f_{CLK} divided by the contents of the SSIORD register. Note that f_{CLKOUT} must be chosen such that it does not introduce harmful spurs within the pass band of the target signal. Users must verify that the output bit rate is sufficient to accommodate the required number of bits per frame for a selected word size and decimation factor. Idle (high) bits are used to fill out each frame.

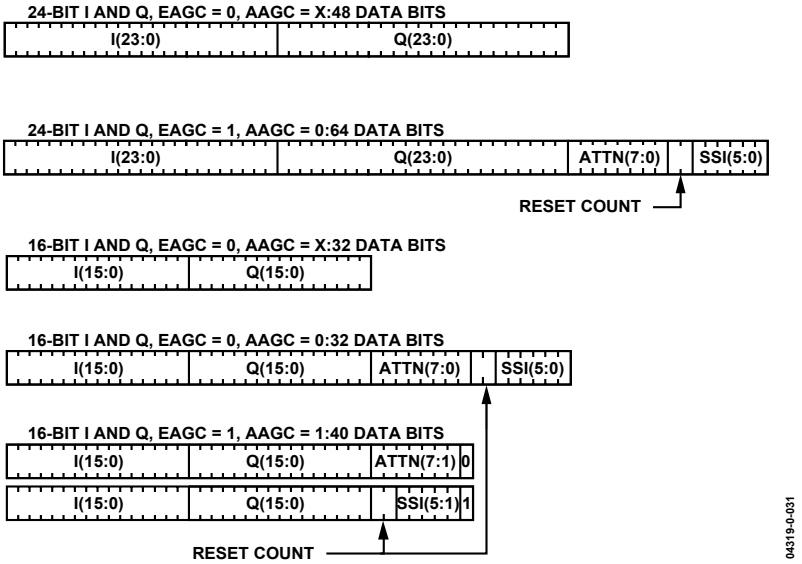


Figure 32. SSI Frame Structure

SSI CONTROL REGISTERS

SSICRA (Address 0x18)

Table 8. SSICRA Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AAGC	EAGC	EFS	SFST	SFSI	SLFS	SCKT	SCKI

Table 9. SSICRA Bit Descriptions

Bit(s)	Name	Width	Default	Description
7	AAGC	1	0	Alternate AGC data bytes.
6	EAGC	1	0	Embed AGC data.
5	EFS	1	0	Embed frame sync.
4	SFST	1	1	Three-state frame sync.
3	SFSI	1	0	Invert frame sync.
2	SLFS	1	0	Late frame sync (1 = late, 0 = early).
1	SCKT	1	1	Three-state CLKOUT.
0	SCKI	1	0	Invert CLKOUT.

SSICRB (Address 0x19)

Table 10. SSICRB Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4_SPI	Reserved	Reserved	Reserved	DW	DS_2	DS_1	DS_0

Table 11. SSICRB Bit Descriptions

Bit(s)	Name	Width	Default	Description
7	4_SPI	1	0	Enable 4-wire SPI interface for SPI read operation via DOUTB.
[6:4]	Reserved	3	0	Reserved.
3	DW	1	0	I/Q data-word width (0 = 16 bit, 1 = 24 bit). Automatically 16-bit when AGCV = 1.
[2:0]	DS	3	7	FS, CLKOUT, and DOUT drive strength Level 0 to Level 7, with 7 being the highest level.

SSIORD (Address 0x1A)

Table 12. SSIORD Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	DIV_3	DIV_2	DIV_1	DIV_0

Table 13. SSIORD Bit Descriptions

Bit(s)	Name	Width	Default	Description
[7:4]	Reserved	4	0	Reserved.
[3:0]	SSIORD	4	1	Output bit rate divisor setting $f_{CLKOUT} = f_{CLK}$/SSIORD where SSIORD = 1 to 15.

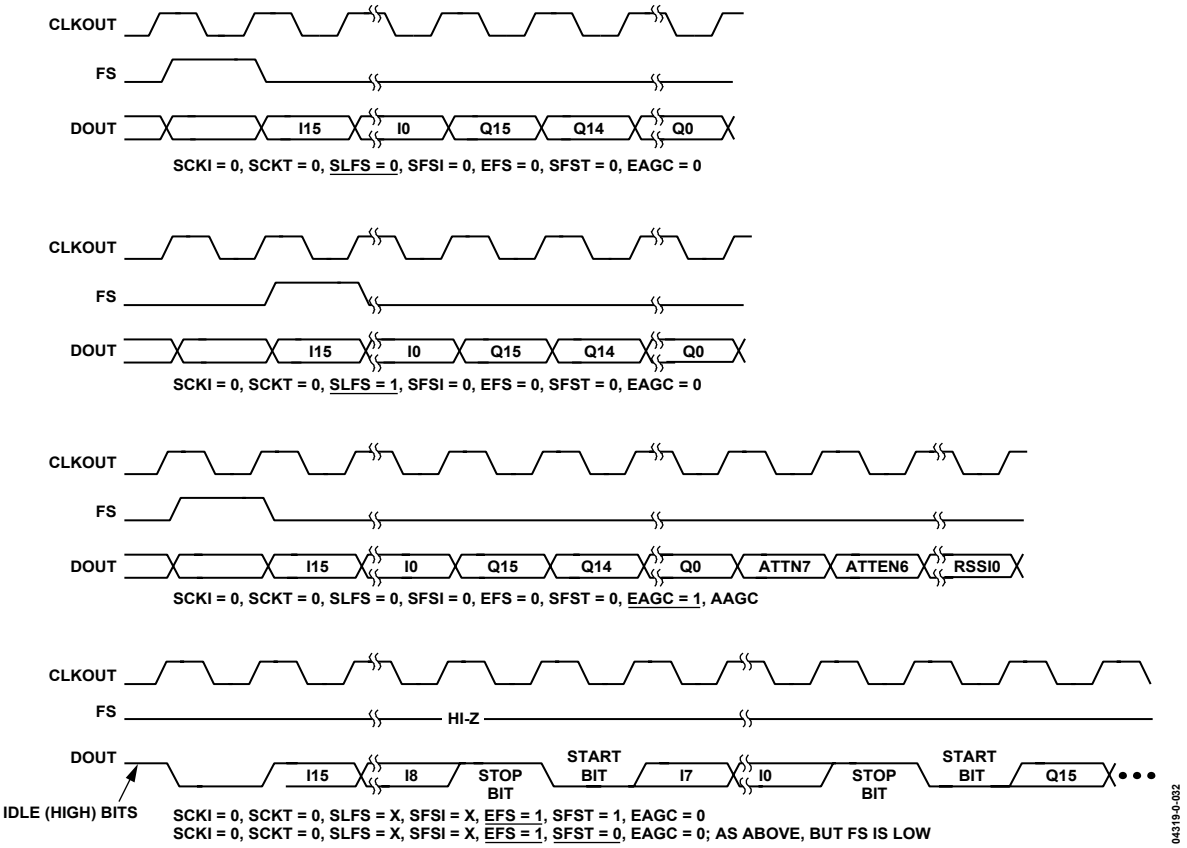


Figure 33. SSI Timing for Several SSICRA Settings with 16-Bit I/Q Data

Table 14. Number of Bits per Frame for Different SSICR Settings

DW	EAGC	EFS	AAGC	Number of Bits per Frame
0 (16 Bits)	0	0	N/A	32
	0	1	N/A	49[1]
	1	0	0	48
	1	0	1	40
	1	1	0	69[1]
	1	1	1	59[1]
1 (24 Bits)	0	0	N/A	48
	0	1	N/A	69[1]
	1	0	0	64
	1	0	1	56
	1	1	0	89[1]
	1	1	1	79[1]

[1] The number of bits per frame with embedded frame sync (EFS = 1); assume at least 10 idle bits are desired.
[2] N/A means not applicable.

The maximum SSIORD setting can be determined by the following equation:

$$SSIORD < TRUNC[(Decimation\ Factor)/(Number\ of\ Bits\ per\ Frame)] \quad (1)$$

where *TRUNC* is the truncated integer value.

If SSIORD = (decimation factor)/(number of bits per frame), the last bit in the SSI frame is not clocked out prior to FS returning high.

Table 14 lists the number of bits within a frame for 16-bit and 24-bit output data formats for all of the different SSICR settings. The decimation factor is determined by the contents of Register 0x07.

An example helps illustrate how the maximum SSIORD setting is determined. Suppose a user selects a decimation factor of 600 (Register 0x07, K = 0, M = 9) and prefers a 3-wire interface with a dedicated frame sync (EFS = 0) containing 24-bit data (DW = 1) with nonalternating embedded AGC data included (EAGC = 1, AAGC = 0). Referring to Table 14, each frame consists of 64 data bits. Using Equation 1, the maximum SSIORD setting is 9 (= *TRUNC*(600/64)). Therefore, the user can select any SSIORD setting between 1 and 9.

Figure 33 illustrates the output timing of the SSI port for several SSI control register settings with 16-bit I/Q data, and Figure 34 shows the associated timing parameters. Note that the same timing relationship holds for 24-bit I/Q data, with the exception that I and Q word lengths now become 24 bits. In the default mode of operation, data is shifted out on rising edges of CLKOUT after a pulse equal to a clock period is output from the frame sync (FS) pin. As described above, the output data consists of a 16-bit or 24-bit I sample followed by a 16-bit or 24-bit Q sample, plus two optional bytes containing AGC and status information.

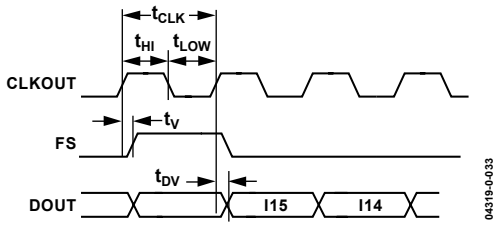


Figure 34. SSI Timing Parameters for SSI Timing

In Figure 34, the timing parameters also apply to inverted CLKOUT or FS modes, with t_{DV} relative to the falling edge of the CLK and/or FS.

The AD9864 also provides the means for controlling the switching characteristics of the digital output signals via the drive strength (DS) field of the SSICRB. This feature is useful in limiting switching transients and noise from the digital output that may ultimately couple back into the analog signal path, potentially degrading the sensitivity performance of the AD9864. Figure 35 and Figure 36 show how the NF can vary as a function of the SSI setting for an IF frequency of 109.65 MHz. The following two observations can be made from these figures:

1. The NF becomes more sensitive to the SSI output drive strength level at higher signal bandwidth settings.
2. The NF is dependent on the number of bits within an SSI frame that become more sensitive to the SSI output drive strength level as the number of bits is increased. Therefore, select the lowest possible SSI drive strength setting that still meets the SSI timing requirements.

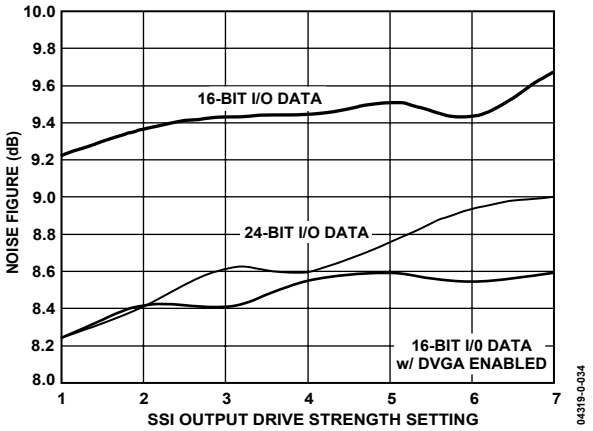


Figure 35. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 10 kHz)

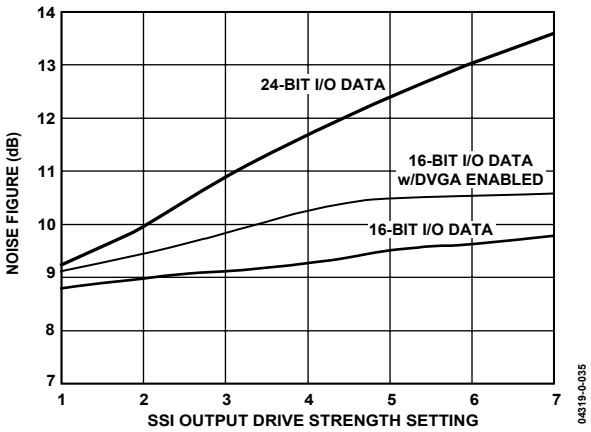


Figure 36. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 75 kHz)

Table 15 lists the typical output rise/fall times as a function of DS for a 10 pF load. Rise/fall times for other capacitor loads can be determined by multiplying the typical values presented by a scaling factor equal to the desired capacitive load divided by 10 pF.

Table 15. Typical Rise/Fall Times (±25%) with a 10 pF Capacitive Load for Each DS Setting

DS	Typ (ns)
0	13.5
1	7.2
2	50
3	3.7
4	3.2
5	2.8
6	2.3
7	2.0

SYNCHRONIZATION USING SYNCB

Many applications require the ability to synchronize one or more AD9864 devices in a way that causes the output data to be precisely aligned to an external asynchronous signal. For example, receiver applications employing diversity often require synchronization of the digital outputs of multiple AD9864 devices. Satellite communication applications using TDMA methods may require synchronization between payload bursts to compensate for reference frequency drift and Doppler effects.

SYNCB can be used for this purpose. It is an active-low signal that clears the clock counters in both the decimation filter and the SSI port. The counters in the clock synthesizers are not reset because it is presumed that the CLK signals of multiple chips would be connected. SYNCB also resets the modulator, resulting in a large-scale impulse that must propagate through the digital filter and SSI data formatting circuitry of the AD9864 before recovering valid output data. As a result, data samples unaffected by this SYNCB induced impulse can be recovered 12 output data samples after SYNCB goes high (independent of the decimation factor). Because SYNCB also resets the modulator, apply SYNCB only after the tuning of the band-pass Σ-Δ ADC has been completed during the initialization phase. For applications that may be performing a periodic SYNCB signal that is synchronous to FS, it is recommended that SYNCB assertion be applied after the rising edge of FS and three CLKOUT cycles before the arrival of the next FS pulse to avoid a possible runt FS pulse that could disrupt the host DSP/FPGA. Lastly, SYNCB must be tied high if unused because it does not include an internal pull-up resistor.

Figure 37 shows the timing relationship between SYNCB and the CLKOUT and FS signals of the SSI port. When the clock synthesizer is enabled to generate the input ADC clock, SYNCB is considered an asynchronous active-low signal that must remain low for at least half an input clock period, that is, $1/(2 \times f_{CLK})$. CLKOUT remains high while FS remains low upon SYNCB going low. CLKOUT becomes active within one to two output clock periods upon SYNCB returning high. If an external ADC clock input is supplied along with a synchronous SYNCB signal, it is recommended that SYNCB go low and returns high on the falling edges of the CLKIN signal to ensure consistent CLKOUT delay relative to rising edge of SYNCB. FS reappears several output cycles later, depending on the decimation factor of the digital filter and the SSIORD setting. Note that for any decimation factor and SSIORD setting, this delay is fixed and repeatable. To verify proper synchronization, monitor the FS signals of the multiple AD9864 devices.

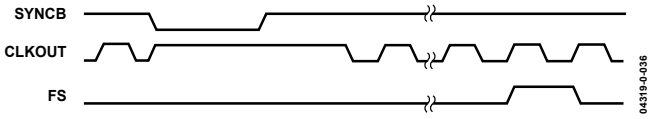


Figure 37. SYNCB Timing

INTERFACING TO DSPS

The AD9864 connects directly to an Analog Devices programmable digital signal processor (DSP). Figure 38 illustrates an example with the Blackfin® series processors, such as the ADSP-BF609. The Blackfin DSP series of 16-bit products is optimized for low power telecommunications applications with its dynamic power management feature, making it well suited for portable radio products. The code compatible family members share the fundamental core attributes of high performance, low power consumption, and the ease-of-use advantages of a microcontroller instruction set.

As shown in Figure 38, the synchronous serial interface (SSI) of the AD9864 links the receive data stream to the serial port (SPORT) of the DSP. For AD9864 setup and register programming, the device connects directly to the SPI port of the DSP. Dedicated select lines (SEL) allow the DSP to program and read back registers of multiple devices using only one SPI port. The DSP driver code pertaining to this interface is available on the AD9864 product page.

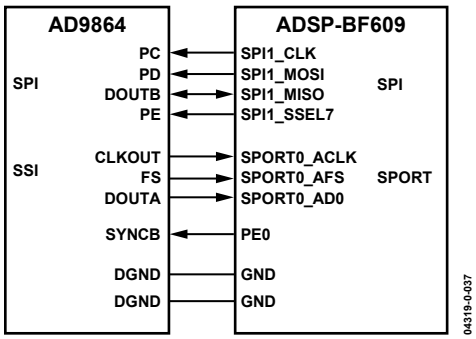


Figure 38. Example of AD9864 and ADSP-BF609 Interface

POWER CONTROL

To allow power consumption to be minimized, the AD9864 possesses numerous SPI programmable power-down and bias control bits. The AD9864 powers up with all of its functional blocks placed into a standby state, that is, STBY register default is 0xFF. Each major block can then be powered up by writing a 0 to the appropriate bit of the STBY register. This scheme provides the greatest flexibility for configuring the IC to a specific application as well as for tailoring the power-down and wake-up characteristics of the IC. Table 16 summarizes the function of each of the STBY bits. Note that when all the blocks are in standby, the master reference circuit is also put into standby, and therefore the current is reduced further by 0.4 mA.

Table 16. Standby Control Bits

STBY Bit	Effect	Current Reduction (mA)[1]	Wake-Up Time (ms)
7: REF	Voltage reference off; all biasing shut down.	0.6	<0.1 (C_{REF} = 4.7 nF)
6: LO	LO synthesizer off, IOUTL three-state.	1.2	See Note 2
5: CKO	Clock oscillator off.	1.1	See Note 2
4: CK	Clock synthesizer off, IOUTC three-state. Clock buffer off if ADC is off.	1.3	See Note 2
3: GC	Gain control DAC OFF. GCP and GCN three-state.	0.2	Depends on C_{GC}
2: LNAMX	LNA and mixer off. CXVM, CXVL, and CXIF three-state.	8.2	<2.2
1: Unused			
0: ADC	ADC off; clock buffer off if CLK synthesizer off; VCM three-state; clock to the digital filter halted; digital outputs static.	9.2	<0.1

[1] When all blocks are in standby, the master reference circuit is also put into standby, and thus the current is further reduced by 0.4 mA.
[2] Wake-up time is dependent on programming and/or external components.

LO SYNTHESIZER

The LO synthesizer shown in Figure 39 is a fully programmable phase-locked loop (PLL) capable of 6.25 kHz resolution at input frequencies up to 300 MHz and reference clocks of up to 26 MHz. It consists of a low noise, digital, phase-frequency detector (PFD), a variable output current charge pump (CP), a 14-bit reference divider, programmable A and B counters, and a dual-modulus 8/9 prescaler.

The A (3-bit) and B (13-bit) counters, in conjunction with the dual 8/9 modulus prescaler, implement an N divider with N = 8 × B + A. In addition, the 14-bit reference counter (R counter) allows selectable input reference frequencies, f_{REF}, at the PFD input. A complete PLL can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO).

The A, B, and R counters can be programmed via the following registers: LOA, LOB, and LOR. The charge pump output current is programmable via the LOI register from 0.625 mA to 5.0 mA using the equation

$$I_{PUMP} = (LOI + 1) \times 0.625 \text{ mA} \quad (2)$$

An on-chip fast acquire function (enabled by the LOF bit) automatically increases the output current for faster settling during channel changes. The synthesizer can also be disabled using the LO standby bit located in the STBY register.

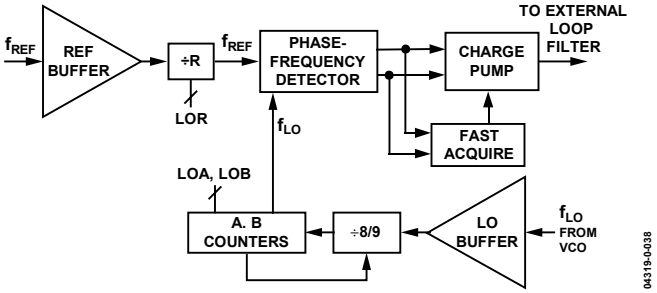


Figure 39. LO Synthesizer

The LO (and CLK) synthesizer works in the following manner. The externally supplied reference frequency, f_{REF}, is buffered and divided by the value held in the R counter. The internal f_{REF} is then compared to a divided version of the VCO frequency, f_{LO}. The phase/frequency detector provides up and down pulses whose widths vary, depending upon the difference in phase and frequency of the input signals of the detector. The up/down pulses control the charge pump, making current available to charge the external low-pass loop filter when there is a discrepancy between the inputs of the PFD. The output of the low-pass filter feeds an external VCO whose output frequency, f_{LO}, is driven such that its divided down version, f_{LO}, matches that of f_{REF}, thus closing the feedback loop.

The synthesized frequency is related to the reference frequency and the LO register contents as follows:

$$f_{LO} = (8 \times LOB + LOA)/LOR \times f_{REF} \quad (3)$$

Note that the minimum allowable value in the LOB register is 3, and its value must always be greater than that loaded into LOA.

An example helps to illustrate how the values of LOA, LOB, and LOR can be selected. Consider an application employing a 13 MHz crystal oscillator (f_{REF} = 13 MHz), with the requirement that f_{REF} = 100 kHz and f_{LO} = 143 MHz, that is, high side injection with f_{IF} = 140.75 MHz and f_{CLK} = 18 MSPS. LOR is selected to be 130 so that f_{REF} = 100 kHz. The N-divider factor is 1430, which can be realized by selecting LOB = 178 and LOA = 6.

The stability, phase noise, spur performance, and transient response of the AD9864 LO (and CLK) synthesizers are determined by the external loop filter, the VCO, the N-divide factor, and the reference frequency, f_{REF}. A good overview of the theory and practical implementation of PLL synthesizers (featured as a 3-part series in Analog Dialogue) can be found on the Analog Devices website. A free software copy of the Analog Devices ADIsimPLL, a PLL synthesizer simulation tool, is also available at www.analog.com. Note that the ADF4112 can be used as a close approximation to the LO synthesizer of the AD9864 when using this software tool.

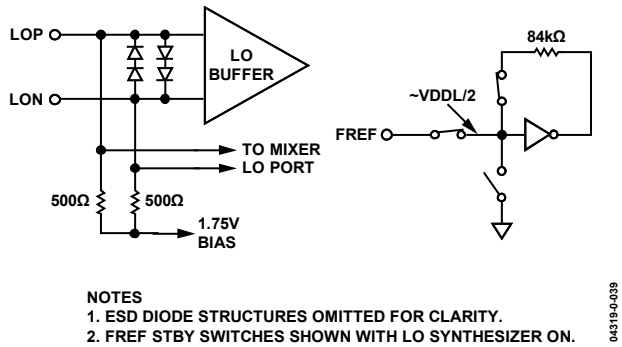


Figure 40. Equivalent Input of LO and REF Buffers

Figure 40 shows the equivalent input structures of the LO and REF buffers of the synthesizers (excluding the ESD structures). The LO input is fed to the buffer of the LO synthesizer as well as the LO port of the AD9864 mixer. Both inputs are self biasing and thus tolerate ac-coupled inputs. The LO input can be driven with a single-ended or differential signal. Single-ended, dc-coupled inputs ensure sufficient signal swing above and below the common-mode bias of the LO and REF buffers (that is, 1.75 V and VDDL/2). Note that the f_{REF} input is slew rate dependent and must be driven with input signals exceeding 7.5 V/µs to ensure proper synthesizer operation. If this condition cannot be met, an external logic gate can be inserted prior to the f_{REF} input to square up the signal, thus allowing an f_{REF} input frequency approaching dc.

Fast Acquire Mode

The fast acquire circuit attempts to boost the output current when the phase difference between the divided-down LO (that is, f_{LO}) and the divided-down reference frequency (that is, f_{REF}) exceeds the threshold determined by the LOFA register. The LOFA register specifies a divisor for the f_{REF} signal that determines the period (T) of this divided-down clock. This period defines the time interval used in the fast acquire algorithm to control the charge pump current.

Assume that the nominal charge pump current is at its lowest setting (LOI = 0), and denote this minimum current by I_0. When the output pulse from the phase comparator exceeds T, the output current for the next pulse is $2I_0$. When the pulse is wider than 2T, the output current for the next pulse is $3I_0$, and so forth, up to eight times the minimum output current. If the nominal charge pump current is more than the minimum value (LOI > 0), the preceding rule is only applied if it results in an increase in the instantaneous charge pump current. If the charge pump current is set to its lowest value (LOI = 0) and the fast acquire circuit is enabled, the instantaneous charge pump current never falls below $2I_0$ when the pulse width is less than T. Thus, the charge pump current when fast acquire is enabled is given by

$$I_{PUMP\text{-}FA} = I_0 \times [1 = \text{Max}(1, LOI, Pulse\ Width/T)] \quad (4)$$

The recommended setting for LOFA is LOR/16. Choosing a larger value for LOFA increases T. Thus, for a given phase difference between the LO input and the f_{REF} input, the instantaneous charge pump current is less than that available for a LOFA value of LOR/16. Similarly, a smaller value for LOFA decreases T, making more current available for the same phase difference. In other words, a smaller value of LOFA enables the synthesizer to settle faster in response to a frequency hop than a large LOFA value. Take care to choose a value for LOFA that is large enough (values greater than 4 are recommended) to prevent the loop from oscillating back and forth in response to a frequency hop.

Table 17. SPI Registers Associated with LO Synthesizer

Address (Hex)	Bit(s)	Width	Default Value	Name
0x00	[7:0]	1	0xFF	STBY
0x08	[5:0]	6	0x00	LOR [13:8]
0x09	[7:0]	8	0x38	LOR [7:0]
0x0A	[7:5]	3	0x5	LOA
	[4:0]	5	0x00	LOB [12:8]
0x0B	[7:0]	8	0xiD	LOB [7:0]
0x0C	6	1	0	LOF
	5	1	0	LOINV
	[4:2]	3	0x00	LOI
	[1:0]	2	0x00	LOTM
0x0D	[3:0]	4	0x00	LOFA [13:8]
0x0E	[7:0]	8	0x04	LOFA [7:0]

CLOCK SYNTHESIZER

The clock synthesizer is a fully programmable integer-N PLL capable of supporting input clock and reference frequencies up to 26 MHz. It is similar to the LO synthesizer described in Figure 39 with the following exceptions:

- It does not include an 8/9 prescaler nor an A counter.
- It includes a negative-resistance core that, when used in conjunction with an external LC tank and varactor, serves as the VCO.

The 14-bit reference counter and 13-bit N-divider counter can be programmed via the CKR and CKN registers. The clock frequency, f_{CLK}, is related to the reference frequency by the equation

$$f_{CLK} = (CKN/CKR \times f_{REF}) \quad (5)$$

The charge pump current is programmable via the CKI register from 0.625 mA to 5.0 mA using the equation

$$I_{PUMP} = (CKI + 1) \times 0.625\ \text{mA} \quad (6)$$

The fast acquire subcircuit of the charge pump is controlled by the CKFA register in the same manner the LO synthesizer is controlled by the LOFA register. An on-chip lock detect function (enabled by the CKF bit) automatically increases the output current for faster settling during channel changes. The synthesizer may also be disabled using the CK standby bit located in the STBY register.

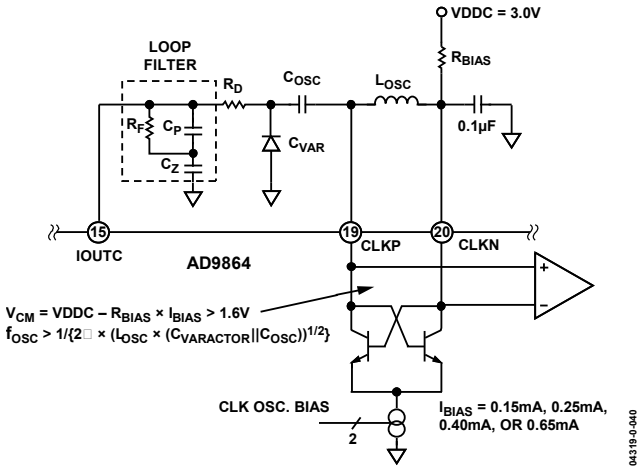


Figure 41. External Loop Filter, Varactor, and LC Tank Required to Realize a Complete Clock Synthesizer

The AD9864 clock synthesizer circuitry includes a negative resistance core so that only an external LC tank circuit with a varactor is needed to realize a voltage controlled clock oscillator (VCO). Figure 41 shows the external components required to complete the clock synthesizer along with the equivalent input circuitry of the CLK input. The resonant frequency of the VCO is approximately determined by L_{OSC} and the series equivalent capacitance of C_{OSC} and C_{VAR}. As a result, L_{OSC}, C_{OSC}, and C_{VAR} must be selected to provide a sufficient tuning range to ensure both proper start-up oscillation and locking of the clock synthesizer. Both the C_{OSC} and L_{OSC} values must have ±5% tolerance along with L_{OSC} having a Q > 20 at the desired clock frequency.

The bias, I_{BIAS}, of the negative-resistance core has four programmable settings. The lower equivalent Q of the LC tank circuit may require a higher bias setting of the negative resistance core to ensure proper oscillation. Select R_{BIAS} so that the common-mode voltage at CLKP and CLKN is approximately 1.6 V. The synthesizer may be disabled via the CK standby bit to allow the user to employ an external synthesizer and/or VCO in place of those resident on the IC. Note that if an external CLK source or VCO is used, the clock oscillator must be disabled via the CKO standby bit.

The phase noise performance of the clock synthesizer is dependent on several factors, including the CLK oscillator I_{BIAS} setting, charge pump setting, loop filter component values, and internal f_{REF} setting. Figure 42 and Figure 43 show how the measured phase noise attributed to the clock synthesizer varies (relative to an external f_{CLK}) as a function of the I_{BIAS} setting and charge pump setting for a −31 dBm IFIN signal at 73.35 MHz with an external LO signal at 71.1 MHz. Figure 42 shows that the optimum phase noise is achieved with the highest I_{BIAS} (CKO) setting, while Figure 43 shows that the higher charge pump values provide the optimum performance for the given loop filter configuration. The AD9864 clock synthesizer and oscillator were set up to provide an f_{CLK} of 18 MHz from an external f_{REF} of 16.8 MHz. The following external component values were selected for the synthesizer: R_F = 390 Ω, R_D = 2 kΩ, C_Z = 0.68 µF, C_P = 0.1 µF, C_{OSC} = 91 pF, L_{OSC} = 1.2 µH, and C_{VAR} = Toshiba 1SV228 varactor.

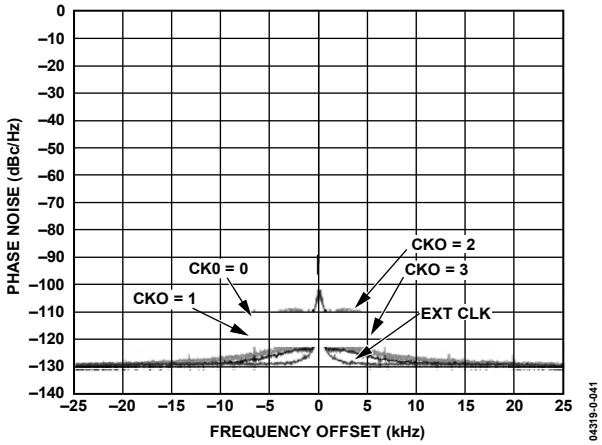


Figure 42. CLK Phase Noise vs. I_{BIAS} Setting (CKO); IF = 73.35 MHz, IF = 71.1 MHz, IFIN = −31 dBm, f_{CLK} = 18 MHz, f_{REF} = 16.8 MHz; CLK SYN Settings: CKI = 7, CLR = 56, and CLN = 60 with f_{REF} = 300 kHz

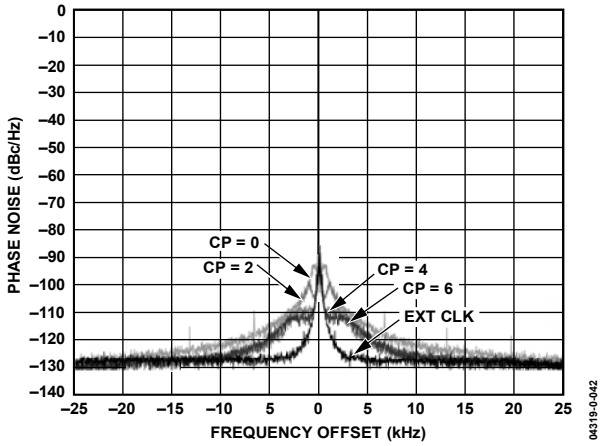


Figure 43. CLK Phase Noise vs. I_{BIAS} Setting (CKO); IF = 73.35 MHz, IF = 71.1 MHz, IFIN = −31 dBm, f_{CLK} = 18 MHz, f_{REF} = 16.8 MHz; CLK SYN Settings: CKO Bias = 3, CKR = 56, and CKN = 60 with f_{REF} = 300 kHz

Table 18. SPI Registers Associated with CLK Synthesizer

Address (Hex)	Bit(s)	Width	Default Value	Name
0x00	[7:0]	8	0xFF	STBY
0x01	[3:2]	2	0x00	CKOB
0x10	[5:0]	6	0x00	CKR [13:8]
0x11	[7:0]	8	0x38	CKR [7:0]
0x12	[4:0]	5	0x00	CKN [12:8]
0x13	[7:0]	8	0x3C	CKN [7:0]
0x14	6	1	0	CKF
	5	1	0	CKINV
	[4:2]	3	0x00	CKI
	[1:0]	1	0x00	CKTM
0x15	[3:0]	4	0x00	CKFA [13:8]
0x16	[7:0]	8	0x04	CKFA [7:0]

IF LNA/MIXER

The AD9864 contains a single-ended LNA followed by a Gilbert type active mixer, shown in Figure 44 with the required external components. The LNA uses negative shunt feedback to set its input impedance at the IFIN pin, thus making it dependent on the input frequency. It can be modeled as approximately 370 Ω||1.4 pF (±20%) below 100 MHz. Figure 45 and Figure 46 show the equivalent input impedance vs. frequency characteristics of the AD9864. The increase in shunt resistance vs. frequency can be attributed to the reduction in bandwidth, thus the amount of negative feedback of the LNA. Note that the input signal into IFIN must be ac-coupled via a 10 nF capacitor because the LNA input is self biasing.

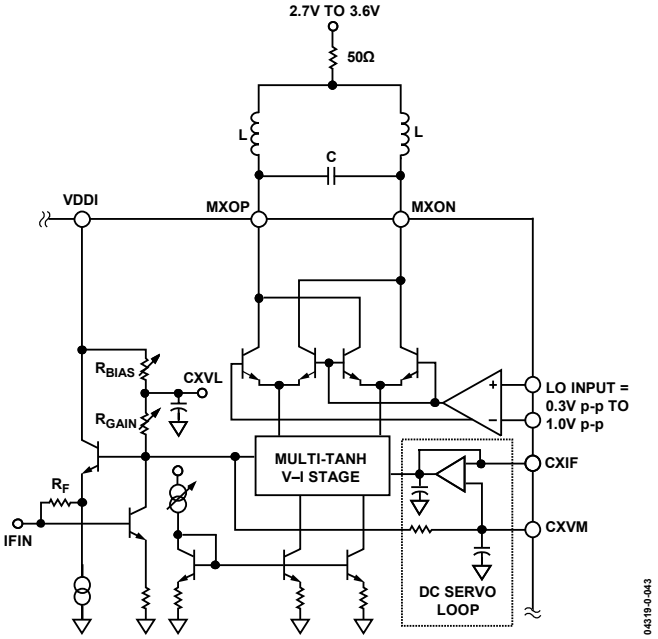


Figure 44. Simplified Schematic of AD9864 LNA/Mixer

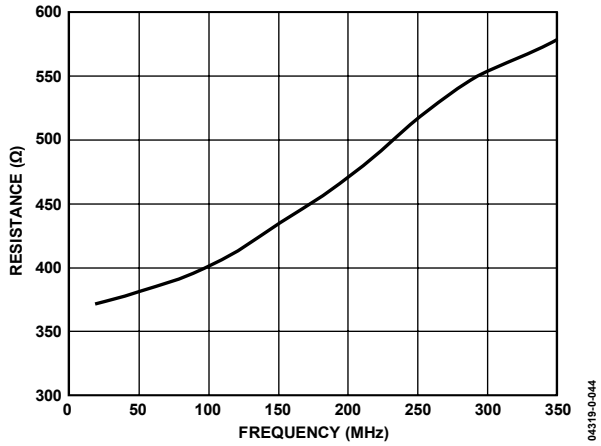


Figure 45. Shunt Input Resistance vs. Frequency of AD9864 IF1 Input

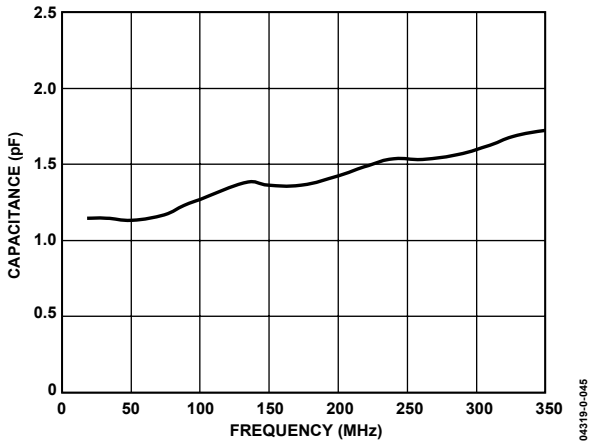


Figure 46. Shunt Capacitance vs. Frequency of AD9864 IF1 Input

The differential LO port of the mixer is driven by the LO buffer stage shown in Figure 44, which can be driven single-ended or differential. Because it is self biasing, the LO signal level can be ac-coupled and range from 0.3 V p-p to 1.0 V p-p with negligible effect on performance. The open-collector outputs of the mixer, MXOP and MXON, drive an external resonant tank consisting of a differential LC network tuned to the IF of the band-pass Σ-Δ ADC, that is, $f_{IF2_ADC} = f_{CLK}/8$. The two inductors provide a dc bias path for the mixer core via a series resistor of 50 Ω, which is included to dampen the common-mode response. The output of the mixer must be ac-coupled to the input of the band-pass Σ-Δ ADC, IF2P, and IF2N via two 100 pF capacitors to ensure proper tuning of the LC center frequency.

The external differential LC tank forms the resonant element for the first resonator of the band-pass Σ-Δ modulator, and so must be tuned to the $f_{CLK}/8$ center frequency of the modulator. The inductors must be chosen such that their impedance at $f_{CLK}/8$ is approximately 140, that is, $L = 180/f_{CLK}$. An accuracy of 20% is considered to be adequate. For example, at f_{CLK} = 18 MHz, L = 10 µH is a good choice. Once the inductors have been selected, the required tank capacitance may be calculated using the relation

$$f_{CLK}/8 = 1/[2 \times \pi \times \sqrt{(2L \times C)}]$$

For example, at f_{CLK} = 18 MHz and L = 10 µH, a capacitance of 250 pF is needed. However, to accommodate an inductor tolerance of ±10%, the tank capacitance must be adjustable from 227 pF to 278 pF. Selecting an external capacitor of 180 pF ensures that even with a 10% tolerance and stray capacitances as high as 30 pF, the total capacitance is less than the minimum value needed by the tank. Extra capacitance is supplied by the AD9864 on-chip programmable capacitor array. Because the programming range of the capacitor array is at least 160 pF, the AD9864 has plenty of range to make up for the tolerances of low cost external components. Note that if f_{CLK} is increased by a factor of 1.44 MHz to 26 MHz so that $f_{CLK}/8$ becomes 3.25 MHz, reducing L and C by approximately the same factor (L = 6.9 µH and C = 120 pF) satisfies the requirements stated previously.

A 16 dB step attenuator is also included within the LNA/mixer circuitry to prevent large signals (that is, > −18 dBm) from overdriving the Σ-Δ modulator. In such instances, the Σ-Δ modulator becomes unstable, thus severely desensitizing the receiver. The 16 dB step attenuator can be invoked by setting the ATTEN bit (Register 0x03, Bit 7), causing the mixer gain to be reduced by 16 dB. The 16 dB step attenuator can be used in applications where a potential target or blocker signal could exceed the IF input clip point. Although the LNA is driven into compression, it may still be possible to recover the desired signal if it is FM. See Table 19 for the gain compression characteristics of the LNA and mixer with the 16 dB attenuator enabled.

Table 19. SPI Registers Associated with LNA/Mixer

Address (Hex)	Bit(s)	Width	Default Value	Name
0x00	[7:0]	8	0xFF	STBY
0x03	7	1	0	ATTEN

BAND-PASS Σ-Δ ADC

The ADC of the AD9864 is shown in Figure 47. The ADC contains a sixth-order, multibit band-pass Σ-Δ modulator that achieves very high instantaneous dynamic range over a narrow frequency band. The loop filter of the band-pass Σ-Δ modulator consists of two continuous-time resonators followed by a discrete time resonator, with each resonator stage contributing a pair of complex poles. The first resonator is an external LC tank, while the second is an on-chip active RC filter. The output of the LC resonator is ac-coupled to the second resonator input via 100 pF capacitors. The center frequencies of these two continuous-time resonators must be tuned to $f_{CLK}/8$ for the ADC to function properly. The center frequency of the discrete time resonator automatically scales with f_{CLK}, thus no tuning is required.

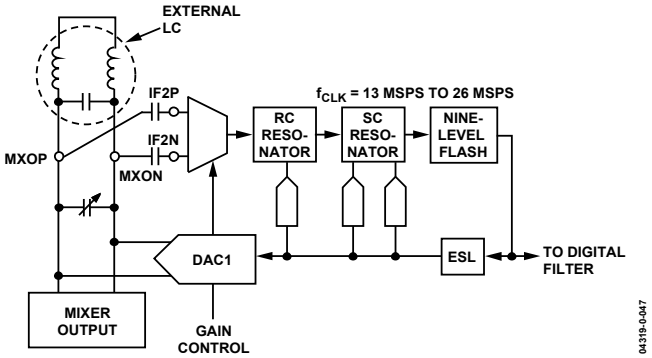


Figure 47. Equivalent Circuit of Sixth-Order Band-Pass Σ-Δ Modulator

Figure 48 shows the measured power spectral density measured at the output of the undecimated band-pass Σ-Δ modulator. Note that the wide dynamic range achieved at the center frequency, $f_{CLK}/8$, is achieved once the LC and RC resonators of the Σ-Δ modulator have been successfully tuned. The out-of-band noise is removed by the decimation filters following quadrature mixer.

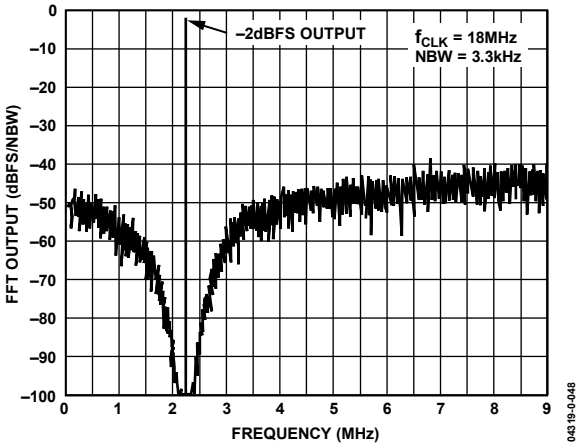


Figure 48. Measured Undecimated Spectral Output of Σ-Δ Modulator ADC with f_{CLK} = 18 MSPS and Noise Bandwidth of 3.3 kHz

The signal transfer function of the AD9864 possesses inherent anti-alias filtering by virtue of the continuous time portions of the loop filter in the band-pass Σ-Δ modulator. Figure 49 illustrates this property by plotting the nominal signal transfer function of the ADC for frequencies up to $2f_{CLK}$. The notches that naturally occur for all frequencies that alias to the $f_{CLK}/8$ pass band are clearly visible. Even at the widest bandwidth setting, the notches are deep enough to provide greater than 80 dB of alias protection. Thus, the wideband IF filtering requirements preceding the AD9864 are determined mostly by the image band of the mixer, which is offset from the desired IF input frequency by $f_{CLK}/4$ (that is, $2 \times f_{CLK}/8$) rather than any aliasing associated with the ADC.

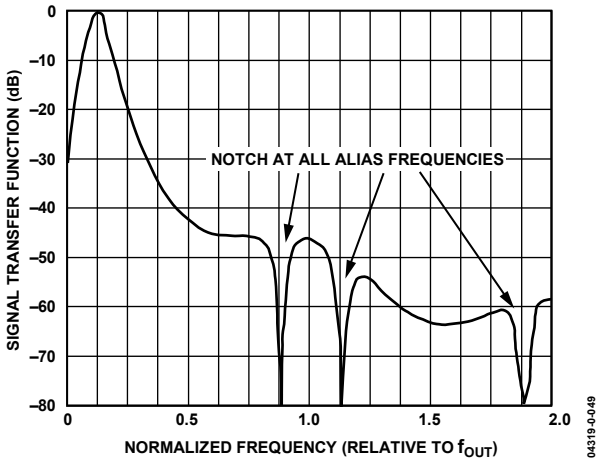


Figure 49. Signal Transfer Function of the Band-Pass Σ-Δ Modulator from 0 f_{CLK} to $2f_{CLK}$

Figure 50 shows the nominal signal transfer function magnitude for frequencies near the $f_{CLK}/8$ pass band. The width of the pass band determines the transfer function droop, but even at the lowest oversampling ratio (48) where the pass band edges are at $\pm f_{CLK}/192$ ($\pm 0.005\ f_{CLK}$), the gain variation is less than 0.5 dB. Also consider the amount of attenuation offered by the signal transfer function near $f_{CLK}/8$ when determining the narrow-band IF filtering requirements preceding the AD9864.

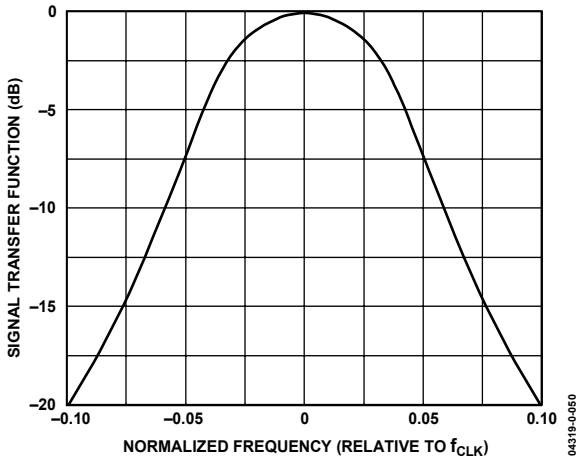


Figure 50. Magnitude of the Signal Transfer Function of the ADC near $f_{CLK}/8$

Tuning of the Σ-Δ modulator's two continuous-time resonators is essential in realizing the full dynamic range of the ADC, and must be performed upon system startup. To facilitate tuning of the LC tank, a capacitor array is internally connected to the MXOP and MXON pins. The capacitance of this array is programmable from 0 pF to 200 pF ± 20% and can be programmed either automatically or manually via the SPI port. The capacitors of the active RC resonator are similarly programmable. Note that the AD9864 can be placed in and out of its standby mode without retuning since the tuning codes are stored in the SPI registers.

When tuning the LC tank, the sampling clock frequency must be stable and the LNA/mixer, LO synthesizer, and ADC must all be placed in standby. Because large LO and IF signals (>−40 dBm) present at the inputs of the AD9864 can corrupt the calibration, these signals must be minimized or disabled during the calibration sequence. Tuning is triggered when the ADC is taken out of standby if the TUNE_LC bit of Register 0x1C has been set. This bit clears when the tuning operation is complete (less than 6 ms). The tuning codes can be read from the 3-bit CAPL1 (0x1D) and the 6-bit CAPL0 (0x1E) registers.

In a similar manner, tuning of the RC resonator is activated if the TUNE_RC bit of Register 0x1C is set when the ADC is taken out of standby. This bit clears when tuning is complete. The tuning code can be read from the CAPR (0x1F) register. Setting both the TUNE_LC and TUNE_RC bits tunes the LC tank and the active RC resonator in succession. During tuning, the ADC is not operational and neither data nor a clock is available from the SSI port.

The following mechanisms prevent the tuning procedure from finishing (that is, Register 0x1C does not clear):

- CLK signal is not present or scaled/biased properly into CLKP (and/or CLKN) pin such that internal clock receiver does not square-up the input clock signal. To determine if the CLK input signal is being received correctly, a clock signal appears at the CLKOUT when the ADC is not in standby mode (Register 0x00), and the CLKOUT buffer is not three-stated (Register 0x18).
- LC resonator fails to resonate during tune operation. Check to see proper values are used for LC tank and that it is connected to MXOP/MXON pins. Also check if 100 pF capacitors are connected between MXOP (MXON) and IF2P (IF2N) pins.
- SYCNB pin is low.
- Capacitor value (between the MXOP/MXON and IF2P/IF2N pins) is larger than 100 pF.

Table 20 lists the recommended sequence of the SPI commands for tuning the ADC, and Table 21 lists all of the SPI registers associated with band-pass Σ-Δ ADC. Note that the recommended sequence includes additional steps for robustness. These steps are additional measures to prevent the back-end ADC from generating an internal unstable signal that locks the state machine, thus preventing resonator tuning. It also allows five attempts to calibrate the resonators. As a further safeguard, the user can save the settings for Register 0x1D, Register 0x1E, and Register 0x1F determined during factory test and reload these settings after five attempts. Note that that the occurrence of this tuning issue is extremely rare among devices shipped to date, and the occurrence among any suspect devices being quite low (<0.1%).

Table 20. Tuning Sequence

Address (Hex)	Value (Hex)	Comments
0x3E	0x47	Disable internal ADC unstable signal. Enable RC Q enhancement. Bypass RC and SC resonators.
0x38	0x01	Enable manual control of feedback DAC
0x39	0x0F	Set DAC to midscale
0x00	0x45	LO synthesizer, LNA/mixer, and ADC are placed in standby.[1]
0x1C	0x03	Set TUNE_LC and TUNE_RC. Wait for CLK to stabilize if CLK synthesizer used.
0x00	0x44	Take the ADC out of standby. Wait for 0x1C to clear (<6 ms).
0x1C	0x00	If 0x1C does not clear, clear 0x1C and make five attempts before exiting loop.
0x38	0x00	Disable manual control of feedback DAC
0x3E	0x00	Re-enable ADC unstable signal. Disable RC Q enhancement. Disable bypass of RC and SC resonators.
0x00	0x40	LNA/mixer (and LO SYN if used) can now be taken out of standby

[1] If external CLK VCO or source is used, the CLK oscillator must also be disabled. Large IF or LO signals can corrupt the calibration; these signals must be disabled during the calibration sequence.

Table 21. SPI Registers Associated with Band-Pass Σ-Δ ADC

Address (Hex)	Value	Width	Default Value	Name
0x00	[7:0]	8	0xFF	STBY
0x1C	1	1	0	TUNE_LC
	0	1	0	TUNE_RC
0x1D	[2:0]	3	0	CAPL1 [2:0]
0x1E	[5:0]	6	0x00	CAPL1 [5:0]
0x1F	[7:0]	8	0x00	CAPR
0x38	0	1	0	DACCR
0x39	[7:0]	8	0x00	DACDATA
0x3E	0	1	0	ADCCR

When the AD9864 is tuned, the noise figure degradation attributed solely to the temperature drift of the LC and RC resonators is minimal. Because the drift of the RC resonator is actually negligible compared to that of the LC resonator, the external L and C components temperature drift characteristics tend to dominate. Figure 51 shows the degradation in noise figure as the product of the LC value is allowed to vary from −12.5% to +12.5%. Note that the noise figure remains relatively constant over a ±3.5% range (±35,000 ppm), suggesting that most applications do not need to be retuned over the operating temperature range.

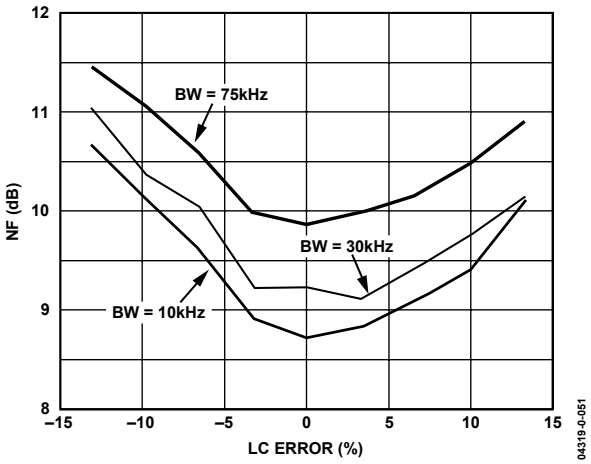


Figure 51. Typical Noise Figure Degradation from L and C Component Drift (f_{CLK} = 18 MSPS, f_{IF} = 73.3501 MHz)

DECIMATION FILTER

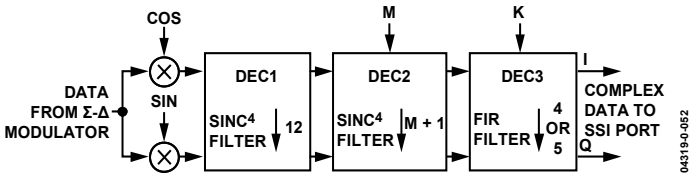


Figure 52. Decimation Filter Architecture

The decimation filter shown in Figure 52 consists of an $f_{CLK}/8$ complex mixer and a cascade of three linear phase FIR filters: DEC1, DEC2, and DEC3. DEC1 downsamples by a factor of 12 using a fourth-order comb filter. DEC2 also uses a fourth-order comb filter, but its decimation factor is set by the M field of Register 0x07. DEC3 is either a decimate-by-5 FIR filter or a decimate-by-4 FIR filter, depending on the value of the K bit within Register 0x07. Thus, the composite decimation factor can be set to either 60 × M or 48 × M for K equal to 0 or 1, respectively.

The output data rate (f_{OUT}) is equal to the modulator clock frequency (f_{CLK}) divided by the decimation factor of the digital filter. Due to the transition region associated with the frequency response of the decimation filter, the decimation factor must be selected so that f_{OUT} is equal to or greater than twice the signal bandwidth, which ensures low amplitude ripple in the pass band along with the ability to provide further application-specific digital filtering prior to demodulation.

Figure 53 shows the response of the decimation filter at a decimation factor of 900 (K = 0, M = 14) and a sampling clock frequency of 18 MHz. In this example, the output data rate (f_{OUT}) is 20 kSPS, with a usable complex signal bandwidth of 10 kHz centered around dc. As this figure shows, the first and second alias bands (occurring at even integer multiples of $f_{OUT}/2$) have the least attenuation but provide at least 88 dB of attenuation. Note that signals falling around frequency offsets that are odd integer multiples of $f_{OUT}/2$ (that is, 10 kHz, 30 kHz, and 50 kHz) fall back into the transition band of the digital filter.

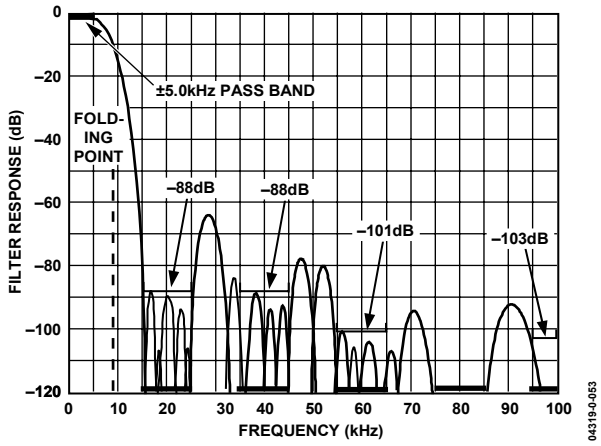


Figure 53. Decimation Filter Frequency Response for f_{OUT} = 20 kSPS (f_{CLK} = 18 MHz, OSR = 900)

Figure 54 shows the response of the decimation filter with a decimation factor of 48 and a sampling clock rate of 26 MHz. The alias attenuation is at least 94 dB and occurs for frequencies at the edges of the fourth alias band. The difference between the alias attenuation characteristics of Figure 53 and those of Figure 54 is due to the fact that the third decimation stage decimates by a factor of 5 for Figure 53 compared with a factor of 4 for Figure 54.

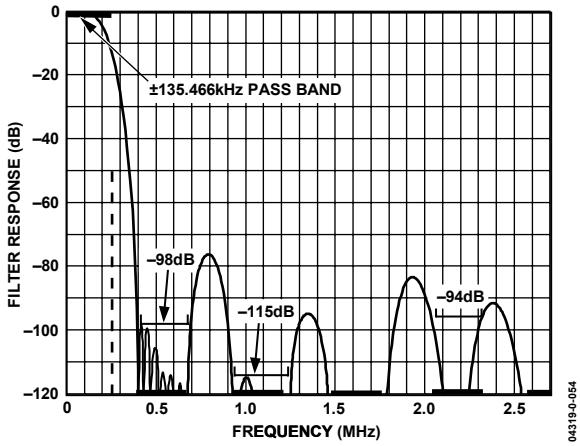


Figure 54. Decimation Filter Frequency Response for f_{OUT} = 541.666 kSPS (f_{CLK} = 26 MHz, OSR = 48)

Figure 55 and Figure 56 show expanded views of the pass band for the two possible configurations of the third decimation filter. When decimating by 60n (K = 0), the pass-band gain variation is 1.2 dB; when decimating by 48n (K = 1), the pass-band gain variation is 0.9 dB. Normalization of full scale at band center is accurate to within 0.14 dB across all decimation modes. Figure 57 and Figure 58 show the folded frequency response of the decimator for K = 0 and K = 1, respectively.

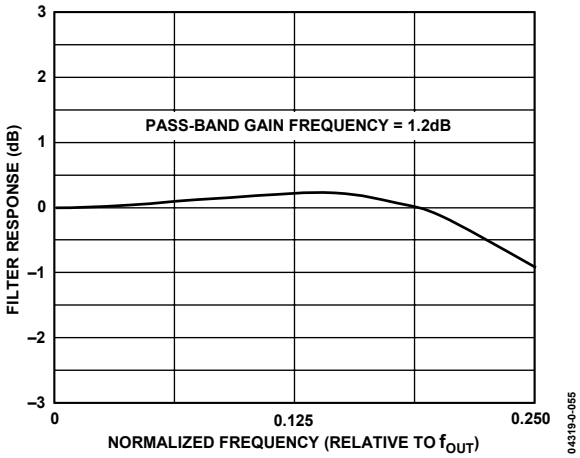


Figure 55. Pass-Band Frequency Response of the Decimator for K = 0

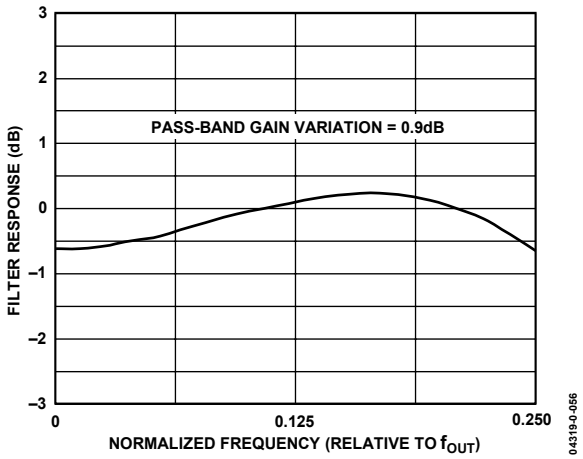


Figure 56. Pass-Band Frequency Response of the Decimator for K = 1

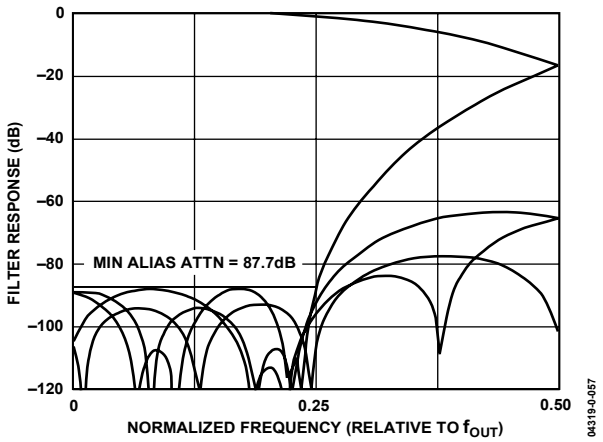


Figure 57. Folded Decimator Frequency Response for K = 0

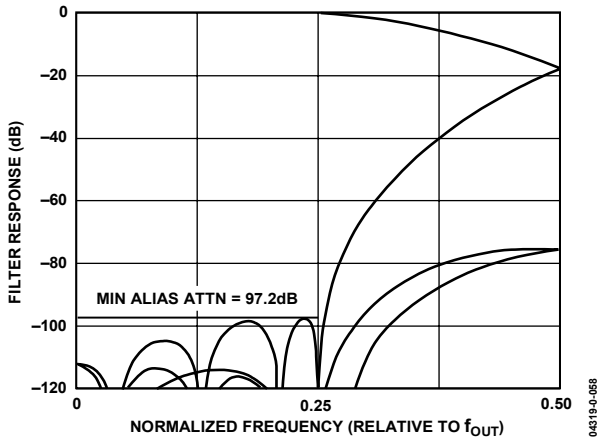


Figure 58. Folded Decimator Frequency Response for K = 1

VARIABLE GAIN AMPLIFIER OPERATION WITH AUTOMATIC GAIN CONTROL

The AD9864 contains both a variable gain amplifier (VGA) and a digital VGA (DVGA) along with all of the necessary signal estimation and control circuitry required to implement automatic gain control (AGC), as shown in Figure 59. The AGC control circuitry provides a high degree of programmability, allowing users to optimize the AGC response as well as the dynamic range of the AD9864 for a given application. The VGA is programmable over a 12 dB range and implemented within the ADC by adjusting its full-scale reference level. Increasing the full scale of the ADC is equivalent to attenuating the signal. An additional 12 dB of digital gain range is achieved by scaling the output of the decimation filter in the DVGA. Note that a slight increase in the supply current (0.67 mA) is drawn from VDDI and VDDF as the VGA changes from 0 dB to 12 dB attenuation.

The purpose of the VGA is to extend the usable dynamic range of the AD9864 by allowing the ADC to digitize a desired signal over a large input power range as well as recover a low level signal in the presence of larger unfiltered interferers without saturating or clipping the ADC. The DVGA is most useful in extending the dynamic range in narrow-band applications requiring a 16-bit I and Q data format. In these applications, quantization noise resulting from internal truncation to 16 bits as well as external 16-bit fixed point post processing can degrade the effective noise figure of the AD9864 by 1 dB or more.

The DVGA is enabled by writing a 1 to the AGCV field. The VGA (and the DVGA) can operate in either a user controlled variable gain mode or automatic gain control (AGC) mode. It is worth noting that the VGA imparts negligible phase error upon the desired signal as its gain is varied over a 12 dB range. This is due to the bandwidth of the VGA being far greater than the down converted desired signal (centered about $f_{CLK}/8$) and remaining relatively independent of gain setting. As a result, phase modulated signals experience minimal phase error as the AGC varies the VGA gain while tracking an interferer or the desired signal under fading conditions. Note that the envelope of the signal is still affected by the AGC settings.

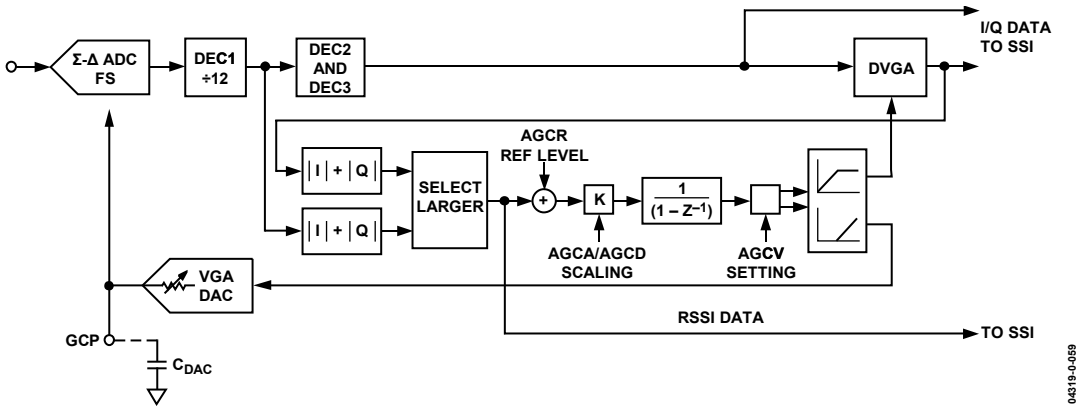


Figure 59. Functional Block Diagram of VGA and AGC

Variable Gain Control

The variable gain control is enabled by setting the AGCR field of Register 0x06 to 0. In this mode, the gain of the VGA (and the DVGA) can be adjusted by writing to the 16-bit AGCG register. The maximum update rate of the AGCG register via the SPI port is $f_{CLK}/240$. The MSB of this register is the bit that enables 16 dB of attenuation in the mixer. This feature allows the AD9864 to cope with large level signals beyond the VGA range (that is, > −18 dBm at LNA input) to prevent overloading of the ADC.

The lower 15 bits specify the attenuation in the remainder of the signal path. If the DVGA is enabled, the attenuation range is from −12 dB to +12 dB because the DVGA provides 12 dB of digital gain. In this case, all 15 bits are significant. However, with the DVGA disabled, the attenuation range extends from 0 dB to 12 dB and only the lower 14 bits are useful. Figure 60 shows the relationship between the amount of attenuation and the AGC register setting for both cases.

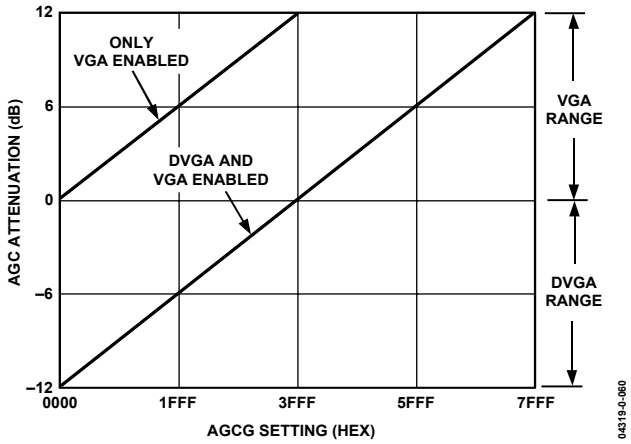


Figure 60. AGC Gain Range Characteristics vs. AGCG Register Setting With and Without DVGA Enabled

Referring to Figure 59, the gain of the VGA is set by an 8-bit control DAC that provides a control signal to the VGA appearing at the gain control pin (GCP). For applications implementing automatic gain control, the output resistance of the DAC can be reduced by a factor of 9 to decrease the attack time of the AGC response for faster signal acquisition. An external capacitor, CDAC, from GCP to analog ground is required to smooth the output of the DAC each time it updates as well as to filter wideband noise. Note that CDAC, in combination with the programmable output resistance of the DAC, sets the −3 dB bandwidth and time constant associated with this RC network.

A linear estimate of the received signal strength is performed at the output of the first decimation stage (DEC1) and output of the DVGA (if enabled), as discussed in the AGC section. This data is available as a 6-bit RSSI field within an SSI frame with 60 corresponding to a full-scale signal for a given AGC attenuation setting. The RSSI field is updated at $f_{CLK}/60$ and can be used with the 8-bit attenuation field (or AGCG attenuation setting) to determine the absolute signal strength. Note that the RSSI data must be post filtered to remove the ac ripple component that is dependent on the frequency offset relative to the IF frequency.

The accuracy of the mean RSSI reading (relative to the IF input power) depends on the input signal's frequency offset relative to the IF frequency because both the response of the DEC1 filter as well as the signal transfer function of the ADC attenuate the downconverted signal level of the mixer, centered at $f_{CLK}/8$. As a result, the estimated signal strength of input signals falling within proximity to the IF is reported accurately, while those signals at increasingly higher frequency offsets incur larger measurement errors. Figure 61 shows the normalized error of the RSSI reading as a function of the frequency offset from the IF frequency. Note that the significance of this error becomes apparent when determining the maximum input interferer (or blocker) levels with the AGC enabled.

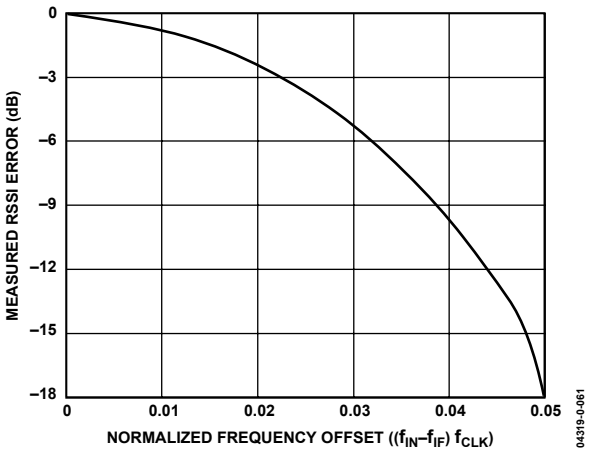


Figure 61. Normalized RSSI Error vs. Normalized IF Frequency Offset

Automatic Gain Control (AGC)

The gain of the VGA (and DVGA) is automatically adjusted when the AGC is enabled via the AGCR field of Register 0x06. In this mode, the gain of the VGA is continuously updated at $f_{CLK}/60$ in an attempt to ensure that the maximum analog signal level into the ADC does not exceed the ADC clip level and that the rms output level of the ADC is equal to a programmable reference level. With the DVGA enabled, the AGC control loop also attempts to minimize the effects of 16-bit truncation noise prior to the SSI output by continuously adjusting the gain of the DVGA to ensure maximum digital gain while not exceeding the programmable reference level.

This programmable level can be set at 3 dB, 6 dB, 9 dB, 12 dB, and 15 dB below the ADC saturation (clip) level by writing values from 1 to 5 to the 3-bit AGCR field. Note that the ADC clip level is defined to be 2 dB below its full scale (−18 dBm at the LNA input for a matched input and maximum attenuation). If AGCR is 0, automatic gain control is disabled. Because clipping of the ADC input degrades the SNR performance, the reference level must also take into consideration the peak-to-rms characteristics of the target (or interferer) signals.

Referring again to Figure 59, the majority of the AGC loop operates in the discrete time domain. The sample rate of the loop is $f_{CLK}/60$; therefore, registers associated with the AGC algorithm are updated at this rate. The number of overload and ADC reset occurrences within the final I/Q update rate of the AD9864, as well as the AGC value (8 MSB), can be read from the SSI data upon proper configuration.

The AGC performs digital signal estimation at the output of the first decimation stage (DEC1) as well as the DVGA output that follows the last decimation stage (DEC3). The rms power of the I and Q signal is estimated by the equation

$$\text{Xest}[n] = \text{Abs}(\text{I}[n] + \text{Abs}(\text{Q}[n]) \quad (7)$$

Signal estimation after the first decimation stage allows the AGC to cope with out-of-band interferers and in-band signals that could otherwise overload the ADC. Signal estimation after the DVGA allows the AGC to minimize the effects of the 16-bit truncation noise.

When the estimated signal level falls within the range of the AGC, the AGC loop adjusts the VGA (or DVGA) attenuation setting so that the estimated signal level is equal to the programmed level specified in the AGCR field. The absolute signal strength can be determined from the contents of the ATTN and RSSI field that is available in the SSI data frame when properly configured. Within this AGC tracking range, the 6-bit value in the RSSI field remains constant while the 8-bit ATTN field varies according to the VGA/DVGA setting. Note that the ATTN value is based on the 8 MSB contained in the AGCG field of Register 0x03 and Register 0x04.

A description of the AGC control algorithm and the user adjustable parameters follows. First, consider the case where the in-band target signal is bigger than all out-of-band interferers and the DVGA is disabled. With the DVGA disabled, a control loop based only on the target signal power measured after DEC1 is used to control the VGA gain, and the target signal is tracked to the programmed reference level. If the signal is too large, the attenuation is increased with a proportionality constant determined by the AGCA setting. Large AGCA values result in large gain changes, thus rapid tracking of changes in signal strength. If the target signal is too small relative to the reference level, the attenuation is reduced; however, now the proportionality constant is determined by both the AGCA and AGCD settings. The AGCD value is effectively subtracted from AGCA, so a large AGCD results in smaller gain changes and thus slower tracking of fading signals.

The 4-bit code in the AGCA field sets the raw bandwidth of the AGC loop. With AGCA = 0, the AGC loop bandwidth is at its minimum of 50 Hz, assuming f_{CLK} = 18 MHz. Each increment of AGCA increases the loop bandwidth by a factor of √2; thus the maximum bandwidth is 9 kHz. A general expression for the attack bandwidth is

$$BW_A = 50 \times (f_{CLK}/18\text{ MHz}) \times 2^{(AGCA/2)}\text{ Hz} \quad (8)$$

Assuming that the loop dynamics are essentially those of a single-pole system, the corresponding attack time is

$$t_{ATTACK} = 2.2/(100 \times \pi \times 2^{(AGCA/2)}) = 35/BW_A \quad (9)$$

The 4-bit code in the AGCD field sets the ratio of the attack time to the decay time in the amplitude estimation circuitry. When AGCD is zero, this ratio is one. Incrementing AGCD multiplies the decay time constant by 21/2, allowing a 180:1 range in the decay time relative to the attack time. The decay time may be computed from

$$t_{DECAY} = t_{ATTACK} \times 2^{(AGCD/2)} \quad (10)$$

Figure 62 shows the AGC response to a 30 Hz pulse-modulated IF burst for different AGCA and AGCD settings. The 3-bit value in the AGCO field determines the amount of attenuation added in response to a reset event in the ADC. Each increment in AGCO doubles the weighting factor. At the highest AGCO setting, the attenuation changes from 0 dB to 12 dB in

approximately 10 µs, while at the lowest setting the attenuation changes from 0 dB to 12 dB in approximately 1.2 ms. In both cases, assume that f_{CLK} = 18 MHz. Figure 63 shows the AGC attack time response for different AGCO settings.

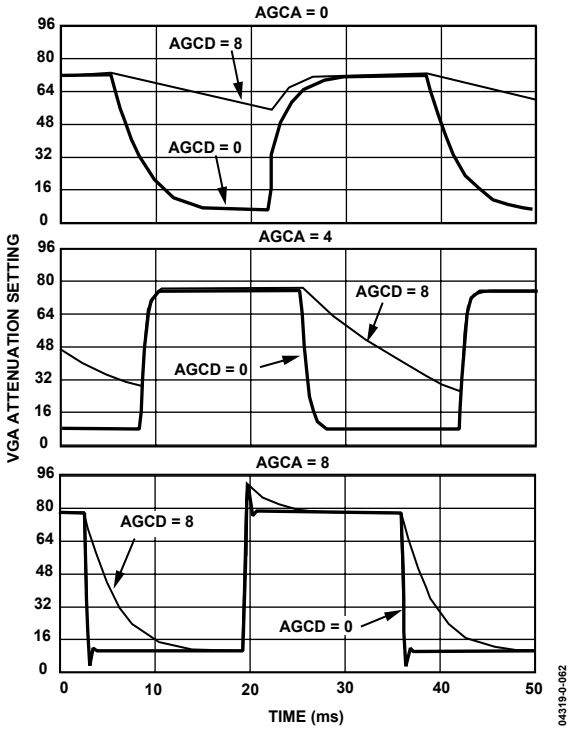


Figure 62. AGC Response for Different AGCA and AGCD Settings with f_{CLK} = 18 MSPS, f_{CLKOUT} = 20 kSPS, Decimate by 900, and AGCO = 0

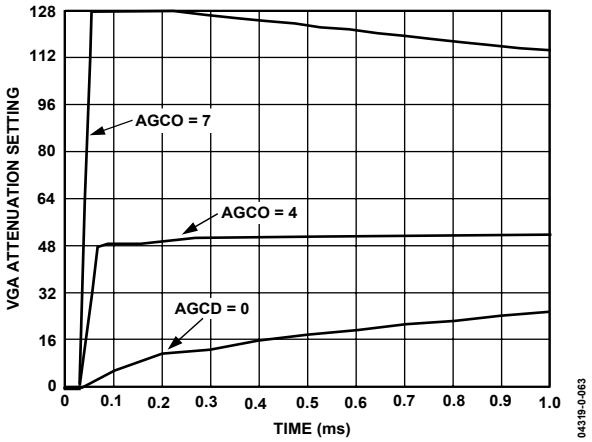


Figure 63. AGC Response for Different AGCO Settings with f_{CLK} = 18 MSPS, f_{CLKOUT} = 300 kSPS, Decimate by 60 and AGCA = AGCD = 0

Lastly, the AGCF bit reduces the DAC source resistance by at least a factor of 10, which facilitates fast acquisition by lowering the RC time constant that is formed with the external capacitors connected from the GCP pin to ground (GCN pin). For an overshoot-free step response in the AGC loop, choose the capacitor connected from the GCP pin to the GCN ground pin so that the RC time constant is less than one quarter of the raw loop.

Specifically,

$$RC < 1/(8\pi BW) \quad (11)$$

where:
R is the resistance between the GCP pin and ground (72.5 kΩ ±30% if AGCF = 0, < 8 kΩ if AGCF = 1).
BW is the raw loop bandwidth.

Note that with C chosen at this upper limit, the loop bandwidth increases by approximately 30%.

Now consider the case described previously but with the DVGA enabled to minimize the effects of 16-bit truncation. With the DVGA enabled, a control loop based on the larger of the two estimated signal levels (that is, the output of DEC1 and DVGA) controls the DVGA gain. The DVGA multiplies the output of the decimation filter by a factor of 1 to 4 (that is, 0 dB to 12 dB). When signals are small, the DVGA gain is 4 and the 16-bit output is extracted from the 24-bit data produced by the decimation filter by dropping 2 MSB and taking the next 16 bits. As signals become larger, the DVGA gain decreases to the point where the DVGA gain is 1 and the 16-bit output data is simply the 16 MSB of the internal 24-bit data. As signals become even larger, attenuation is accomplished by the normal method of increasing the full scale of the ADC.

The extra 12 dB of gain range provided by the DVGA reduces the input-referred truncation noise by 12 dB and makes the data more tolerant of LSB corruption within the DSP. The price paid for this extension to the gain range is that the start of AGC action is 12 dB lower and that the AGC loop becomes unstable if its bandwidth is set too wide. The latter difficulty results from the large delay of the decimation filters, DEC2 and DEC3, when the user implements a large decimation factor. As a result, given the option, the use of 24-bit data is preferable to using the DVGA. Figure 64 indicates which AGCA values are reasonable for various decimation factors (DEC FAC). The white cells indicate that the (decimation factor/AGCA) combination works well; the light gray cells indicate ringing and an increase in the AGC settling time; and the dark gray cells indicate that the combination results in instability or near instability in the AGC loop. Setting AGCF = 1 improves the time-domain behavior at the expense of increased spectral spreading.

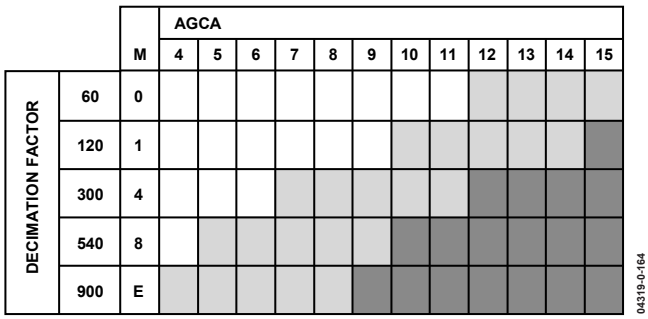


Figure 64. AGCA Limits when DVGA is Enabled

Finally, consider the case of a strong out-of-band interferer (that is, −18 dBm to −32 dBm for matched IF input) that is larger than the target signal and large enough to be tracked by the control loop based on the output of the DEC1. The ability of the control loop to track this interferer and set the VGA attenuation to prevent clipping of the ADC is limited by the accuracy of the digital signal estimation occurring at the output of DEC1. The accuracy of the digital signal estimation is a function of the frequency offset of the out-of-band interferer relative to the IF frequency as shown in Figure 61. Interferers at increasingly higher frequency offsets incur larger measurement errors, potentially causing the control loop to inadvertently reduce the amount of VGA attenuation that may result in clipping of the ADC. Figure 65 shows the maximum measured interferer signal level versus the normalized IF offset frequency (relative to f_{CLK}) tolerated by the AD9864 relative to its maximum target input signal level (0 dBFS = −18 dBm). Note that the increase in allowable interferer level occurring beyond 0.04 × f_{CLK} results from the inherent signal attenuation provided by the signal transfer function of the ADC.

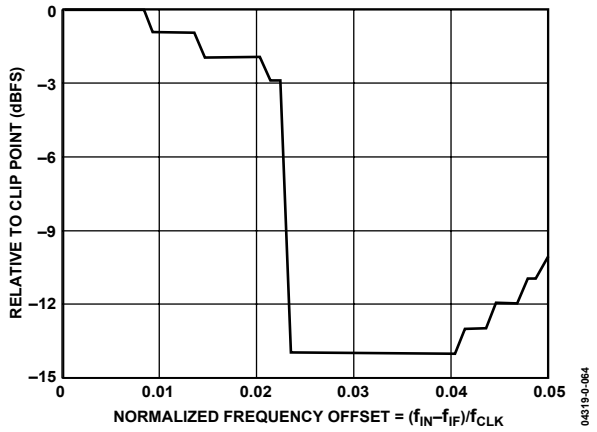


Figure 65. Maximum Interferer (or Blocker) Input Level vs. Normalized IF Frequency Offset

Table 22. SPI Registers Associated with AGC

Address (Hex)	Bit(s)	Width	Default Value	Name
0x03	7	1	0	ATTEN
	[6:0]	7	0x00	AGCG [14:8]
0x04	[7:0]	8	0x00	AGCG [7:0]
0x05	[7:4]	4	0	AGCA
	[3:0]	4	0x00	AGCD
0x06	7	1	0	AGCV
	[6:4]	3	0x00	AGCO
	3	1	0	AGCF
	[2:0]	3	0x00	AGCR

System Noise Figure (NF) vs. VGA (or AGC) Control

The system noise figure of the AD9864 is a function of the ACG attenuation and output signal bandwidth. Figure 66 plots the nominal system NF as a function of the AGC attenuation for both narrow-band (20 kHz) and wideband (150 kHz) modes with f_{CLK} = 18 MHz. Also shown on the plot is the SNR that is observed at the output for a −2 dBFS input. The high dynamic range of the ADC within the AD9864 ensures that the system NF increases gradually as the AGC attenuation is increased. In narrow-band (BW = 20 kHz) mode, the system noise figure increases by less than 3 dB over a 12 dB AGC range, while in wideband (BW = 150 kHz) mode, the degradation is approximately 5 dB. Therefore, the highest instantaneous dynamic range for the AD9864 occurs with 12 dB of AGC attenuation, since the AD9864 can accommodate an additional 12 dB peak signal level with only a moderate increase in its noise floor.

As Figure 66 shows, the AD9864 can achieve an SNR in excess of 100 dB in narrow-band applications. To realize the full performance of the AD9864 in such applications, it is recommended that the I/Q data be represented with 24 bits. If 16-bit data is used, the effective system NF increases because of the quantization noise present in the 16-bit data after truncation.

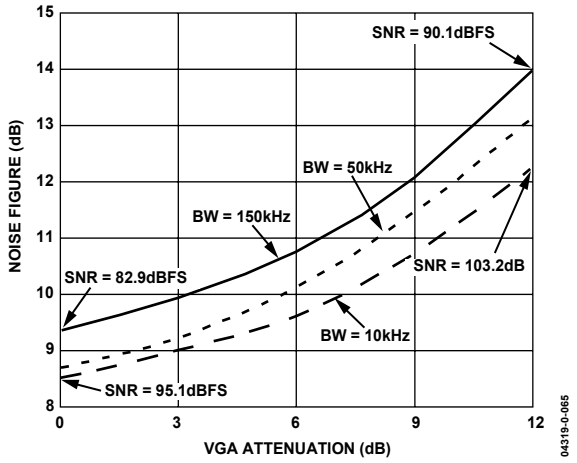


Figure 66. Nominal System Noise Figure and Peak SNR vs. AGCG Setting (f_{IF} = 73.35 MHz, f_{CLK} = 18 MSPS, and 24-bit I/Q Data)

Figure 67 plots the nominal system NF with 16-bit output data as a function of AGC in both narrow-band and wideband mode. In wideband mode, the NF curve is virtually unchanged relative to the 24-bit output data because the output SNR before truncation is always less than the 96 dB SNR that 16-bit data can support. However, in narrow-band mode, where the output SNR approaches or exceeds the SNR that can be supported with 16-bit data, the degradation in system NF is more severe. Furthermore, if the signal processing within the DSP adds noise at the level of an LSB, the system noise figure can be degraded even more than Figure 67 shows. For example, this might occur in a fixed 16-bit DSP whose code is not optimized to process the AD9864 16-bit data with minimal quantization effects. To limit the quantization effects within the AD9864, the 24-bit data

undergoes noise shaping just prior to 16-bit truncation, thus reducing the in-band quantization noise by 5 dB (with 2× oversampling). Therefore, 98.8 dBFS SNR performance is still achievable with 16-bit data in a 10 kHz BW.

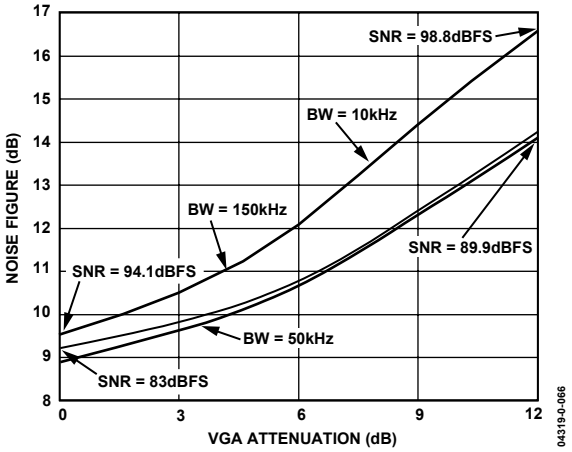


Figure 67. Nominal System Noise Figure and Peak SNR vs. AGCG Setting (f_{IF} = 73.35 MHz, f_{CLK} = 18 MSPS, and 16-bit I/Q Data)

APPLICATIONS CONSIDERATIONS

Frequency Planning

The LO frequency (and/or ADC clock frequency) must be chosen carefully to prevent known internally generated spurs from mixing down along with the desired signal and thus degrading the SNR performance. The major sources of spurs in the AD9864 are the ADC clock and digital circuitry operating at 1/3 of f_{CLK}. Therefore, the clock frequency (f_{CLK}) is the most important variable in determining which LO (and therefore IF) frequencies are viable.

Many applications have frequency plans that take advantage of industry-standard IF frequencies due to the large selection of low cost crystal or SAW filters. If the selected IF frequency and ADC clock rate result in a problematic spurious component, select an alternative ADC clock rate by slightly modifying the decimation factor and CLK synthesizer settings (if used) so that the output sample rate remains the same. Also, applications requiring a certain degree of tuning range must take into consideration the location and magnitude of these spurs when determining the tuning range as well as optimum IF and ADC clock frequency.

Figure 69 plots the measured in-band noise power as a function of the LO frequency for f_{CLK} = 18 MHz and an output signal bandwidth of 150 kHz when no signal is present. Any LO frequency resulting in large spurs must be avoided. As this figure shows, large spurs result when the LO is $f_{CLK}/8$ = 2.25 MHz away from a harmonic of 18 MHz , that is, n $f_{CLK} \pm f_{CLK}/8$. Also problematic are LO frequencies whose odd order harmonics (that is, m × f_{LO}) mix with harmonics of f_{CLK} to $f_{CLK}/8$. This spur mechanism is a result of the mixer being internally driven by a squared-up version of the LO input consisting of the LO frequency and its odd order harmonics. These spur frequencies can be calculated from the relation

$$m \times f_{LO} = (n \pm 1/8) \times f_{CLK} \quad (12)$$

where:
m = 1, 3, 5...
n = 1, 2, 3...

A second source of spurs is a large block of digital circuitry that is clocked at $f_{CLK}/3$. Problematic LO frequencies associated with this spur source are given by

$$f_{LO} = f_{CLK}/3 + n \times f_{CLK} \pm f_{CLK}/8 \quad (13)$$

where n = 1, 2, 3...

Figure 70 shows that omitting the LO frequencies given by Equation 12 for m = 1, 3, and 5, and by Equation 13 accounts for most of the spurs. Some of the remaining low level spurs can be attributed to coupling from the SSI digital output. Therefore, users are also advised to optimize the output bit rate (f_{CLKOUT} via the SSIORD register) and the digital output driver strength to achieve the lowest spurious and noise figure performance for a particular LO frequency and f_{CLK} setting. This is especially the case for particularly narrow-band channels where low level spurs can degrade the sensitivity performance of the AD9864.

Despite the many spurs, sweet spots in the LO frequency are generally wide enough to accommodate the maximum signal bandwidth of the AD9864. As evidence of this property, Figure 68 shows that the in-band noise is quite constant for LO frequencies ranging from 70 MHz to 71 MHz.

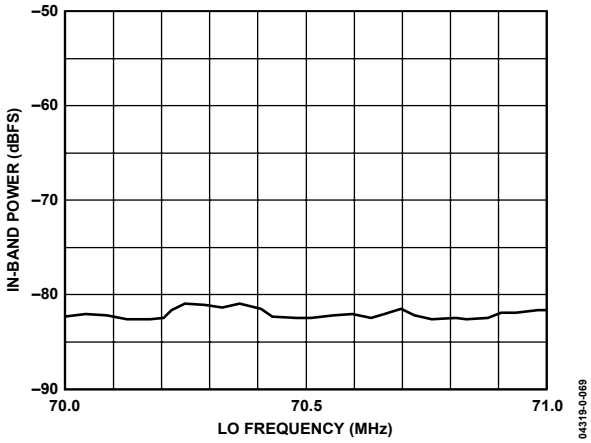


Figure 68. Expanded View from 70 MHz to 71 MHz

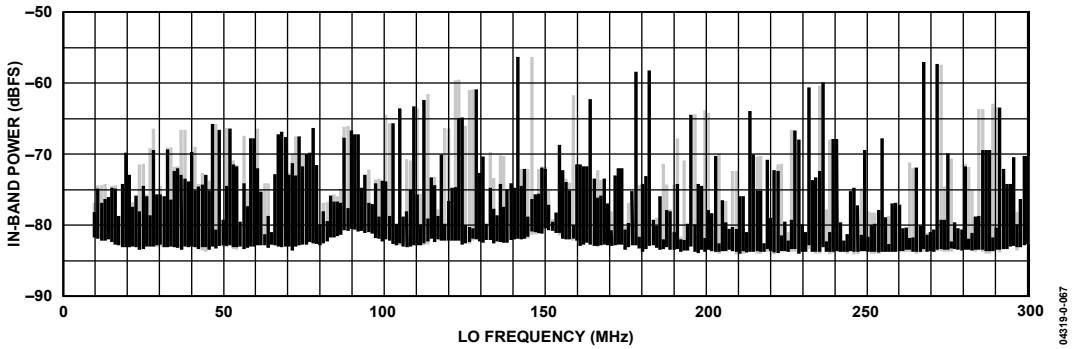


Figure 69. Total In-Band Noise + Spur Power with No Signal Applied as a Function of the LO Frequency (f_{CLK} = 18 MHz and Output Signal Bandwidth = 150 kHz)

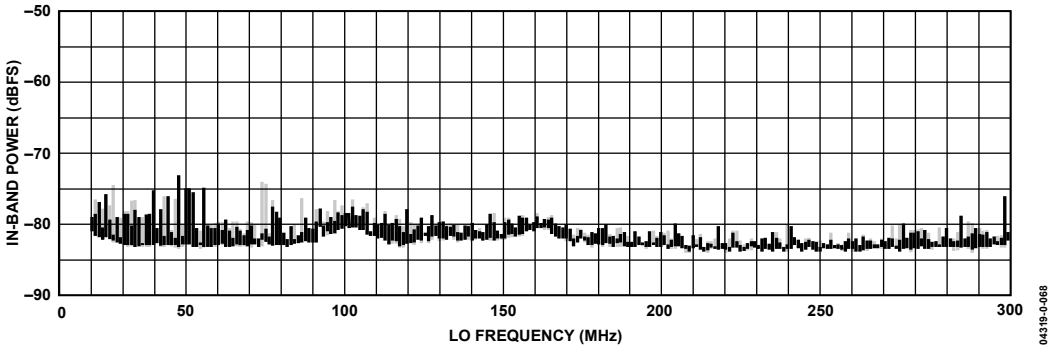


Figure 70. Same as Figure 69 Excluding LO Frequencies Known to Produce Large In-Band Spurs

Spurious Responses

The spectral purity of the LO (including its phase noise) is an important consideration because LO spurs can mix with undesired signals present at the AD9864 IFIN input to produce an in-band response. To demonstrate the low LO spur level introduced within the AD9864, Figure 71 plots the demodulated output power as a function of the input IF frequency for an LO frequency of 71.1 MHz and a clock frequency of 18 MHz.

The two large −10 dBFS spikes near the center of the plot are the desired responses at f_{LO}, ± f_{IF2_ADC}, where $f_{IF2_ADC} = f_{CLK}/8$, that is, at 68.85 MHz and 73.35 MHz. LO spurs at $f_{LO} \pm f_{SPUR}$ result in spurious responses at offsets of ± f_{SPUR} around the desired responses. Close-in spurs of this kind are not visible on the plot; however, small spurious responses at $f_{LO} \pm f_{IF2_ADC} \pm f_{CLK}$ (at 50.85 MHz, 55.35 MHz, 86.85 MHz, and 91.35 MHz) are visible at the −90 dBFS level. This data indicates that the AD9864 does an excellent job of preserving the purity of the LO signal.

Figure 71 can also be used to gauge how well the AD9864 rejects undesired signals. For example, the half-IF response (at 69.975 MHz and 72.225 MHz) is approximately −100 dBFS, giving a selectivity of 90 dB for this spurious response. The largest spurious response at approximately −70 dBFS occurs with input frequencies of 70.35 MHz and 71.85 MHz. These spurs result from third-order nonlinearity in the signal path (that is, abs [$3 \times f_{LO} - 3 \times f_{IF_INPUT}$] = $f_{CLK}/8$).

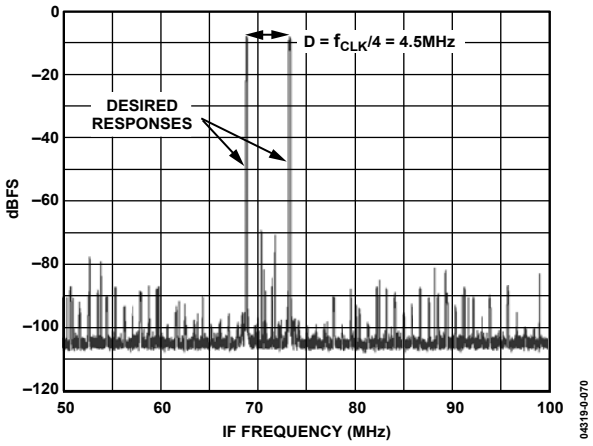


Figure 71. Response of AD9864 to a −20 dBm IF Input when f_{LO} = 71.1 MHz

EXTERNAL PASSIVE COMPONENT REQUIREMENTS

Figure 72 shows an example circuit using the AD9864 and Table 23 shows the nominal dc bias voltages seen at the different pins. The purpose is to show the various external passive components required by the AD9864, along with nominal dc voltages for troubleshooting purposes.

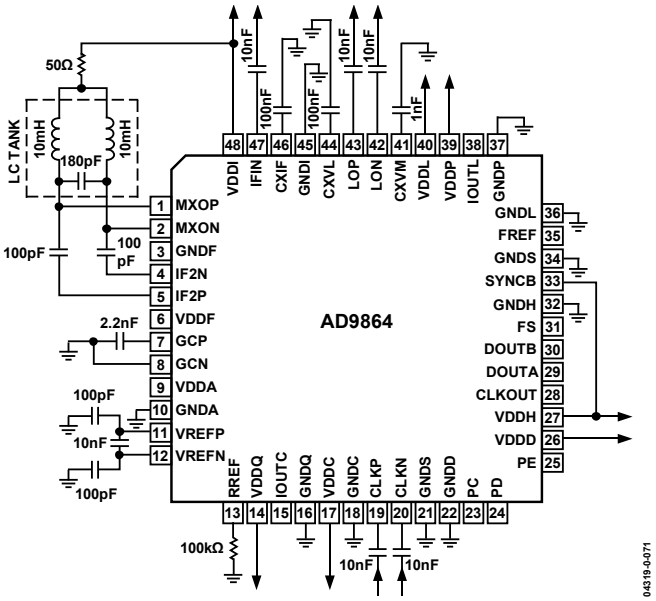


Figure 72. Example Circuit Showing Recommended Component Values

Table 23. Nominal DC Bias Voltages

Pin Number	Mnemonic	Nominal DC Bias (V)
1	MXOP	VDDI – 0.2
2	MXON	VDDI – 0.2
4	IF2N	1.3 – 1.7
5	IF2P	1.3 – 1.7
11	VREFP	VDDA/2 + 0.250
12	VREFN	VDDA/2 – 0.250
13	RREF	1.2
19	CLKP	VDDC – 1.3
20	CLKN	VDDC – 1.3
35	FREF	VDDC/2
41	CXVM	1.6 – 2.0
42	LON	1.65 – 1.9
43	LOP	1.65 – 1.9
44	CXVL	VDDI – 0.05
46	CXIF	1.6 – 2.0
47	IFIN	0.9 – 1.1

The LO, CLK, and IFIN signals are coupled to their respective inputs using 10 nF capacitors. The output of the mixer is coupled to the input of the ADC using 100 pF. An external 100 kΩ resistor from the RREF pin to GND sets up the internal bias currents of the AD9864. VREFP and VREFN provide a differential reference voltage to the Σ-Δ ADC of the AD9864, and must be decoupled by a 0.01 μF differential capacitor along with two 100 pF capacitors to GND. The remaining capacitors are used to decouple other sensitive internal nodes to GND. Note that SYNCB is tied to VDDH because it is unused.

Although power supply decoupling capacitors are not shown, it is recommended that a 0.1 μF surface-mount capacitor be placed as close as possible to each power supply pin for maximum effectiveness. Also not shown is the input impedance matching network used to match the IF input of the AD9864 to the external IF filter. Lastly, the loop filter components associated with the LO and CLK synthesizers are not shown.

LC component values for f_{CLK} = 18 MHz are given in Figure 72. For other clock frequencies, the two inductors and the capacitor of the LC tank must be scaled in inverse proportion to the clock. For example, if f_{CLK} = 26 MHz, the two inductors must be 6.9 μH and the capacitor must be approximately 120 pF. A tolerance of 10% is sufficient for these components because tuning of the LC tank is performed upon system startup.

APPLICATIONS

Superheterodyne Receiver Example

The AD9864 is well suited for analog and/or digital narrow-band radio systems based on a superheterodyne receiver architecture. The superheterodyne architecture is noted for achieving exceptional dynamic range and selectivity by using two or more downconversion stages to provide amplification of the target signal while filtering the undesired signals. The AD9864 greatly simplifies the design of these radio systems by integrating the complete IF strip (excluding the LO VCO) while providing an I/Q digital output (along with other system parameters) for the demodulation of both analog and digital modulated signals. The exceptional dynamic range of the AD9864 often simplifies the IF filtering requirements and eliminates the need for an external AGC.

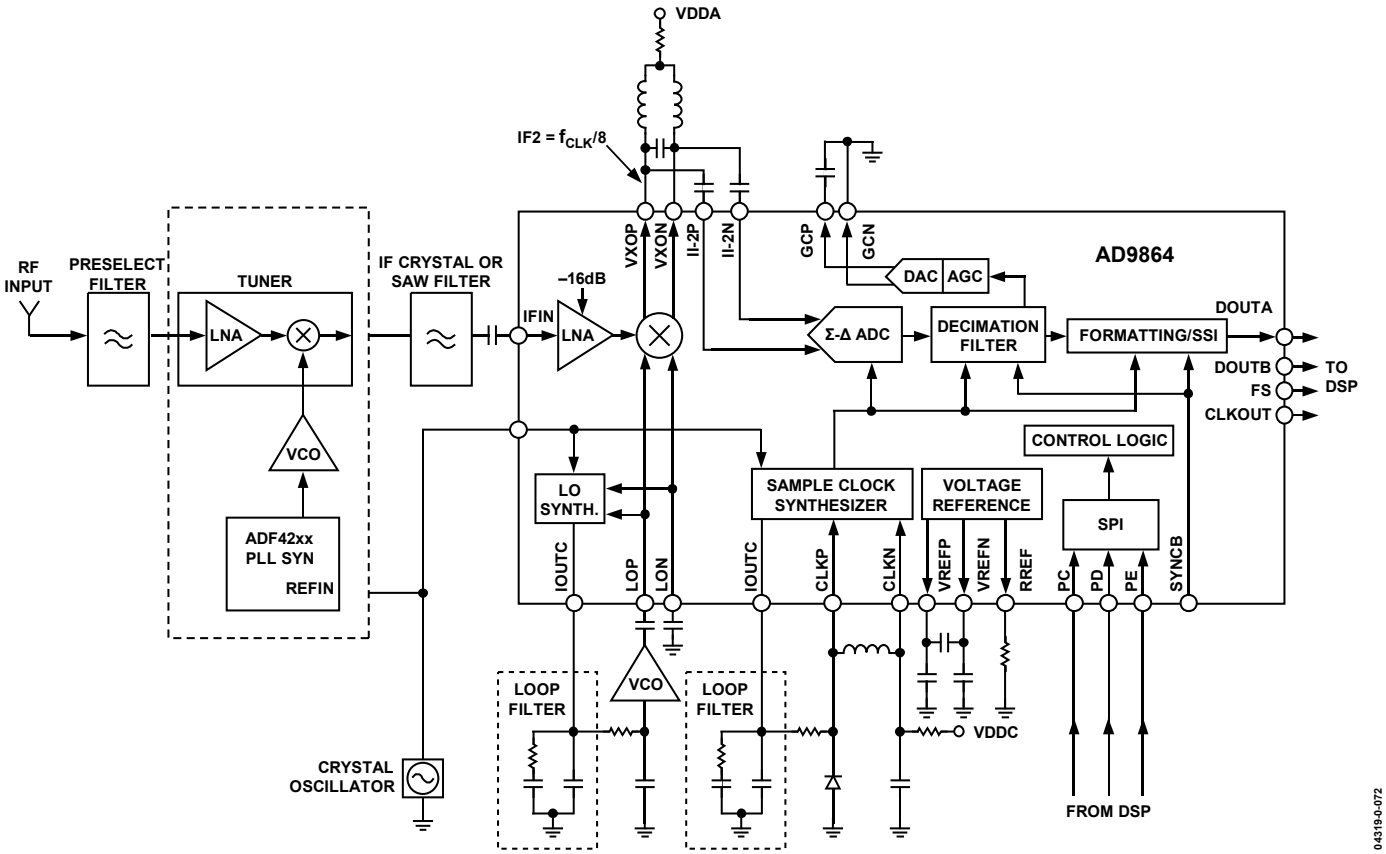


Figure 73. Typical Dual Conversion Superheterodyne Application Using the AD9864

Figure 73 shows a typical dual conversion superheterodyne receiver using the AD9864. An RF tuner is used to select and downconvert the target signal to a suitable first IF for the AD9864. A preselect filter may precede the tuner to limit the RF input to the band of interest. The output of the tuner drives an IF filter that provides partial suppression of adjacent channels and interferers that could otherwise limit the dynamic range of the receiver. Set the conversion gain of the tuner such that the peak IF input signal level into the AD9864 is no greater than −18 dBm to prevent clipping. The AD9864 downconverts the first IF signal to a second IF that is exactly 1/8 of the clock rate of the Σ-Δ ADC ($f_{CLK}/8$) to simplify the digital quadrature demodulation process.

This second IF signal is then digitized by the Σ-Δ ADC, demodulated into its quadrature I and Q components, filtered via matching decimation filters, and reformatted to enable a synchronous serial interface to a DSP. In this example, the LO and CLK synthesizers of the AD9864 are both enabled, requiring some additional passive components (for the loop filters and CLK oscillator of the synthesizer) and a VCO for the LO synthesizer. Note that not all of the required decoupling capacitors are shown. See the External Passive Component Requirements section and Figure 72 for more information on required external passive components.

The selection of the first IF frequency is often based on the availability of low cost standard crystal or SAW filters as well as system frequency planning considerations. In general, crystal filters are often used for narrow-band radios having channel bandwidths below 50 kHz with IFs below 120 MHz, while SAW filters are more suited for channel bandwidths greater than 50 kHz with IFs greater than 70 MHz. The ultimate stop-band rejection required by the IF filter depends on how much suppression is required at the AD9864 image band resulting from downconversion to the second IF. This image band is offset from the first IF by twice the second IF frequency (± $f_{CLK}/4$, depending on high-side or low-side injection).

The selectivity and bandwidth of the IF filter depends on both the magnitude and frequency offset(s) of the adjacent channel blocker(s) that could overdrive the input of the AD9864 or generate in-band intermodulation components. Further suppression is performed within the AD9864 by its inherent band-pass response and digital decimation filters. Note that some applications require additional application-specific filtering performed in the DSP that follows the AD9864 to remove the adjacent channel and/or implement a matched filter for optimum signal detection.

Choose the output data rate of the AD9864, f_{OUT}, to be at least twice the bandwidth or symbol rate of the desired signal to ensure that the decimation filters provide a flat pass-band response as well as to allow for postprocessing by a DSP. After f_{OUT} is determined, the decimation factor of the digital filters must be set such that the input clock rate, f_{CLK}, falls between the AD9864

rated operating range of 13 MHz to 26 MHz and no significant spurious products related to f_{CLK} fall within the desired pass band, resulting in a reduction in sensitivity performance. If a spurious component is found to limit the sensitivity performance, the decimation factor can often be modified slightly to find a spurious free pass band. Selecting a higher f_{CLK} is typically more desirable given a choice, because the filtering requirements of the first IF often depend on the transition region between the IF frequency and the image band ($\pm f_{CLK}/4$). Lastly, the output SSI clock rate, f_{CLKOUT}, and digital driver strength must be set to their lowest possible settings to minimize the potential harmful effects of digital induced noise while preserving a reliable data link to the DSP. Note that the SSICRA, SSICRB, and SSIORD registers (0x18, 0x19, and 0x1A) provide a large degree of flexibility for optimization of the SSI interface.

Synchronization of Multiple AD9864 Devices

Some applications, such as receiver diversity and beam steering, may require two or more AD9864 devices operating in parallel while maintaining synchronization. Figure 73 shows an example of how multiple AD9864 devices can be cascaded, with one device serving as the master and the other devices serving as the slaves. In this example, all of the devices have the same SPI register configuration since they share the same SPI interface to the DSP. Because the state of each of the internal counters of the AD9864 devices is unknown upon initialization, synchronization of the devices is required via a SYNCB pulse (see Figure 37) to synchronize their digital filters and to ensure precise time alignment of the data streams.

Although the synthesizers of all of the device are enabled, the LO and CLK signals for the slave(s) are derived from the synthesizers of the master and are referenced to an external crystal oscillator. All of the necessary external components (the loop filters, varactor, LC, and VCO) required to ensure proper closed-loop operation of the master synthesizers are included. Note that the FREF input of the slave devices must be tied to ground.

Note that although the VCO output of the LO synthesizer is ac-coupled to the LO input(s) of the slave, all of the CLK inputs of the devices must be dc-coupled if the CLK oscillators of the AD9864 are enabled. This is because of the dc current required by the CLK oscillators in each device. In essence, these negative impedance cores are operating in parallel, increasing the effective Q of the LC resonator circuit. R_{BIAS} must be sized such that the sum of the dc bias currents of the oscillators maintains a common-mode voltage of approximately 1.6 V.

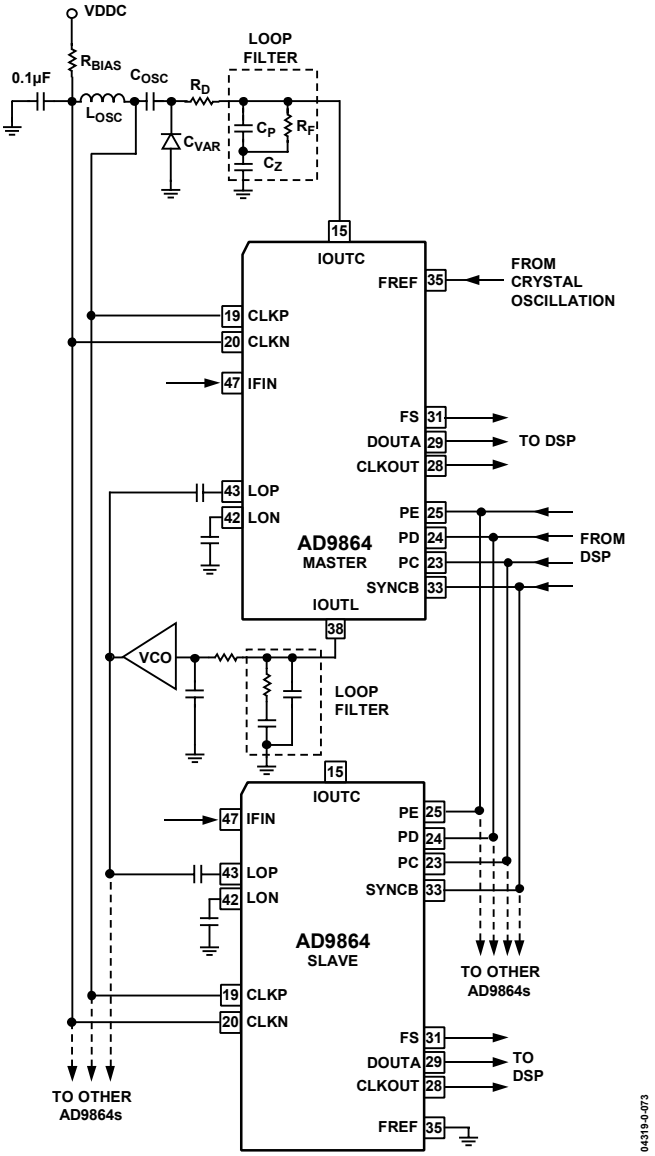


Figure 74. Example of Synchronizing Multiple AD9864 Devices

Split Path Rx Architecture

A split path Rx architecture may be attractive for those applications whose instantaneous dynamic range requirements exceed the capability of a single AD9864 device. To cope with these higher dynamic range requirements, two AD9864 devices can be operated in parallel with their respective clip points offset by a fixed amount. Adding a fixed amount of attenuation in front of the AD9864 and/or programming the attenuation setting of its internal VGA can adjust the input-referred clip point. To save power and simplify hardware, the LO and CLK circuits of the device can also be shared. Connecting the SYNCB pins of the two devices and pulsing this line low synchronizes the two devices.

An example of this concept for possible use in a GSM base station is shown in Figure 75. The signal chain consists of a high linearity RF front end and IF stage followed by two AD9864 devices operating in parallel. The RF front end consists of a duplexer and preselect filter to pass the GSM RF band of interest. A high performance LNA isolates the duplexer from the preselect filter while providing sufficient gain to minimize system NF. An RF mixer is used to downconvert the entire GSM band to a suitable IF, where much of the channel selectivity is accomplished. The 170.6 MHz IF is chosen to avoid any self induced spurs from the AD9864. The IF stage consists of two SAW filters isolated by a 15 dB gain stage.

The cascaded SAW filter response must provide sufficient blocker rejection for the receiver to meet its sensitivity requirements under worst-case blocker conditions. A composite response having 27 dB, 60 dB, and 100 dB rejection at frequency offsets of ±0.8 MHz, ±1.6 MHz, and ±6.5 MHz, respectively, provides enough blocker suppression to ensure that the AD9864 with the lower clip point is not overdriven by any blocker. This configuration results in the best possible receiver sensitivity under all blocking conditions.

The output of the last SAW filters drives the two AD9864 devices via a direct signal path and an attenuated signal path. The direct path corresponds to the AD9864 having the lowest clip point and provides the highest receiver sensitivity with a system noise figure of 4.7 dB. The VGA of this device is set for maximum attenuation, so its clip point is approximately −17 dBm. Since conversion gain from the antenna to the AD9864 is 19 dB, the digital output of this path is nominally selected unless the target signal's power exceeds −36 dBm at the antenna. The attenuated path corresponds to the AD9864 having the highest input-referred clip point, and its digital output point of this path is set to 7 dBm by inserting a 30 dB attenuator and setting the VGA of the AD9864 to the middle of its 12 dB range. This setting results in a ±6 dB adjustment of the clip point, allowing the clip point difference to be calibrated to exactly 24 dB, so that a simple 5-bit shift would make up the gain difference. The attenuated path can handle signal levels up to −12 dB at the antenna before being overdriven. Because the SAW filters provide sufficient blocker suppression, the digital data from this path need only be selected when the target signal exceeds −36 dBm. Although the sensitivity of the receiver with the attenuated path is 20 dB lower than the direct path, the strong target signal ensures a sufficiently high carrier-to-noise ratio.

Because GSM is based on a TDMA scheme, digital data (or path) selection can occur on a slot-by-slot basis. Configure the AD9864 to provide serial I and Q data at a frame rate of 541.67 kSPS, as well as additional information including a 2-bit reset field and a 6-bit RSSI field. These two fields contain the information needed to decide whether the direct or attenuated path is to be used for the current time slot.

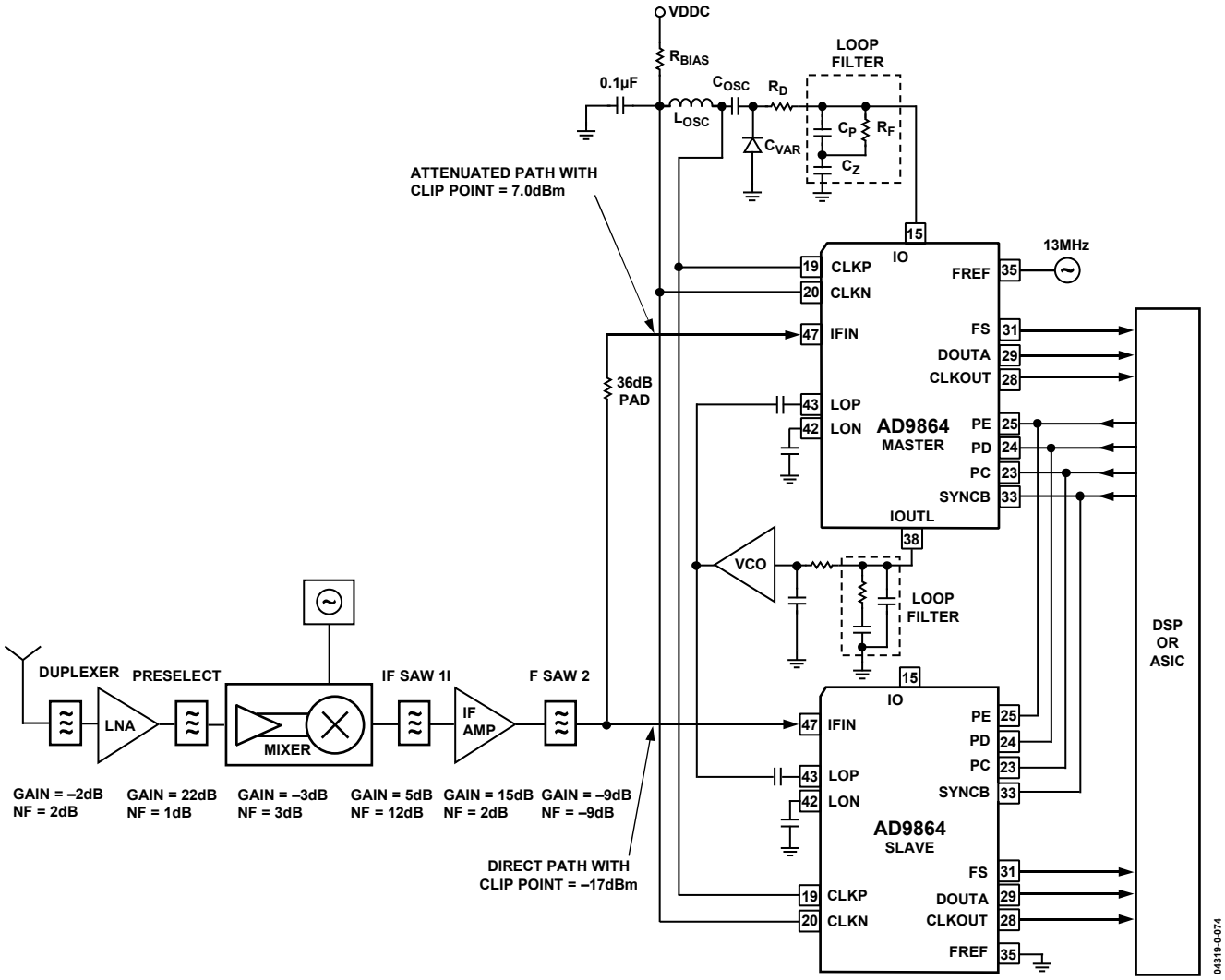


Figure 75. Example of Split Path Rx Architecture to Increase Receiver Dynamic Range Capabilities

Hung Mixer Mode

The AD9864 can operate in hung mixer mode by tying one of the self biasing inputs of the LO to ground (that is, GNDI), or the positive supply (VDDI). In this mode, the AD9864 acts as a narrow-band, band-pass Σ-Δ ADC, because its mixer passes the IFIN signal without any frequency translation. The IFIN signal must be centered around the resonant frequency of the Σ-Δ ADC, $f_{CLK}/8$, and the clock rate, f_{CLK}, and decimation factors must be selected to accommodate the bandwidth of the desired input signal. Note that the LO synthesizer can be disabled because it is no longer required.

Because the mixer does not have any losses associated with the mixing operation, the conversion gain through the LNA and mixer is higher resulting in a nominal input clip point of −24 dBm. The SNR performance is dependent on the VGA attenuation setting, I/Q data resolution, and output bandwidth as shown in Figure 76. Applications requiring the highest instantaneous dynamic range must set the VGA for maximum attenuation. Several extra decibels in SNR performance can be gained at lower signal bandwidths by using 24-bit I/Q data.

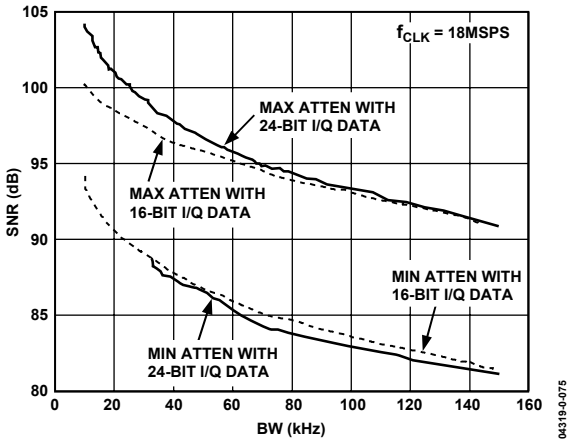


Figure 76. Hung Mixer SNR vs. BW and VGA

LAYOUT EXAMPLE, EVALUATION BOARD, AND SOFTWARE

The evaluation platform and its accompanying software provide a simple way to evaluate the AD9864. Figure 77 shows the AD9864 evaluation board connected to the HSC-ADC-EVALCZ data capture card in its simplest configuration with only an external 5 V lab supply and RF signal generator required for the AD6676 evaluation board. The evaluation board is designed to be flexible, supporting different IFs as well as LO and CLK generation schemes. An alternative right angle 18-pin header is available for monitoring digital input/output signals or interfacing to other FPGA, DSP, or microcontroller development platforms. The evaluation board also serves as a layout example.

The power supply distribution block provides filtered, adjustable voltages to the main core of the AD9864 as well as the digital input/output supply. In the IF input signal path, component pads are available to implement different IF impedance matching networks. The LO and CLK signals can be externally applied or internally derived from on-board VCOs supporting the on-chip LO and CLK synthesizers. The reference for the on-chip LO and CLK synthesizers can be applied via the external f_{REF} input or an via the on-board crystal oscillator.

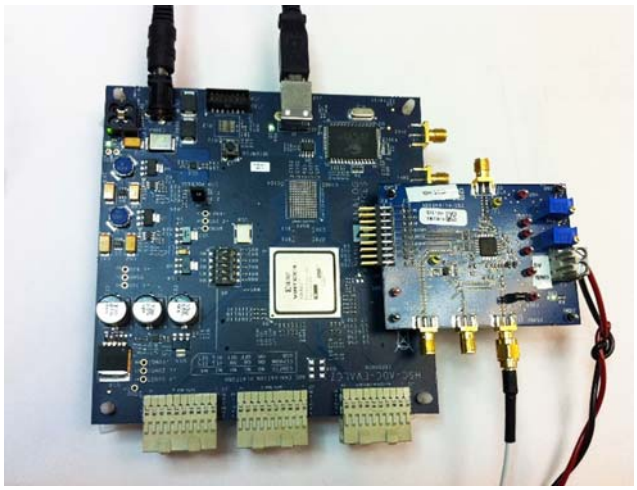


Figure 77. Evaluation Board Platform

A simple software SPI control graphical user interface (GUI) provides a ways to configure the AD9864. Analog Devices VisualAnalog software is used for real-time data analysis. These programs have a convenient GUI that allows easy access to the various SPI port configuration registers and frequency/time domain analysis of the output data.

SPI INITIALIZATION EXAMPLE

Table 24 shows an example SPI initialization sequence that is used to configure the device when using both the on-chip LO and CLK synthesizer. Note the following:

- Step 4 through Step 10 can be avoided if an external clock is supplied. Note that clock synthesizer and oscillator must also be disabled in Step 3 (0x00 = 0x7F) and remain disabled in Step 15 (0x70 or 0x30 depending on the LO synthesizer being enabled).
- Step 20 to Step 24 can be avoided if an external LO source is supplied.
- Wait states are included for both tuning procedure and clock synthesizer (if used).

DEVICE SPI INITIALIZATION

Table 24 shows an example SPI initialization script when both the CLK SYN/OSC and LO SYN are used.

Table 24. SPI Initialization Example, f_{CLKIN} = 16.8 MHz, f_{ADC} = 18 MHz, f_{IF} = 73.35 MHz, LO = 71.10 MHz, f_{DATA_IQ} = 60 kSPS with Decimate by 300

Step	Address (Hex)	Write Value	Description
1	0x3F	0x99	Software reset.
2	0x19	0x87	Enable 4-wire SPI readback while keeping default 16-bit I/Q word width and maximum CMOS output drive strength.
3	0x00	0x45	Take REF, GC, and CLK SYN/LO out of standby.
Configure Clock Synthesizer			
4	0x01	0x0C	Set the CK oscillator bias to 0.65 mA for maximum swing.
5	0x10	0x00	Set the CLK synthesizer MSB and LSB reference frequency divider. (Note that default setting is shown resulting in divide by 56.)
6	0x11	0x38	
7	0x12	0x00	Set the CLK synthesizer MSB and LSB reference frequency divider. (Note that default setting is shown resulting in divide by 300.)
8	0x13	0x3C	
9	0x14	0x03	Set the CLK synthesizer charge pump to 0.625 mA. (Note that setting depends on PLL loop configuration.)
10	Not applicable	Not applicable	Wait until the CLK SYN output frequency settles to within 0.01% of final frequency.
Begin LC and RC Resonator Calibration			
11	0x3E	0x47	Disable the internal ADC unstable signal. Enable RC Q enhancement, and bypass the RC and SC resonators.
12	0x38	0x01	Enable manual control of feedback DAC.
13	0x39	0x0F	Set DAC to midscale.
14	0x1C	0x03	Set LC and RC tuning bits.
15	0x00	0x44	Bring ADC out of standby to initiate LC and RC calibration.
16	0x1C	Readback value	Wait 6 ms and read back Register 0x1C. If Register 0x1C clears, proceed to Step 17. If Register 0x1C does not clear, reset Register 0x1C and return to Step 14. Make five attempts before exiting loop.
17	0x38	0x00	Disable manual control of feedback DAC.
18	0x3E	0x00	Re-enable ADC unstable signal, disable RC_Q enhancement, and disable bypass of RC and SC resonators.
End of LC and RC Resonator Calibration			
19	0x00	0x00	Bring LNA/Mixer and LO synthesizer out of standby.
Configure LO Synthesizer			
20	0x08	0x00	Set the LO synthesizer MSB and LSB reference frequency divider. (Note that the default setting is shown resulting in divide by 56.)
21	0x09	0x38	
22	0x0A	0xA0	Set the LO synthesizer A and B counters. (Note that the default setting is shown resulting in divide by 237.)
23	0x0B	0x1D	
24	0x0C	0x03	Set the LO synthesizer charge pump to 0.625 mA. (Note that setting depends on PLL loop configuration.)
Configure Remaining SPI Registers			
25	0x03 to 0x07		Set AGC registers.
26	0x07	0x04	Set decimation factor to 300.
27	0x1A	0x01	Set SSIORD register, which determines the CLKOUT frequency.
28	0x18	0x40	Take FS and CLKOUT out of tristate and configure SSI frame format.

OUTLINE DIMENSIONS

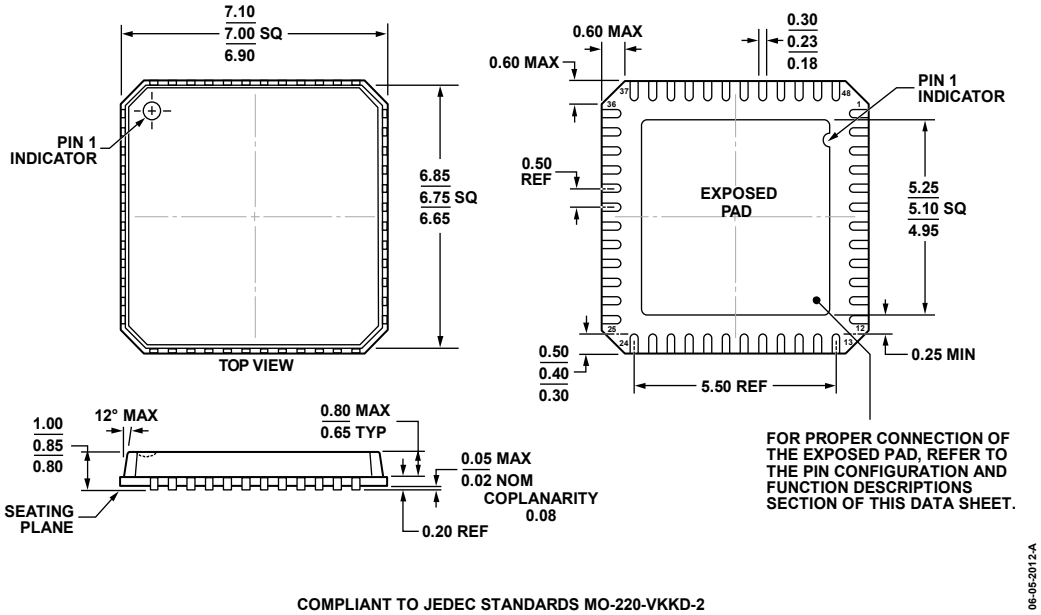


Figure 78. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.85 mm Package Height
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9864BCPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-1
AD9864BCPZRL	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-1
AD9864-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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