

MOSFET – N-Channel, POWER trench

150 V, 167 A, 5.9 mΩ

FDH055N15A

Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced POWER trench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

- $R_{DS(on)} = 4.8 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 120 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb-Free and is RoHS Compliant

Applications

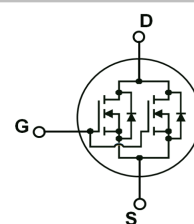
- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



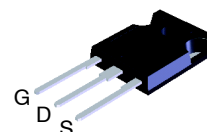
ON Semiconductor®

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V_{DS}	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	5.9 mΩ @ 10 V	167 A

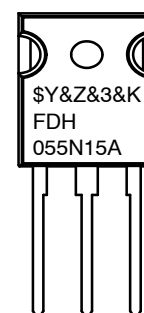


N-CHANNEL MOSFET



TO-247-3LD
CASE 340CK

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDH055N15A	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDH055N15A

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		150	V
V _{GSS}	Gate to Source Voltage	– DC	±20	V
		– AC (f > 1 Hz)	±30	
I _D	Drain Current	– Continuous (T _C = 25°C, Silicon Limited)	167 (Note 1)	A
		– Continuous (T _C = 100°C, Silicon Limited)	118	
		– Continuous (T _C = 25°C, Package Limited)	156	
I _{DM}	Drain Current	– Pulsed (Note 2)	668	A
E _{AS}	Single Pulsed Avalanche Energy (Note 3)		835	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 4)		6.0	V/ns
P _D	Power Dissipation	(T _C = 25°C)	429	W
		– Derate above 25°C	2.86	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to + 175	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Second		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Calculated continuous current based on maximum allowable junction temperature, Package limitation current is 156 A.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. Starting T_J = 25°C, L = 3 mH, I_{AS} = 23.6 A
4. I_{SD} ≤ 120 A, di/dt ≤ 200 A/s, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDH055N15A	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Package Method	Reel Size	Tape Width	Quantity
FDH055N15A	FDH055N15A	TO-247-3LD	Tube	N/A	N/A	30 Units

FDH055N15A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	150	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.1	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 120 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 120 V, T _C = 150°C	–	–	500	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	–	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 120 A	–	4.8	5.9	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 120 A	–	219	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz	–	7100	9445	pF
C _{oss}	Output Capacitance		–	664	885	pF
C _{rss}	Reverse Transfer Capacitance		–	23	35	pF
C _{oss(er)}	Energy Related Output Capacitance	V _{DS} = 75 V, V _{GS} = 0 V	–	1159	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 75 V, I _D = 120 A, V _{GS} = 10 V (Note 5)	–	92	–	nC
Q _{gs}	Gate to Source Gate Charge		–	31	–	nC
Q _{gs2}	Gate Charge Threshold to Plateau		–	15	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	16	–	nC
ESR	Equivalent Series Resistance(G–S)	f = 1 MHz	–	1.2	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 75 V, I _D = 120 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 5)	–	35	80	ns
t _r	Turn-On Rise Time		–	67	144	ns
t _{d(off)}	Turn-Off Delay Time		–	71	152	ns
t _f	Turn-Off Fall Time		–	21	52	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	167 (Note 1)	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	668	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 120 A	–	–	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 120 A, V _{DS} = 75 V, dI _F /dt = 100 A/μs	–	105	–	ns
Q _{rr}	Reverse Recovery Charge		–	342	–	nC
Q _{rr}	Reverse Recovery Charge	V _{GS} = 0 V, I _{SD} = 30 A, V _{DS} = 75 V, dI _F /dt = 100 A/μs	–	348	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially Independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

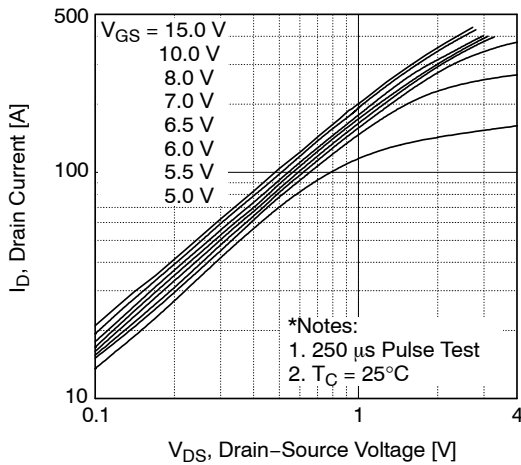


Figure 1. On-Region Characteristics

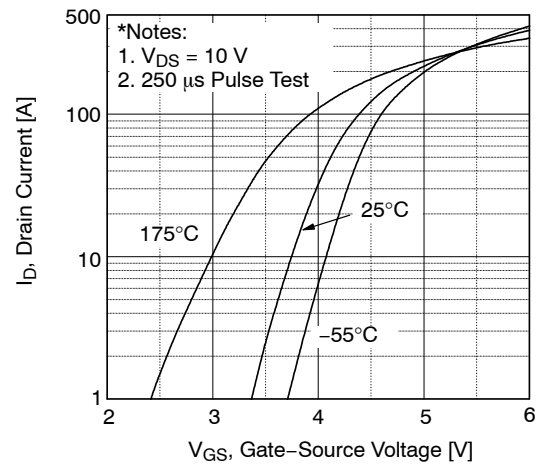


Figure 2. Transfer Characteristics

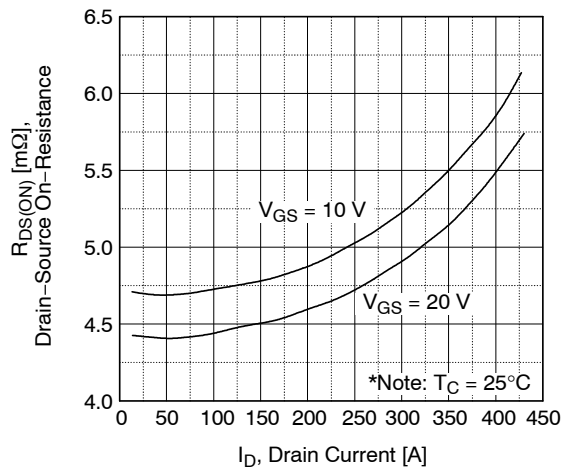


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

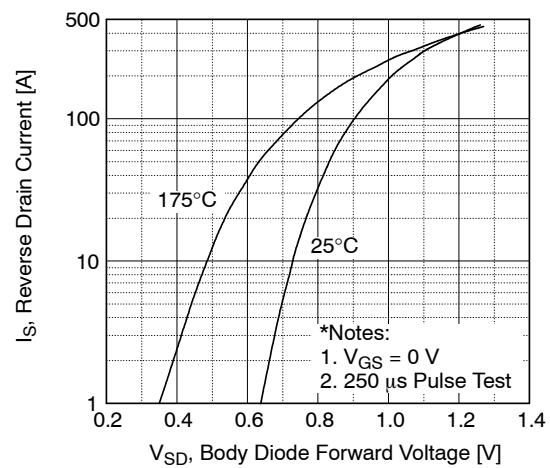


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

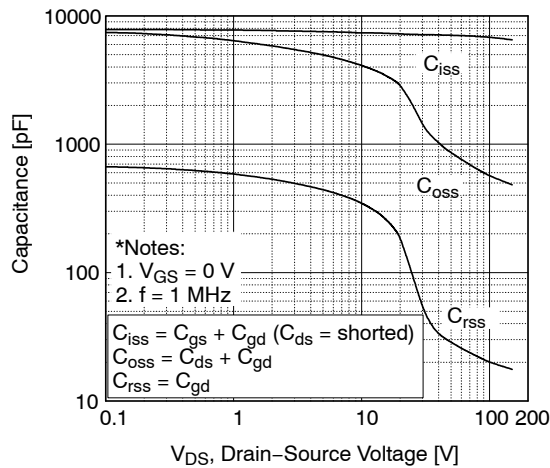


Figure 5. Capacitance Characteristics

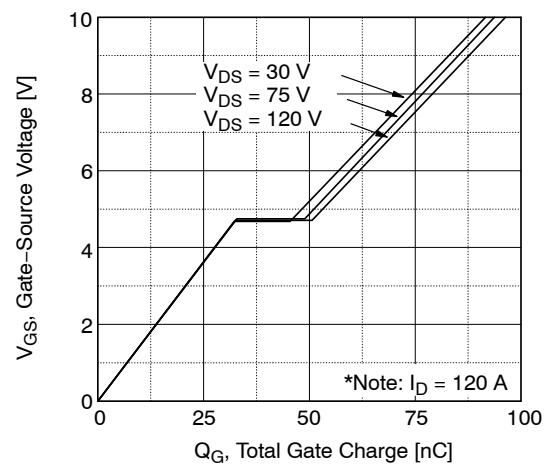


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

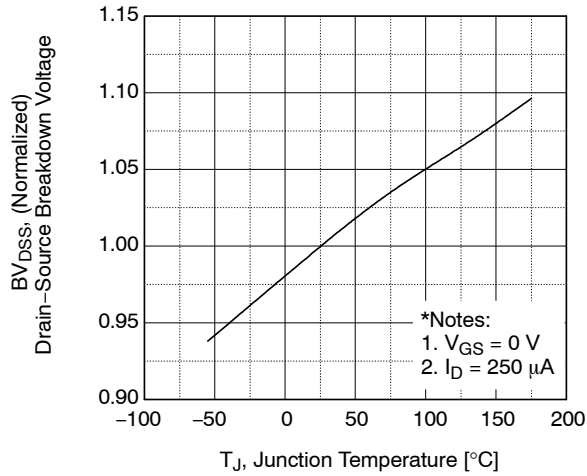


Figure 7. Breakdown Voltage Variation vs. Temperature

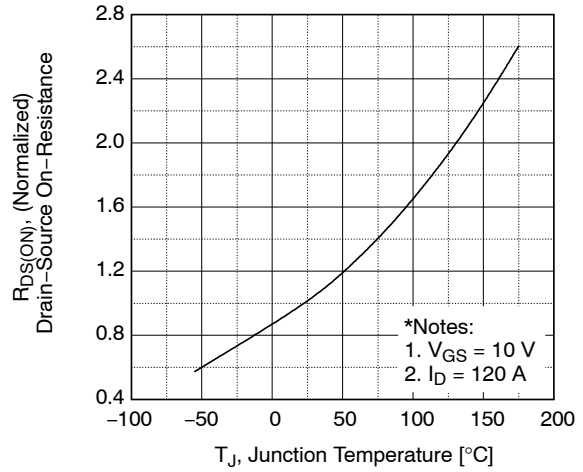


Figure 8. On-Resistance Variation vs. Temperature

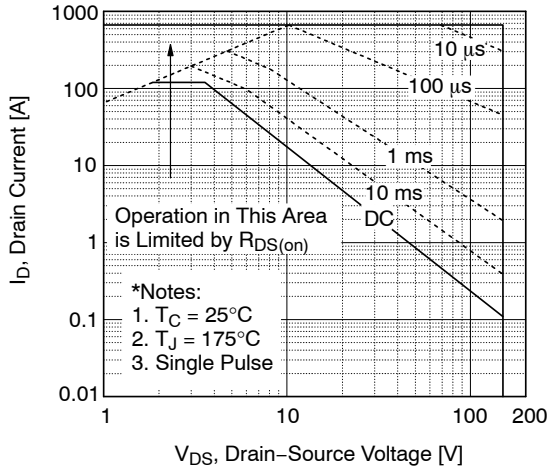


Figure 9. Maximum Safe Operating Area

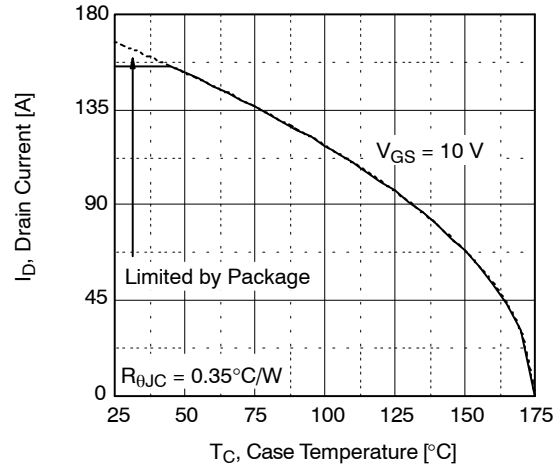


Figure 10. Maximum Drain Current vs. Case Temperature

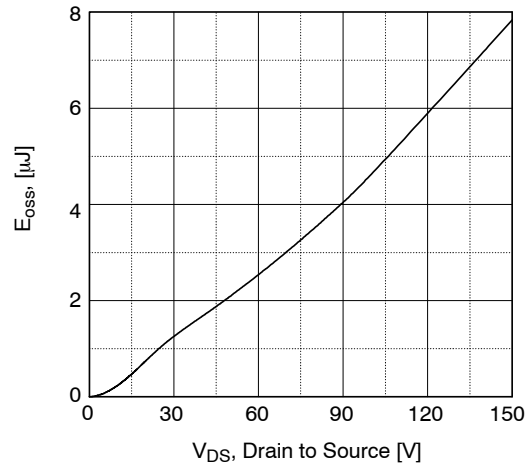


Figure 11. Eoss vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (continued)

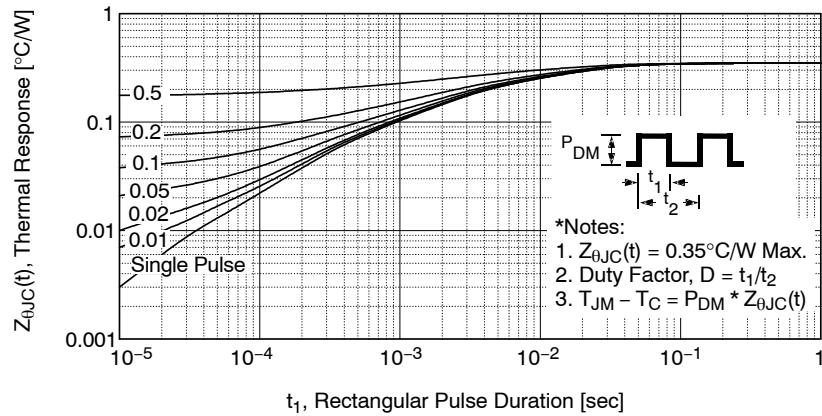


Figure 12. Transient Thermal Response Curve

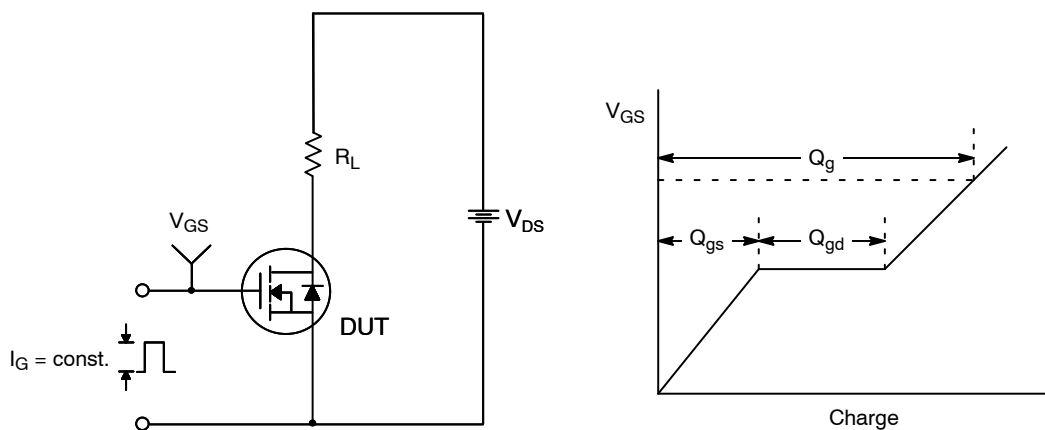


Figure 13. Gate Charge Test Circuit & Waveform

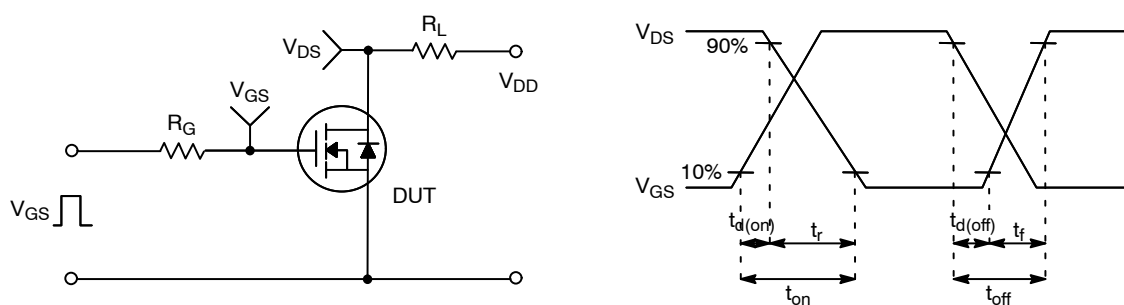


Figure 14. Resistive Switching Test Circuit & Waveforms

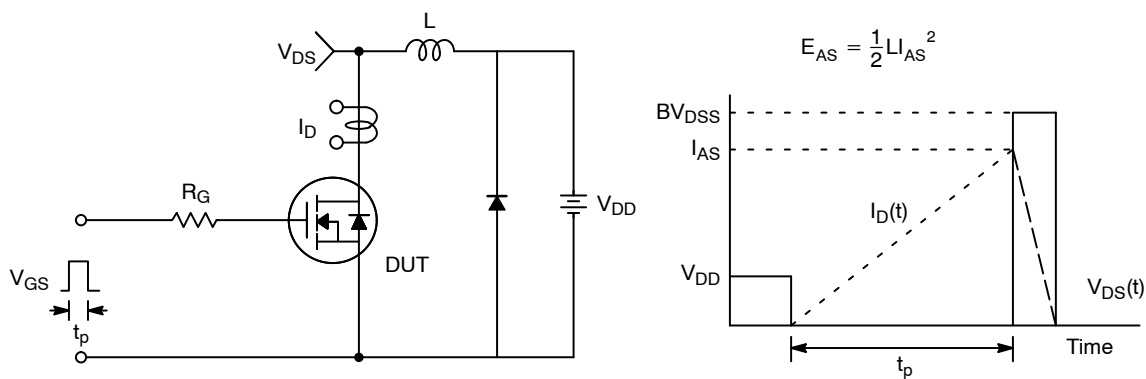
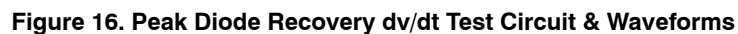
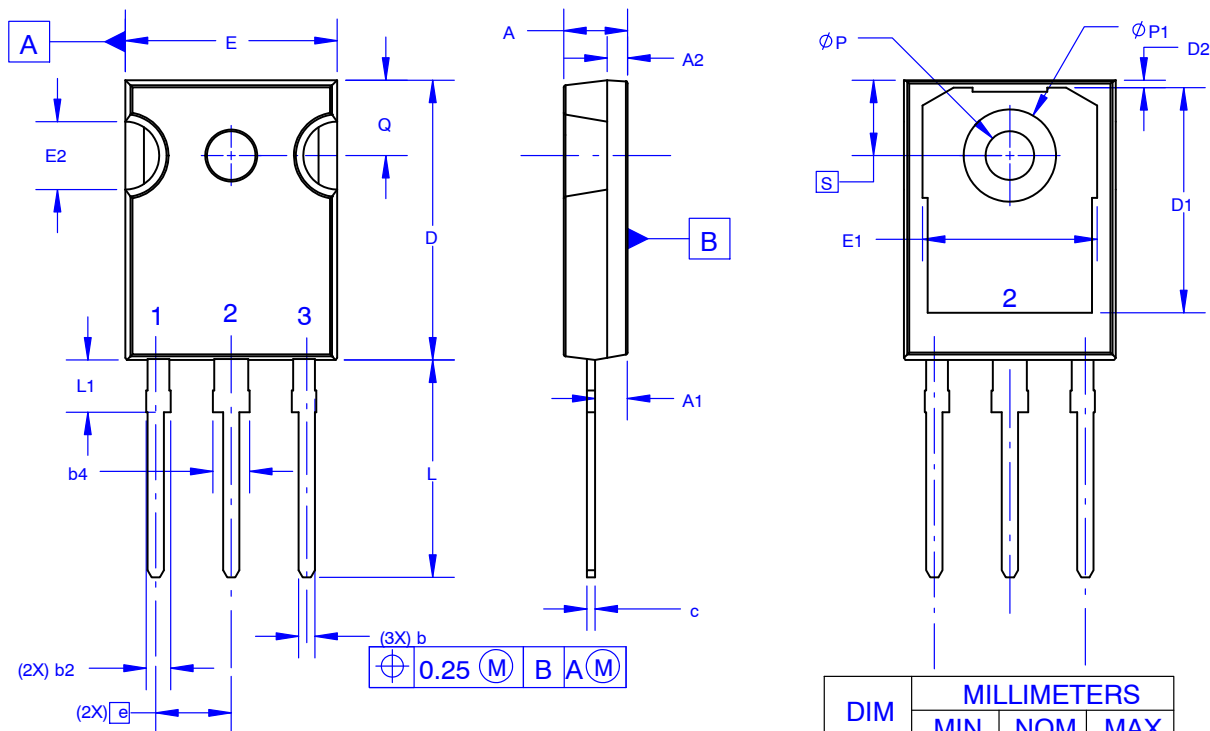


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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TO-247-3LD SHORT LEAD CASE 340CK ISSUE A

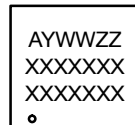
DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ϕP	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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