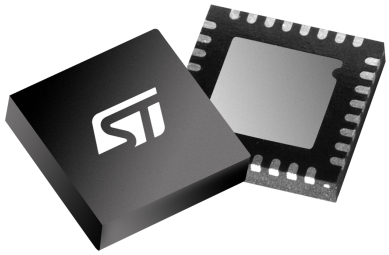
L9961

Datasheet

Battery management system solution



VFQFPN32
(5x5x1.00 mm)

Prerelease product(s)

Product status link
L9961

Product label
SUSTAINABLE TECHNOLOGY

Product summary		
Order code	**Package**	**Packing**
L9961	SO16N	Tube
L9961 -TR		Tape and reel

Features

- 2 µA shipment - DEEP SLEEP mode current and 5 µA standby consumption (with VREG LDO active) standby consumption (with VREG LDO active)
- Integrated 3.3 V VREG LDO for supplying MCU and LEDs
- Measures cell voltage (3 to 5 cells), with over/undervoltage detection and balance undervoltage protection
- 12-bit voltage measurement with maximum error of ±15 mV in the [1.5–4.5] V range, for -40 °C < T_J < 105 °C
- Measures stack voltage, with over/under voltage detection and plausibility check vs. sum of cells
- Measures pack temperature via NTC, with over/undertemperature detection
- Ratiometric temperature measurement with ±0.8% max. gain error in the [0.2–VREG] V range, for -40 °C < T_J < 105 °C
- Measures battery current, with Coulomb counting, overcurrent (both directions) and short-circuit in discharge protection.
- 16-bit signed current measurement with 0.1% full scale error at room temperature
- I2C peripheral for device programming and data transfers over I2C bus
- Cell balancing supporting up to 70 mA per cell
- Dual configurable HS/LS predriver for pack relay management
- Pack fuse management
- Embedded NVM for configuration parameters storage
- High hotplug robustness

Applications

- Cordless power tools
- Backup energy storage systems and UPS
- Light electric vehicles (e-bikes, scooters, etc)
- Portable and semi-portable equipment
- Medical equipment

Description

L9961 is part of a complete battery pack monitoring, balancing, and protecting system for Li-Ion and Li-Polymer cells in 3, 4 or 5 series configurations. The L9961 uses a high precision ADC to provide cell voltage, stack voltage and temperature conversion via external NTC. Voltage monitoring functions are cyclically performed with a programmable loop time. Stack current is also monitored via a high accuracy CSA, continuously running and performing also Coulomb counting. Cell balancing is available and can be simultaneously activated on all cells. IC configuration and information exchange for SOC/SOH estimation are performed via I2C peripheral. The IC also integrates a dual pre-driver programmable in both HS/LS configurations for driving pack relays. L9961 also implements battery pack fuse protection to prevent fire and explosion hazards. A 3.3 V regulator with a high current capability is available for supplying pack controller and other external circuitry in both standby and normal operation modes. The IC protects the battery pack against over/under voltage conditions and monitors for over/under temperature. It also features protection against overcurrent (both directions) and short-circuit in discharge events. Safety-relevant configurations can be stored in the internal NVM to avoid re-programming the device at each wakeup.

Prerelease product(s)

1 Pin description and block diagram

1.1 Device pinout

Table 1. Device pinout

Pin #	Pin name	Pin function	Pin type	Internal PU/PD	Active
1	C0	Cell 1 negative terminal	Analog in		
2	ISENSEP	Current sense ADC positive input terminal	Analog in		
3	ISENSEM	Current sense ADC negative input terminal	Analog in		
4	GND	Device ground	Power in		
5	SCL	I2C clock line	Digital input		Low
6	SDA	I2C data line	Digital input/ open-drain		Low
7	RDY	Ready interrupt output	Push/pull		
8	VREG	3.3 V LDO output	Power out		
9	NTC	NTC sensing input	Analog in		
10	OD	Open-drain switch for NTC connection to GND	Open-drain		Low
11	FAULTN_SAFE	Critical fault output	Open-drain		Low
12	FAULTN	Fault output / external CHG/ DCHG shutdown trigger	Digital input/ open-drain		Low
13	TM_ENTER	Reserved for debug. Connect to GND.		PD	
14	WAKEUP	Wakeup from STANDBY input	Digital I/O	PD	High
15	NSHIP	Wakeup from SHIPMENT - DEEP SLEEP input	Analog in		High
16	FUSE	Fuse pre-driver output / external fuse activation trigger	Analog out/digital in	PD	High
17	DCHG	Discharge switch gate	Analog out		
18	VSD	Discharge switch source	Analog out		
19	VSC	Charge switch source	Analog out		
20	CHG	Charge switch gate	Analog out		
21	VCP1M	Charge pump flying capacitor input	Analog		
22	VCP1P	Charge pump flying capacitor input	Analog		
23	VCP2M	Charge pump flying capacitor input	Analog		
24	VCP2P	Charge pump flying capacitor input	Analog		
25	VCP	Charge pump output	Power out		
26	VB	Device battery input	Power in		
27	TM1	Reserved for debug. Connect to GND.			

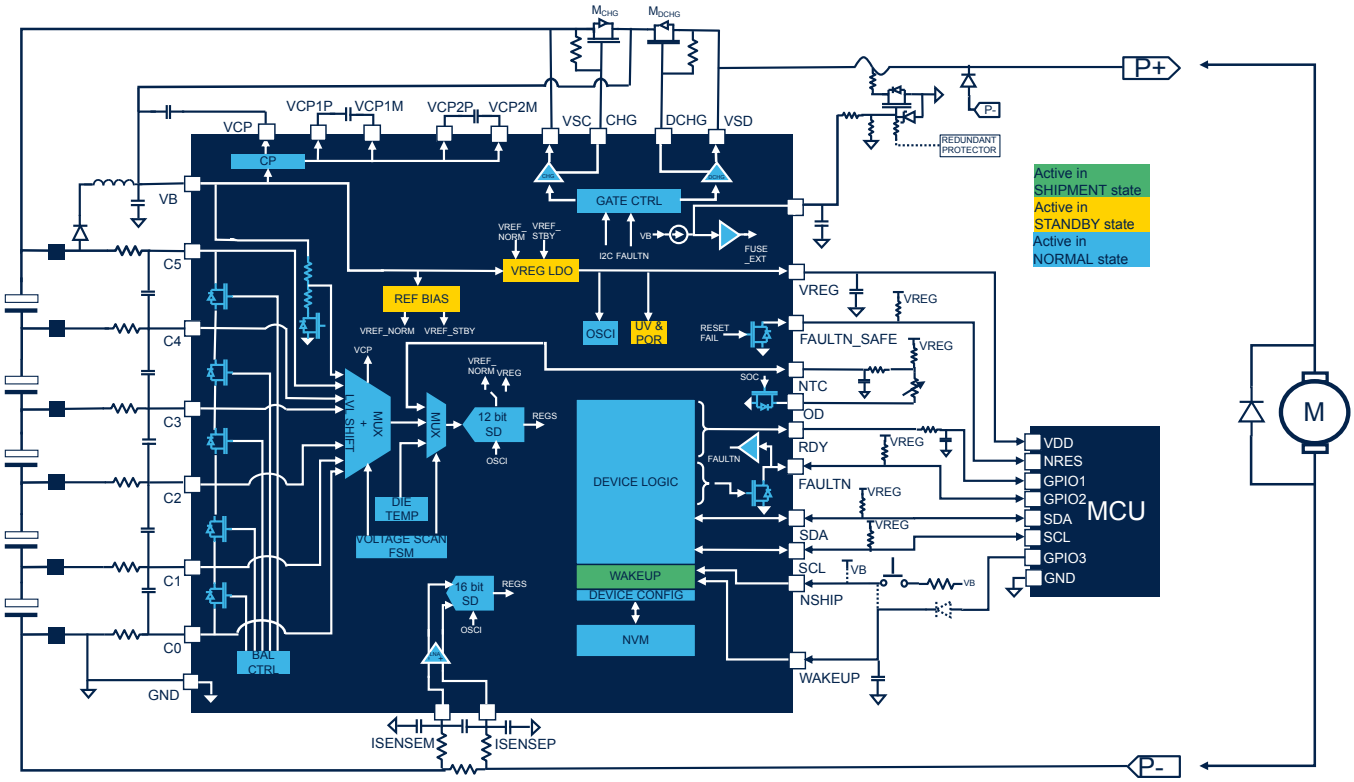
Prerelease product(s)

Pin #	Pin name	Pin function	Pin type	Internal PU/PD	Active
28	C5	Cell 5 positive terminal	Analog in		
29	C4	Cell 4 positive terminal	Analog in		
30	C3	Cell 3 positive terminal	Analog in		
31	C2	Cell 2 positive terminal	Analog in		
32	C1	Cell 1 positive terminal	Analog in		

Prerelease product(s)

1.2 Block diagram

Figure 1. **Block diagram**



GADG230620220924SA

Prerelease product(s)

2 Product electrical and thermal ratings

2.1 Operating range (OR)

Within the operating range the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation, unless the AMR are exceeded.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

Table 2. Operating ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
VB	Battery level	4.3		25	V
VCP	Charge pump tank output pin		VB+12 V		V
VCP1P, VCP2P, VCP1M, VCP2M	Charge pump flying capacitor pin	0		VCP	V
C1, C2, C3, C4	Cell terminal pins	0		VB	V
C5	Cell terminal pins	0		VB+0.6	V
C1, C2, C3, C4, C5	Cell terminal differential Voltage	1		4.7	V
VREG	3.3 V regulated voltage		3.3		V
NTC	Analog input pin	0		VREG	V
OD	Open drain pin	0		VREG	V
SDA, SCL	Digital input pins	0		VREG	V
FAULTN_SAFE, RDY, FAULTN	Digital output pin	0		VREG	V
WAKEUP	Analog input pin	0		VB	V
NSHIP	Analog input pin	0		VB	V
FUSE	Analog output pin	0		VB	V
VSD	Discharge MOS source	-1		VB+1	V
VSC	Charge MOS source	-1		VB+1	V
CHG	Charge MOS gate	VSC		Min(VCP; VSC + 12 V)	
DCHG	Discharge MOS gate	VSD		Min(VCP; VSD + 12 V)	
|ISENSEP – ISENSEM|	CSA input differential mode range	-200		300	mV
(|ISENSEPI + ISENSEM|) /2	CSA input common mode range	-200		200	mV
GND	Device ground		0		V
TM1	Device ground		0		V
TM_ENTER	Device ground		0		V
C0	Cell terminal voltage	-0.15		0.15 V	V

Prerelease product(s)

2.2 Absolute maximum ratings (AMR)

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground GND.

Table 3. Absolute maximum ratings

Symbol	Min.	Typ.	Max.	Unit
VB	-0.3		40	V
VCP	VB-0.3		VB+20	V
VCP1P	VB-0.3		VB+20	V
VCP2P	VCP1P-0.3		VB+20	V
VCP1M,VCP2M	Max(-0.3; VB-20 V)		VB+0.3	V
C1, C2, C3, C4, C5	-0.3		40	V
C(n)-C(n-1) for n=1 to 5	-0.3		40 (if VB=40 V)	V
VREG	-0.3		4.3	V
NTC	-0.3		VREG + 0.3	V
OD	-0.3		VREG + 0.3	V
SDA, SCL	-0.3		VREG + 0.3	V
FAULTN_SAFE, RDY, FAULTN	-0.3		VREG + 0.3	V
WAKEUP	-0.3		40	V
NSHIP	-0.3		40	V
FUSE	-0.3		40	V
VSC, VSD	-2		40	V
CHG	VSC		Min(VCP; VSC + 20 V)	V
DCHG	VSD		Min (VCP; VSD + 20 V)	V
ISENSEP, ISENSEM	-2		VREG + 0.3	V
GND		0		V
C0	-0.3		6	V
TM_ENTER	-0.3		6	V
TM1	-0.3		40	V

2.3 ESD ratings

Table 4 lists the device ESD ratings.

Table 4. ESD protection

Item	Parameter	Condition	Min.	Max.	Unit
All pins	HBM	Tested per AEC-Q100-002	-2	2	kV
All pins	CDM	Tested per AEC-Q100-011	-500	500	V
All pins	Latch-up	Tested per AEC-Q100-004, Class-2, Level-A	-100	100	mA

Prerelease product(s)

2.4 Thermal ratings

Table 5 lists the device thermal ratings.

Table 5. Thermal ratings

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_A	Operating and testing temperature		-40		85	°C
T_J	Operating junction temperature range		-40		120	°C
T_{stg}	Storage temperature range		-55		150	°C
R_{thJA}	Thermal resistance, junction-to-ambient	According JEDEC standard on 2s2p PCB		38		°C/W
		ON L9961 EVAL Board		TBD		°C/W

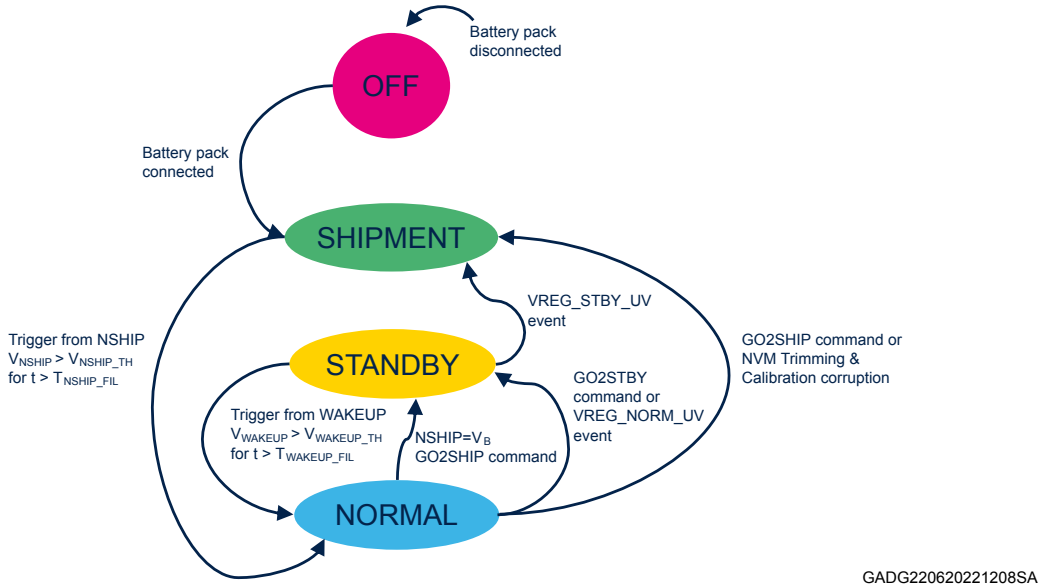
Prerelease product(s)

3 Functional description

3.1 Device funcional states

L9961 can operate in 3 different states when battery is applied: SHIPMENT - DEEP SLEEP, STANDBY or NORMAL.

Figure 2. Device FSM



3.1.1 Shipment - DEEP SLEEP

The SHIPMENT - DEEP SLEEP state is recommended for pack shipping and storage purposes. When in this state, L9961 current consumption from VB pin is reduced to just I_{VB_SHIP}, allowing long periods of inactivity to reduce battery pack discharge.

When the battery pack is first applied (L9961 receives VB supply for the first time), the device transitions to either shipment - DEEP SLEEP state or NORMAL state depending on NSHIP pin. If NSHIP is biased to VB pin, the device starts in NORMAL State, otherwise the device begins in SHIPMENT - DEEP SLEEP state.

The device can enter SHIPMENT - DEEP SLEEP from NORMAL state upon receiving a GO2SHIP command through I2C communications (GO2SHIP command is asserted by setting the GO2SHIP bit to '10' in the register 0x21) or if VREG voltage drops below the minimum level ($V_{VREG_STBY_UV}$) required to supply the device.

To avoid inadvertent reactivation, the NSHIP pin shall be set low before sending the GO2SHIP command, and it shall be kept low during the transition to SHIPMENT - DEEP SLEEP.

Sending a GO2SHIP command while NSHIP is high will cause the device to move to STANDBY state.

3.1.2 STANDBY

The STANDBY state is recommended to manage short periods of inactivity, where wakeup from MCU is needed. While in STANDBY, L9961 current consumption from VB pin is reduced to I_{VB_STBY}.

The device is powered but no system functions are available, except WAKEUP sensing and VREG regulator which operates with reduced performance charateristics While VREG is operational, the FAULTN_SAFE pin is released allowing the MCU to operate in lower power mode.

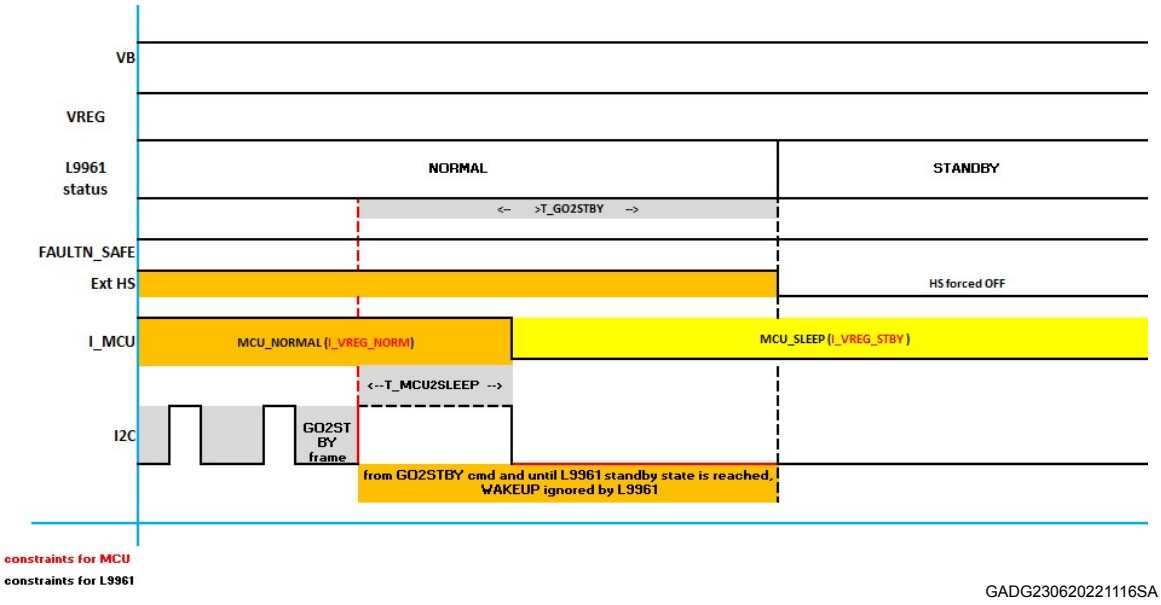
STANDBY state can be reached from NORMAL state, upon receiving a GO2STBY command through I2C communications (GO2STBY command is asserted by setting the GO2STBY bit to '10' in the register 0x22) or if VREG drops below the minimum level ($V_{VREG_NORM_UV}$) required for L9961 to correctly perform its normal features.

Prerelease product(s)

Once L9961 acknowledges the GO2STBY command, it moves to STANDBY state after $T_{GO2STBY}$. To allow a smooth transition, MCU must move to a low power state (where its average current consumption is less than I_{VREG_STBY}) within $T_{MCU2STBY}$ after sending GO2STBY command to L9961.

To avoid inadvertent reactivation, the WAKEUP pin shall be set low before sending the GO2STBY command, and it shall be kept low during the transition to STANDBY.

Figure 3. Timing diagram: transition from NORMAL to STANDBY upon GO2STBY command



GADG230620221116SA

3.1.3 NORMAL

The NORMAL state is recommended when the system is working. All IC functions are active, including voltage/temperature/current monitoring and protection. Pack relay management and I²C peripheral are also available.

L9961 current consumption from VB pin while in NORMAL state varies over time, due to the execution of periodical tasks, balancing activation/deactivation, pre-driver turn on/off events. The average current consumption can be estimated using the *"L9961_Power_Management.xlsx"* tool embedded in this document.

NORMAL state can be reached:

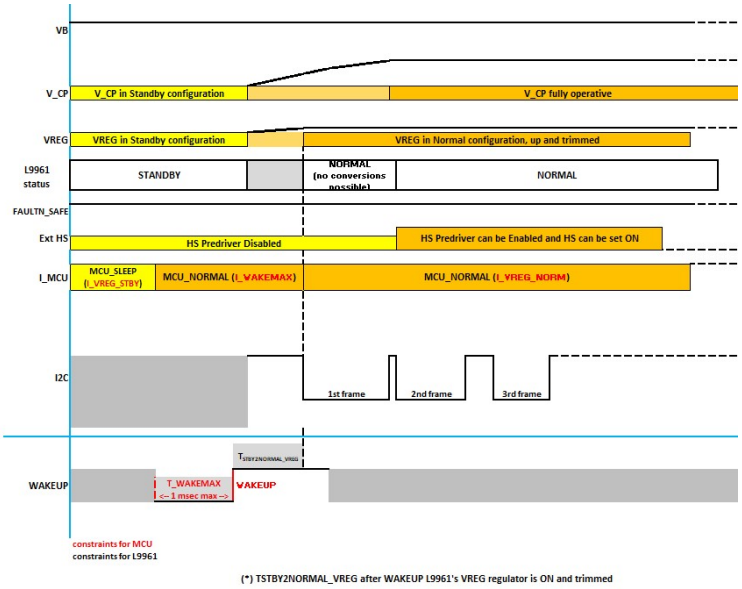
- from STANDBY state, if WAKEUP pin is higher than V_{WAKEUP_TH} for at least T_{WAKEUP_STBY}. Refer to Figure 4
  - The wakeup source can be either an external stimulus (pushbutton or other) or the system MCU asserting the WAKEUP pin via GPIO (refer to Figure 1)
  - Transition from STANDBY to NORMAL must be properly handled, as VREG regulator needs to switch from reduced performance to full power within a defined time window. Such an operation requires $T_{STBY2NORMAL}$ from the receival of the WAKEUP condition to be accomplished
  - During $T_{STBY2NORMAL}$, VREG can sustain a load current up to IWAKEMAX for a maximum $T_{WAKEMAX}$ time interval, within which the MCU must wakeup L9961
  - After $T_{STBY2NORMAL}$, the VREG regulator has reached its NORMAL state specification. After T_{I2C_READY} a RDY pulse is generated to mark the transition to NORMAL. This allows the MCU to fully operate in its normal state, respond to watchdog, serve interrupts, and so on. L9961 is capable of decoding I2C commands and receive new configurations
  - It takes $T_{CP_STARTUP}$ from the receival of WAKEUP condition for the charge pump to be ready. After $T_{CP_STARTUP,}$ L9961 will run monitoring/diagnostic tasks and manage the pre-driver stage
  - Once L9961 is in NORMAL the MCU is expected to set the WAKEUP pin low to reduce current consumption.

Prerelease product(s)

- From SHIPMENT - DEEP SLEEP state, if NSHIP pin is higher than V_{NSHIP_TH} for at least T_{WAKEUP_NSHIP}.
  - After $T_{SHIP2NORMAL}$, the VREG regulator has reached its NORMAL state specification. After T_{I2C_READY} an RDY pulse is generated to mark the transition to NORMAL. This allows the MCU to fully operate in its normal state, respond to watchdog, serve interrupts, and so on. L9961 is capable of decoding I2C commands and receives new configurations
  - MCU should still wait for $T_{CP_STARTUP}$ when out of reset, before trying to operate the pre-driver stage

Upon receival of wakeup condition, transitions to other states are masked until NORMAL state has been fully reached. Once the device enters NORMAL state, the logic starts a $T_{VREG_UV_BLK}$ blanking time on the VREG UV comparator in order to prevent erroneously flagging UV conditions that would bring L9961 back to STANDBY state.

Figure 4. Timing diagram: transition from STANDBY to NORMAL upon WAKEUP detection



GADG230620221116SA

3.1.4 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 2; *T_J according operating range of Table 5.*

Table 6. L9961 operating states electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{VB_SHIP}	Consumption from VB pin when in SHIPMENT - DEEP SLEEP	-30 °C< T_{AMB}=T_J <60 °C			2	µA
I_{VB_STBY}	Consumption from VB pin when in STANDBY	-30 °C< T_{AMB}=T_J <60°C No load on VREG			5	µA
I_{VB_NORM}	Consumption from VB pin when in NORMAL	NORMAL state, CHG/DHCG OFF, no load on VREG, no communication, Balancing OFF, NRES and FAULTN released, CSA disabled.		155	190	µA
$I_{VB_NORM_DELTA_CSA}$	Additional current consumption from VB when current ADC is converting	CSA_EN = 1 CC_ACC_EN = 1 OVC_EN = 1 SC_EN = 1		90	125	µA

Prerelease product(s)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{VB_NORM_DELTA_CONV}$	Additional current consumption from VB when Voltage ADC is continuously converting			135	190	µA
dc_{ADC_CONV}	Percentage time for which $I_{VB_NORM_DELTA_CONV}$ is active (see (1))		3		80	%
$I_{VB_NORM_DELTA_BAL}$	Additional current consumption from VB pin due to 1 Balance ON	Normal condition, additional contribution for 1 Balance ON		8	12	µA
$I_{VB_NORM_DELTA_FET_HS}$ (see(2)	Additional current consumption from VB pin due to 1 Ext FET HS ON	Normal condition, additional contribution for 1 Ext FET ON. HS configuration No ext R mounted		9	20	µA
$I_{VB_NORM_DELTA_FET_LS}$	Additional current consumption from VB pin due to 1 Ext FET LS ON	Normal condition, additional contribution for 1 Ext FET ON. LS configuration No ext R mounted		15	20	µA
I_{VB_DELTA}	Current consumption from VB pin when voltage ADC is converting	Application info		350	420	µA
	Current ADC is converting					
	Ext. FETs enabled T_{MEAS_CYCLE} = 10 ms					
$V_{VB_TRAN_NORM}$	Max allowed transient slope on VB pin	Application info			1	V/µs

1. *The current consumption linked to voltage conversion can be calculated as ($I_{VB_NORM_DELTA_CONV}$ * Duty_cycle_voltage_conversion)/100*
2. *In HS case an additional current contribution must be added to include the effect of charge pump switching activity at increased frequency. This contribution is impacted by the ext parasistic capacitances between each CP pin and GND in the range of 3 uA/pF)*

3.2 Wakeup sources (NSHIP/WAKEUP)

L9961 can be woken up via two dedicated pins:

- NSHIP can be used as wakeup from SHIPMENT - DEEP SLEEP
- WAKEUP can be used as wakeup from STANDBY.

3.2.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4; T_J according operating range of Table 7.

Table 7. VREG electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{WAKEUP_TH}	WAKEUP wakeup threshold		0.8		1.8	V
V_{NSHIP_TH}	NSHIP wakeup threshold		1		3	V
T_{WAKEUP_FIL}	WAKEUP filter time				40	µs
T_{NSHIP_FIL}	NSHIP filter time				20	µs
R_{WAKEUP_PD}	WAKEUP pulldown resistor		60	100	150	kΩ
$T_{MCU2STBY}$	Maximum delay from sending GO2STBY command to MCU in low power mode	Application info			1	ms

Prerelease product(s)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{GO2STBY}$	Maximum delay from receival of GO2STBY command to L9961 in STANDBY state	Application info	2		4	ms
$T_{GO2SHIP}$	Time delay for L9961 from received GO2SHIP command from MCU to enter SHIPMENT - DEEP SLEEP state	Application info	0		10	ms
$I_{WAKEMAX}$	VREG current capability in STANDBY to NORMAL state transition, during $T_{WAKEMAX}$ interval	Application info			15	mA
$T_{WAKEMAX}$	MCU time in NORMAL mode to send a WAKEUP command to L9961	Application info			1	ms
$T_{STBY2NORMAL}$	Time to complete STANDBY to NORMAL transition	From WAKEUP assertion to VREG_UV release			1	ms
$T_{SHIP2NORMAL}$	Time to complete SHIPMENT - DEEP SLEEP to normal transition	From NSHIP assertion to VREG UV release. No load on VREG, 4.7uF capacitance present.			5	ms
T_{I2C_READY}	I2C settling time	From WAKEUP/NSHIP assertion to I2C ready			15	ms
$T_{CP_STARTUP}$	Charge pump startup time	From VREG_UV release ($T_{VREG_UV_BLK}$ expired) to VCP in range			8	ms

3.3 VREG LDO

L9961 provides a system regulator capable of providing power to the system MCU and other peripheral devices or circuits. Performances of the regulator vary according L9961 state:

- In STANDBY State, the regulated voltage is V_{VREG_STBY} and average current capability is limited to I_{VREG_STBY}. Line/load regulation performances are reduced to $V_{VREG_LIN_REG_STBY}$ and $V_{VREG_LOAD_REG_STBY}$ respectively. VREG current limit is still active with a $I_{VREG_CURR_LIM_STBY}$ threshold
- In NORMAL State, the regulated voltage is V_{VREG_NORM}, with a I_{VREG_NORM} average current capability. Line/load regulation performances are defined by $V_{VREG_LIN_REG_NORM}$ and $V_{VREG_LOAD_REG_NORM}$ respectively. VREG current limit is active with a $I_{VREG_CURR_LIM}$ threshold.

3.3.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4*; T_J according operating range of* Table 7.

Table 8. VREG electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{VREG_NORM}	Regulated voltage	NORMAL state 10 µA<Iload<30 mA	3.23	3.3	3.37	V
I_{VREG_NORM}	Current load range	NORMAL state Design info	0.01		35	mA
$I_{VREG_CURR_LIM}$	Current limitation	NORMAL state VREG=2.7 V	40			mA
$I_{VREG_CURR_LIM_STBY}$	Current limitation	STANDBY state VREG=2.6 V	15		85	mA
$V_{VREG_LIN_REG_NORM}$	Line regulation	NORMAL state VB from 4.3V to 22 V in 100 µs Iload=100 µA, 30 mA guaranteed by design	-150		+150	mV

Prerelease product(s)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{VREG_LOAD_REG_NORM}$	Load regulation	NORMAL state Iload from 0 µA to 15 mA (and viceversa), with ideal step transition	-160		+160	mV
V_{VREG_STBY}	Regulated voltage	STANDBY state -30 °C< T_{AMB}=T_J <60 °C	2.8		3.6	V
I_{VREG_STBY}	Output current	STANDBY state -30 °C< T_{AMB}=T_J <60 °C Application info	1		300	µA
$V_{VREG_LIN_REG_STBY}$	Line reg stby	STANDBY state VB from 4.3V to 22 V in 100 µs Iload=0, 50 µA guaranteed by design	-250		+250	mV
$V_{VREG_LOAD_REG_STBY}$	Load regulation in STANDBY	STANDBY state Iload= step 0-50 µA in 100 µs	-400		+400	mV
$V_{VREG_LOAD_REG_STBY_OVL}$	Overload regulation in STANDBY	STANDBY state Iload= step 0-$I_{WAKEMAX}$, pulse lasting $T_{WAKEMAX}$ -30 °C< T_{AMB}=T_J<60 °C	2.7			V
$V_{VREG_NORM_UV}$	VREG Undervoltage threshold in NORMAL state		2.6	2.7	2.9	V
$T_{VREG_UV_FIL}$	VREG UV filter time in NORMAL state			20		µs
$T_{VREG_UV_BLK}$	VREG UV blanking time upon transition to NORMAL state		8			ms
$V_{VREG_STBY_UV}$	VREG Undervoltage threshold in STANDBY state	STANDBY state	2.1	2.5	2.8	V
C_{REG}	External LDO capacitance	Application info, required for stability	-20%	4.7	+20%	µF

3.4 Voltage conversion routine

While in NORMAL state, L9961 cyclically executes the voltage conversion routine as shown in Figure 6. Task execution time is T_{ADCV_CONV}, which is the sum of the individual step duration:

- N_{CELL} represents the number of enabled cells. The T_{CELL_FILTER} filter time is applied to each cell conversion. At least 3 cells must be converted
- The T_{CELL_FILTER} filter time is also applied to VB pin conversion (if enabled)
- The T_{TEMP_FILTER} filter time is applied to NTC conversion (if enabled)
- The T_{TEMP_FILTER} filter time is applied to Die Temperature conversion, which is always performed
- The task is scheduled to run every T_{MEAS_CYCLE} (programmable in TCYCLE field). Changing configuration parameters while a conversion is ongoing may result in inadvertent faults and reactions. MCU is supposed to disable the voltage conversion routine programming T_{MEAS_CYCLE} = 0x0 before applying a new configuration set.

Prerelease product(s)

Figure 5. **Voltage conversion routine steps**



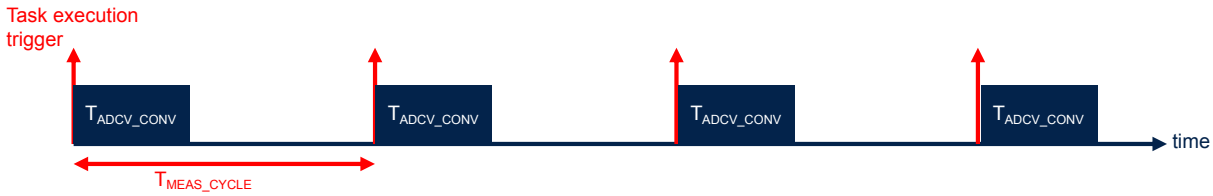
GADG220620221212SA

Table 9. **Voltage conversion routine execution parameters**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{MEAS_CYCLE}	Programmable voltage conversion routine execution period (5 bit) $T_{MEAS_{CYCLE}} = 10ms*CODE$	-	10	-	310	ms

Task execution period T_{MEAS_CYCLE}, must always be greater than the task duration. In case the task execution period is programmed shorter than the task duration, this will result in the task being executed with random periodicity.

Figure 6. **Correct management of the task execution periodicity**



GADG220620221219SA

3.4.1 Cell voltage monitor (Cx)

During cells voltage monitoring step, the voltage conversion routine measures differential voltages at Cx pins and stores results in VCELL<x> registers. The digital sum of cells is stored in the VCELL_SUM_MEAS register.

A cell is converted only if its corresponding VCELL<x>_EN bit is enabled. By default, all cells are disabled. At least 3 cells must be enabled in order to guarantee proper operation.

If less than 5 cells are used:

- Mount the cells starting from the bottom-most (C0-C1)

Measurements are compared to programmable thresholds to detect the failures listed in Table 12.

Table 10. **Cell voltage monitor diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell UV	If a cell voltage falls below VCELL_UV_TH, the corresponding UV counter is incremented by 1	The CELL<x>_UV flag is set	If a cell voltage raises above VCELL_UV_TH, the corresponding UV counter is decremented by 1.	The discharge FET is restored to the status defined by the DCHG_ON bit	VCELL<x>_EN masks measurement execution. The UV flag of a disabled cell can always be cleared

Prerelease product(s)

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell UV	If the UV counter reaches VCELL_UV_CNT_TH, it saturates and the cell UV fault is acknowledged.	The discharge FET is turned OFF	If the UV counter reaches zero, the cell UV flag can be cleared by MCU	FAULTN line is released	CELL_UV_PRDRV_MSK masks reaction on DCHG pin
		FAULTN line is asserted			CELL_UV_FAULTN_MSK masks reaction on FAULTN pin
Cell severe UV	If a cell voltage falls below VCELL_SEVERE_UV_TH, the severe UV fault is acknowledged	The CELL<x>_SEVERE_UV flag is set	If a cell voltage raises above VCELL_SEVERE_UV_TH, the cell severe UV flag can be cleared by MCU	The discharge FET is restored to the status defined by the DCHG_ON bit	VCELL<x>_EN masks measurement execution. The severe UV flag of a disabled cell can always be cleared
		The discharge FET is turned OFF		FUSE pre-driver is disabled	CELL_SEVERE_UV_PRDRV_MSK masks reaction on DCHG pin
		FUSE pre-driver is enabled		FAULTN line is released	CELL_SEVERE_UV_FUSE_MSK masks reaction on FUSE pin
		FAULTN line is asserted			CELL_SEVERE_UV_FAULTN_MSK masks reaction on FAULTN pin
Cell OV	If a cell voltage raises above VCELL_OV_TH, the corresponding OV counter is incremented by 1	The CELL<x>_OV flag is set	If a cell voltage falls below VCELL_OV_TH, the corresponding OV counter is decremented by 1.	The charge FET is restored to the status defined by the CHG_ON bit	VCELL<x>_EN masks measurement execution. The OV flag of a disabled cell can always be cleared
	If the OV counter reaches VCELL_OV_CNT_TH, it saturates and the cell OV fault is acknowledged.	The charge FET is turned OFF	If the OV counter reaches zero, the cell OV flag can be cleared by MCU	FAULTN line is released	CELL_OV_PRDRV_MSK masks reaction on CHG pin
		FAULTN_SAFE is pulled low for $T_{FAULTN_SAFE_LOW}$ (if a pulse on FAULTN_SAFE pin was not already generated after a previous not masked and not cleared Cell OV / Cell Severe OV detection)			CELL_OV_RST_MSK masks reaction FAULTN_SAFE pin
		FAULTN line is asserted			CELL_OV_FAULTN_MSK masks reaction on FAULTN pin
Cell severe OV	If a cell voltage raises above VCELL_SEVERE_OV_TH, the severe OV fault is acknowledged	The CELL<x>_SEVERE_OV flag is set	If a cell voltage falls below VCELL_SEVERE_OV_TH, the cell severe OV flag can be cleared by MCU	The charge FET is restored to the status defined by the CHG_ON bit	VCELL<x>_EN masks measurement execution. The severe OV flag of a disabled cell can always be cleared
		The charge FET is turned OFF		FUSE pre-driver is disabled	CELL_SEVERE_OV_PRDRV_MSK masks reaction on CHG pin
		FUSE pre-driver is enabled		FAULTN line is released	CELL_SEVERE_OV_FUSE_MSK masks reaction on FUSE pin

Prerelease product(s)

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell severe OV	If a cell voltage raises above VCELL_SEVERE_OV_TH, the severe OV fault is acknowledged	FAULTN_SAFE is pulled low for $T_{FAULTN_SAFE_LOW}$ (if a pulse on FAULTN_SAFE pin was not already generated after a previous not masked and not cleared Cell OV / Cell Severe OV detection)	If a cell voltage falls below VCELL_SEVERE_OV_TH, the cell severe OV flag can be cleared by MCU	FAULTN line is released	CELL_SEVERE_OV_RST_MSK masks reaction FAULTN_SAFE pin
		FAULTN line is asserted			CELL_SEVERE_OV_FAULTN_MSK masks reaction on FAULTN pin
Cell balance UV	If a cell voltage falls below VCELL_BAL_UV_TH, the corresponding Bal UV counter is incremented by 1	The BAL<x>_UV flag is set	If a cell voltage raises above VCELL_BAL_UV_TH, the corresponding Bal UV counter is decremented by 1.	The Balancing FET is restored to the status defined by the corresponding BAL<x>_ON bit	VCELL<x>_EN masks measurement execution. The Bal UV flag of a disabled cell can always be cleared
	If the Bal UV counter reaches VCELL_BAL_UV_CNT_TH, it saturates the Bal UV fault is acknowledged	Any ongoing balancing is stopped on the affected cell, regardless of BAL<x>_ON bit	If the Bal UV counter reaches zero, the Bal UV flag can be cleared by MCU	FAULTN line is released	BAL_UV_BAL_MSK masks reaction on balancing
		FAULTN line is asserted			BAL_UV_FAULTN_MSK masks reaction on FAULTN pin

3.4.1.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: VB according operating range of Table 4; T_J according operating range of Table 7.

Table 11. Cell voltage monitor electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CELL_RANGE}	Cell voltage input measurement range	Design info	1		4.7	V
V_{CELL_RES}	Cell voltage measurement resolution	Design info, effective range [0-5]V		1.22 (5 V/2^{12})		mV
N_{BIT}	ADC bit number	Design info		12		bit
I_{CELL_LEAK}	Cx leakage current	ADC not converting			500	nA
$V_{CELLERR1}$	ADC total conversion error range 1	1 V ≤ V_{CELL} < 1.5 V -40 °C< T_J<120 °C	-25		25	mV
$V_{CELLERR2}$	ADC total conversion error range 2	1.5 V ≤ V_{CELL} ≤ 4.5 V -40 °C< T_J<105 °C	-15		15	mV
$V_{CELLERR3}$	ADC total conversion error range 3	4.5 V ≤ V_{CELL} ≤ 4.7 V -40 °C< T_J<120°C	-25		25	mV
$V_{CELLERR4}$	ADC total conversion error range 4	1.5 V ≤ VCELL ≤ 4.5 V 105 °C < T_J < 120 °C	-25		25	mV
V_{CELL_NOISE}	Cell conversion noise			1		LSB rms
$T_{CELL_FILTER1}$	Cell and VB acquisition filter time			0.8		ms

Prerelease product(s)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{CELL_FILTER2}$	Cell and VB acquisition filter time			1.31		ms
$T_{CELL_FILTER3}$	Cell and VB acquisition filter time			4.38		ms
$T_{CELL_FILTER4}$	Cell and VB acquisition filter time			16.67		ms
$V_{CELL_OV_TH}$	Programmable cell OV fault threshold (8 bit) $V_{CELL_{OV_{TH}}} = 16V_{CELL_RES}{}^{*}CODE$		0		5	V
$N_{CELL_OV_CNT_TH}$	Programmable cell OV event counter threshold (4 bit)		1		15	events
$V_{CELL_SEVERE_OV_DELTA_TH}$	Programmable cell severe OV threshold (positive delta in respect to cell OV threshold, 8 bit) $V_{CELL_{SEVERE_{OV_{TH}}}} = V_{CELL_{OV_{TH}}} + 16V_{CELL_RES}{}^{*}CODE$ In case of overflow, the $V_{CELL_{SEVERE_{OV_{TH}}}}$ is saturated to the max. specified value		0		5	V
$V_{CELL_UV_TH}$	Programmable cell UV fault threshold (8 bit) $V_{CELL_{UV_{TH}}} = 16V_{CELL_RES}{}^{*}CODE$		0		5	V
$N_{CELL_UV_CNT_TH}$	Programmable cell UV event counter threshold (4 bit)		1		15	events
$V_{CELL_SEVERE_UV_DELTA_TH}$	Programmable cell severe OV threshold (negative delta in respect to cell UV threshold, 8 bit) $V_{CELL_{SEVERE_{UV_{TH}}}} = V_{CELL_{UV_{TH}}} - 16V_{CELL_RES}{}^{*}CODE$ In case of underflow, the $V_{CELL_{SEVERE_{UV_{TH}}}}$ is saturated to the min. specified value		0		5	V
$V_{CELL_BAL_UV_DELTA_TH}$	Programmable balancing UV threshold (positive delta in respect to cell UV threshold, 8 bit) $V_{CELL_{BAL_{UV_{TH}}}} = V_{CELL_{UV_{TH}}} + 16V_{CELL_RES}{}^{*}CODE$ In case of overflow, the $V_{CELL_{SEVERE_{UV_{TH}}}}$ is saturated to the max. specified value		0		5	V
$N_{CELL_BAL_UV_CNT_TH}$	Programmable balance UV event counter threshold (4 bit)		1		15	events

Prerelease product(s)

3.4.2 Battery stack monitor (VB)

The battery stack monitor, (VB), of the voltage conversion routine monitors the battery stack voltage measuring the VB pin through an internal divider.

This function is enabled by programming the corresponding VB_EN I2C bit: if disabled, this step is skipped. To limit power consumption, the internal voltage divider is connected to VB pin at the beginning of the Section 3.4 Voltage conversion routine and it is disconnected right after the VB measurement step is completed.

Stack voltage measurements are stored in the VB_MEAS register and compared to programmable thresholds in order to detect the failures listed in Table 12.

Table 12. Battery stack monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VB UV	If VB voltage falls below VB_UV_TH, the corresponding UV counter is incremented by 1	The VB_UV flag is set	If VB voltage raises above VB_UV_TH, the corresponding UV counter is decremented by 1.	The discharge FET is restored to the status defined by the DCHG_ON bit	VB_EN masks measurement execution. When disabled, the VB_UV flag can always be cleared upon read
	If the UV counter reaches VB_UV_CNT_TH, it saturates and the VB UV fault is acknowledged	The discharge FET is turned OFF	If the UV counter reaches zero, the VB_UV flag can be cleared by MCU	FAULTN line is released	VB_UV_PRDRV_MSK masks reaction on DCHG pin
		FAULTN line is asserted			VB_UV_FAULTN_MSK masks reaction on FAULTN pin
VB OV	If VB voltage raises above VB_OV_TH, the corresponding OV counter is incremented by 1	The VB_OV flag is set	If VB voltage falls below VB_OV_TH, the corresponding OV counter is decremented by 1.	The charge FET is restored to the status defined by the corresponding I2C bit	VB_EN masks measurement execution. When disabled, the VB_OV flag can always be cleared upon read
	If the OV counter reaches VB_OV_CNT_TH, it saturates and the VB OV fault is acknowledged	The charge FET is turned OFF	If the OV counter reaches zero, the VB OV flag can be cleared by MCU	FAULTN line is released	VB_OV_PRDRV_MSK masks reaction on CHG pin
		FAULTN_SAFE is pulled low for $T_{FAULTN_SAFE_LOW}$			VB_OV_RST_MSK masks reaction FAULTN_SAFE pin
		FAULTN line is asserted			VB_OV_FAULTN_MSK masks reaction on FAULTN pin
VB vs. sum of cells plausibility fail	If the absolute value of the difference between VB_MEAS and VCELL_SUM is greater than VB_VSUM_MAX_DIFF_TH, the plausibility check fail is acknowledged	The VB_SUM_CHECK_FAIL flag is set	If the absolute value of the difference between VB_MEAS and VCELL_SUM falls below the VB_VSUM_MAX_DIFF_TH, the VB_SUM_CHECK_FAIL flag can be cleared by MCU	The charge FET is restored to the status defined by the CHG_ON bit	VB_EN masks measurement execution. When disabled, the VB_SUM_CHECK_FAIL flag can always be cleared upon read
		Both charge and Discharge FETs are turned OFF		The discharge FET is restored to the status defined by the DCHG_ON bit	VB_SUM_CHEC_PRDRV_MSK masks reaction on CHG/ DCHG pins
		Balancing is interrupted on all cells		FUSE pre-driver is disabled	VB_SUM_CHEC_FUSE_MSK masks reaction on FUSE pin
		FUSE pre-driver is enabled		Balancing FETs are restored to the status defined by the corresponding BAL<x>_ON bit	VB_SUM_CHEC_BAL_MSK masks reaction on balancing

Prerelease product(s)

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VB vs. sum of cells plausibility fail	If the absolute value of the difference between VB_MEAS and VCELL_SUM is greater than VB_VSUM_MAX_DIFF_TH, the plausibility check fail is acknowledged	FAULTN line is asserted	If the absolute value of the difference between VB_MEAS and VCELL_SUM falls below the VB_VSUM_MAX_DIFF_TH, the VB_SUM_CHECK_FAIL flag can be cleared by MCU	FAULTN line is released	VB_SUM_CHECK_FAULTN_MSK masks reaction on FAULTN pin

3.4.2.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4*; T_J according operating range of* Table 7.

Table 13. Battery stack monitor external parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{B_RANGE}	VB voltage input measurement range	Design info	4.3		25	V
V_{B_RES}	VB voltage measurement resolution	Design info		6.1 (25 V/2^{12})		mV
N_{BIT}	ADC bit number	Design info		12		bit
V_{BERR_1}	VB voltage measurement total	4.3 V<VB<7.5 V -40 °C< T_J<105 °C	-150		150	mV
V_{BERR_2}	VB voltage measurement total	7.5 V<VB<22.5 V -40 °C< T_J<105 °C	-100		100	mV
V_{BERR_3}	VB voltage measurement total	22.5 V<VB<25 V -40 °C< T_J<105 °C	-150		150	mV
$V_{B_OV_TH}$	Programmable VB OV fault threshold (8 bit) $V_{B_{OV_{TH}}} = 16V_{B_RES}{*}CODE$	Tested by SCAN	0		25	V
$N_{VB_OV_CNT_TH}$	Programmable VB OV event counter threshold (4 bit)	Tested by SCAN	1		15	events
$V_{B_UV_TH}$	Programmable VB UV fault threshold (8 bit) $V_{B_{UV_{TH}}} = 16V_{B_RES}{*}CODE$	Tested by SCAN	0		25	V
$N_{VB_UV_CNT_TH}$	Programmable VB UV event counter threshold (4 bit)	Tested by SCAN	1		15	events
$V_{B_SUM_MAX_DIFF_TH}$	Programmable plausibility check threshold between VB and sum of cells (8 bit)	Tested by SCAN	0		25	V

3.4.3 Cell temperature monitor (NTC)

The NTC cell temperature monitoring voltage conversion routine monitors pack temperature by sensing the NTC pin. This function is enabled by programming the NTC_EN bit: if disabled, no conversion occurs.

When NTC_EN = 1, the OD open-drain is switched ON at the beginning of the voltage conversion routine, prior to the cells step execution. This allows voltage on the NTC pin to settle before NTC acquisition is performed. Once the NTC is completed, the OD open-drain switch is released, reducing overall current consumption from VREG.

Prerelease product(s)

NTC measurements are stored in the NTC_MEAS register and are compared to programmable thresholds in order to detect the failures listed in Table 16.

Table 14. NTC temperature monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
NTC OT	If NTC voltage falls below NTC_OT_TH, the corresponding OT counter is incremented by 1	The NTC_OT flag is set	If NTC voltage raises above NTC_OT_TH, the corresponding OT counter is decremented by 1.	The charge FET is restored to the status defined by the CHG_ON bit	NTC_EN masks measurement execution. The OT flag of a disabled NTC can always be cleared
	If the OT counter reaches NTC_OT_CNT_TH, the NTC OT fault is acknowledged	The charge FET is turned OFF	If the OT counter reaches zero, the NTC OT flag can be cleared by MCU	FAULTN line is released	NTC_OT_PRDRV_MSK masks reaction on CHG pin
		FAULTN line is asserted			NTC_OT_FAULTN_MSK masks reaction on FAULTN pin
Severe NTC OT	If a NTC voltage falls below NTC_SEVERE_OT_TH, the severe OT fault is acknowledged	The NTC_SEVERE_OT flag is set	If NTC voltage raises above NTC_SEVERE_OT_TH, the severe OT flag can be cleared by MCU	The charge FET is restored to the status defined by the CHG_ON bit	NTC_EN masks measurement execution. When disabled, the severe OT flag can always be cleared
		Both charge and discharge FETs are turned OFF		The discharge FET is restored to the status defined by the DCHG_ON bit	NTC_SEVERE_OT_PRDRV_MSK masks reaction on CHG/ DCHG pins
		Balancing is interrupted on all cells		FUSE pre-driver is disabled	NTC_SEVERE_OT_FUSE_MSK masks reaction on FUSE pin
		FUSE pre-driver is enabled		Balancing FETs are restored to the status defined by the corresponding BAL<x>_ON bit	NTC_SEVERE_OT_BAL_MSK masks reaction on balancing
		FAULTN line is asserted		FAULTN line is released	NTC_SEVERE_OT_FAULTN_MSK masks reaction on FAULTN pin
NTC UT	If NTC voltage raises above NTC_UT_TH, the corresponding UT counter is incremented by 1	The NTC_UT flag is set	If NTC voltage falls below NTC_UT_TH, the corresponding UT counter is decremented by 1.	The charge FET is restored to the status defined by the corresponding I2C bit	NTC_EN masks measurement execution. The UT flag of a disabled NTC can always be cleared
	If the UT counter reaches NTC_UT_CNT_TH, the NTC UT fault is acknowledged	The Charge FET is turned OFF	If the UT counter reaches zero, the NTC_UT flag can be cleared by MCU	FAULTN line is released	NTC_UT_PRDRV_MSK masks reaction on CHG pin
		FAULTN line is asserted			NTC_UT_FAULTN_MSK masks reaction on FAULTN pin

3.4.3.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

VB according operating range of Table 4 *;* T_J *according operating range of* Table 7.

Prerelease product(s)

Prerelease product(s)

Table 15. NTC measurement parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
V_{NTC_RANGE}	NTC pin voltage input measurement range	Ratiometric, design info	0.2		V_{VREG}	V	NTC
V_{NTC_RES}	Cell voltage measurement resolution	Design info		0.806 ($V_{VREG}/2^{12}$)		mV	NTC
N_{BIT}	ADC bit number	Design info		12		bit	NTC
I_{NTC_LEAK}	NTC leakage current	ADC not converting			150	nA	NTC
$V_{NTC_GAIN_ERR}$	NTC gain error	0.2 V ≤ VNTC ≤ VREG -40 °C< T_J<105 °C	-0.8		+0.8	%	NTC
$V_{NTC_OFFSET_ERR}$	NTC Offset Error		-2		+2	LSB	NTC
V_{NTC_NOISE}	NTC Conversion noise			1		LSB rms	NTC
T_{TEMP_FILTER}	NTC acquisition filter time	Tested by SCAN		0.8		ms	NTC
$V_{NTC_OT_TH}$	Programmable NTC OT threshold (12 bit) $V_{NTC_{OTTH}} = V_{NTC_RES}{}^{*}CODE$	Tested by SCAN	0		V_{VREG}	V	NTC
$N_{NTC_OT_CNT_TH}$	Programmable NTC OT event counter threshold (4 bit)	Tested by SCAN	1		15	events	NTC
$V_{NTC_SEVERE_OT_DELTA_TH}$	Programmable NTC severe OT threshold (negative delta in respect to NTC OT Threshold, 12 bit) $V_{NTC_{SEVERE_{OT_{TH}}}} = V_{NTC_{OT_{TH}}} - V_{NTC_RES}{}^{*}CODE$ In case of underflow, the $V_{NTC_{SEVERE_{OT_{TH}}}}$ is saturated to the min specified value	Tested by SCAN	0		V_{VREG}	V	NTC
$V_{NTC_UT_TH}$	Programmable NTC UT threshold (12 bit) $V_{NTC_{UTTH}} = V_{NTC_RES}{}^{*}CODE$	Tested by SCAN	0		V_{VREG}	V	NTC
$N_{NTC_UT_CNT_TH}$	Programmable NTC UT event counter threshold (4 bit)	Tested by SCAN	1		15	events	NTC

3.4.4 Die temperature monitor (T_J)

The die temperature step of the voltage conversion routine monitors L9961 junction temperature. This step is always enabled. The die temperature is encoded according to the following formula:

Die temperature measurement

$$T_j[°C] = 343.165 - 0.196{}^{*}DIE_TEMP_MEAS \quad (1)$$

Die temperature measurements are stored in the DIE_TEMP_MEAS register and compared to a programmable threshold in order to detect the failures listed in Table 18.

Table 16. Die temperature monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
DIE OT	If Die temperature raises above T_{OT_TH}, the DIE_OT fault is acknowledged	The DIE_OT flag is set	If Die temperature falls below T_{OT_TH} – T_{OT_HYST}, the DIE_OT flag can be cleared by MCU upon read	Charge FET is restored to the status defined by the CHG_ON bit	DIE_OT_PRDRV_MSK masks reaction on CHG/DCHG pins

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
DIE OT	If Die temperature raises above T_{OT_TH}, the DIE_OT fault is acknowledged	Both charge and discharge FETs are turned OFF	If Die temperature falls below $T_{OT_TH} - T_{OT_HYST}$, the DIE_OT flag can be cleared by MCU upon read	The discharge FET is restored to the status defined by the DCHG_ON bit	DIE_OT_BAL_MSK masks reaction on balancing
		Balancing is interrupted on all cells		Balancing FETs are restored to the status defined by the corresponding BAL<x>_ON bit	DIE_OT_FAULTN_MSK masks reaction on FAULTN pin
		FAULTN line is asserted		FAULTN line is released	

3.4.4.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4*;* T_J *according operating range of* Table 7.

Table 17. Die temperature monitor electrical parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{j_ERR}	Die temperature total conversion error	-10	-	10	°C
T_{OT_TH}	Overtemperature threshold	150	-		°C
T_{OT_HYST}	Overtemperature threshold hysteresis	5	-	15	°C

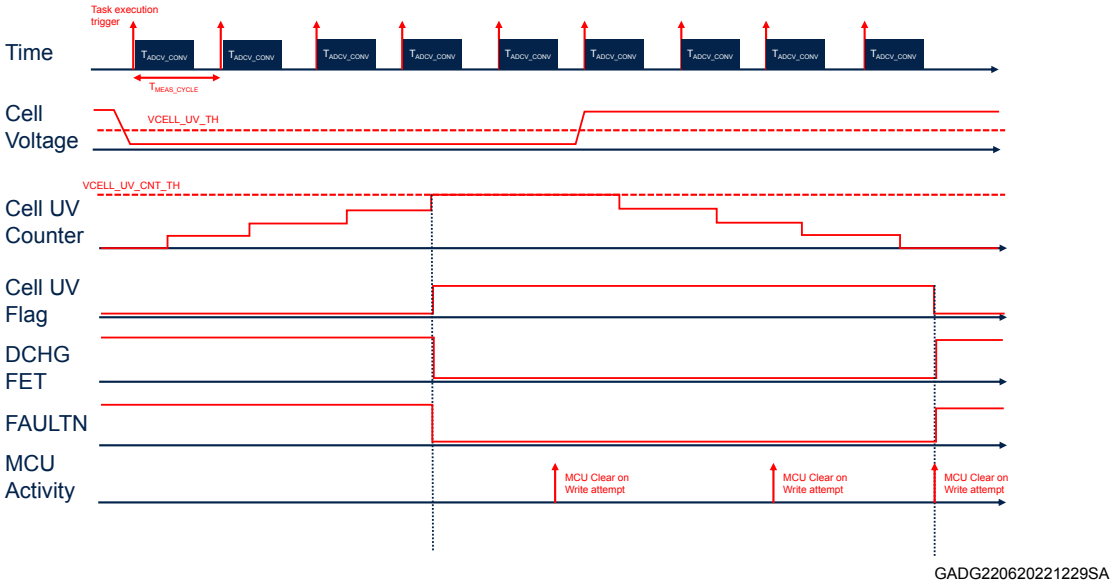
3.4.5 Diagnostics principle

The following example on Cell UV detection applies to all diagnostics featuring a programmable event counter. The counter implements a symmetric hysteresis:

- Each fault is asserted if the corresponding threshold is overcome. In such a case L9961 puts in place the programmed reactions, based on the masking bits
- Fault counter is saturated to the programmed threshold as long as fault is still present. During such an interval, any attempt to clear the fault status is discarded. To avoid inadvertent fault detection, fault counter threshold is saturated to 1 on the lower bound, meaning that at least one fault event must occur for fault detection. Writing a ‘0’ to any I2C fault counter threshold will result in internal threshold being clamped to ‘1’
- When fault is removed and event counter reaches zero, the fault flag can be cleared on write by MCU. In such a case, system is brought back to functional state.

Prerelease product(s)

Figure 7. Example of cell UV detection



Prerelease product(s)

3.5 Current conversion routine

The current conversion routine can be enabled by programming the CSA_EN bit: if disabled, the ADC, the monitoring functions and coulomb counting are not available.

Enabling the current conversion routine increases VB current consumption by $I_{VB_NORM_DELTA_CSA}$.

3.5.1 Current sense ADC (ISENSEP/ISENSEM)

L9961 integrates a current sense amplifier and a fully differential sigma-delta ADC, capable of performing continuous acquisition of the pack current using an external shunt resistor connected between ISENSEP and ISENSEM pins.

Each sample acquisition lasts T_{CUR_FILTER} (programmable via T_CUR_FILTER field) and a new acquisition starts upon completion of the previous conversion.

The latest sample acquired by the ADC is available in the CUR_INST_MEAS register, encoded in 2's complement.

The CSA comes with a native gain error of CSA_{GAIN_ERR}. To furtherly improve the accuracy, L9961 offers the possibility to perform end of line calibration using a single setpoint. By programming the CSA_GAIN_FACTOR register, the gain error can be reduced down to $CSA_{GAIN_ERR_CAL}$.

The end of line calibration procedure is the following:

1. Read the CSA_GAIN_FACTOR register and store the factory correction factor $K_{GAIN_FACTORY}$ in a temporary variable

CSA_GAIN_FACTOR register is decoded as follows:

CSA_GAIN_FACTOR decode

$$CSA_GAIN_FACTOR_{decimal} = b[15]*2^{0} + b[14]*2^{-1} + b[13]*2^{-2} + \ldots + b[0]*2^{-15} \quad (2)$$

1. Force a precise and stable V_{CSA_CAL} voltage on the ISENSEP-ISENSEM pair
2. Enable the CSA and the Coulomb counter by programming CSA_EN = 1 and CC_ACC_EN = 1
3. Let the Coulomb counter acquire at least 30 samples in order to eliminate any superimposed noise
4. Download the Coulomb counter data as described in Section 3.5.2 Coulomb counting and extract the V_{CSA_MEAS} average value
5. Calculate the gain correction factor K_{GAIN_CAL}

CSA gain correction factor definition

$$K_{GAIN_{CAL}} = \frac{V_{CSA_{CAL}}}{V_{CSA_{MEAS}}} \quad (3)$$

1. Calculate the End Of Line correction factor K_{GAIN_EOL} and write it into the CSA_GAIN_FACTOR register

CSA end of line correction factor calculation

$$K_{GAIN_{EOL}} = K_{GAIN_{FACTORY}} K_{GAIN_{CAL}} \quad (4)$$

1. Push the data into the NVM following the procedure described in the Non-Volatile Memory (NVM)

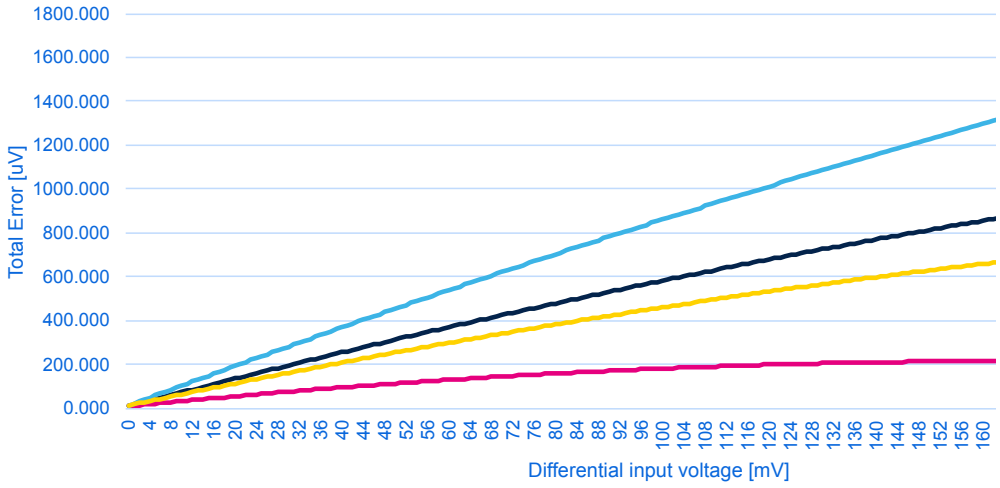
Total conversion error (TCE) can be computed as the following formula (see CSA total conversion error) where the gain error CSA_{GAIN} can be either CSA_{GAIN_ERR} or $CSA_{GAIN_ERR_CAL}$ depending if end of line calibration is performed or not.

Prerelease product(s)

CSA total conversion error

$$\begin{cases} |TCE| = TCE_{25°C} + \frac{\Delta TCE}{\Delta T}|T_{AMB} - 25°C| \\ TCE_{25°C} = \left|CSA_{OFFSET_{ERR}}\right| + |CSA_{GAIN}||V_{ISENSEP} - V_{ISENSEM}| \\ \quad + \left|CSA_{INL_{ERR}}\right|^{*}\left|\frac{\left(|V_{ISENSEP} - V_{ISENSEM}| - \left|V_{DIFF_{RANGE}}\right|\right)^{*}|V_{ISENSEP} - V_{ISENSEM}|}{\left(\frac{V_{DIFF_{RANGE}}}{2}\right)^{2}}\right| \\ \frac{\Delta TCE}{\Delta T} = \left|CSA_{OFFSET_{ERRTHERMAL_{DRIFT}}}\right| + \left|CSA_{GAIN_{ERRTHERMAL_{DRIFT}}}\right|^{*}\frac{|V_{ISENSEP} - V_{ISENSEM}|}{\left|V_{DIFF_{RANGE}}\right|} \end{cases} \quad (5)$$

Figure 8. Current sense ADC total conversion error



GADG120820221205SA

3.5.1.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: VB according operating range of Table 4; T_J according operating range of Table 7.

Table 18. Current sense ADC electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DIFF_RANGE}	ADC differential input range for coulomb counting and overcurrent monitor ISENSEP-ISENSEM	Design info	-200		200	mV
$V_{DIFF_RANGE_EXT}$	ADC extended differential input range for short-circuit in discharge protection ISENSEP-ISENSEM	Design info	0		300	mV
V_{CM_RANGE}	ADC common mode input range (ISENSEP+ISENSEM)/2	Design info	-200		200	mV
T_{CUR_FILTER}	Programmable current Sense sample acquisition time (2 bit)	Tested by SCAN	4.22		33.79	ms

Prerelease product(s)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	$T_{CUR_{FILTER}} = 528us*2^{(3+CODE)}$					
N_{BIT_CSA}	ADC bit number: encoding is in 2's complement	Design info		16		bit
V_{CUR_RES}	CSA resolution	Design info		$V_{DIFF_RANGE_EXT}$ /2^{NBIT_CSA-1}		mV
I_{CSA_LEAK}	ISENSEP, ISENSEM input leakage differential current	ISENSEP, ISENSEM in [0-3.3] V range			190	nA
$R_{CSA_IN_DIFF}$	ISENSEP, ISENSEM differential input impedance	ISENSEP-ISENSEM falls within V_{DIFF_RANGE} Guaranteed by design	400			kΩ
$CSA_{GAIN_ERR_CAL}$	ADC post-calibration gain error	Post-soldering After customer EOL calibration using a single point T_{AMB} = 25 °C 2.6 mV < | ISENSEP-ISENSEM | < V_{DIFF_RANGE}	-0.1		0.1	%
CSA_{GAIN_ERR}	ADC native gain error	Post-soldering T_{AMB} = 25 °C 2.6 mV < | ISENSEP-ISENSEM | < V_{DIFF_RANGE}	0.5		0.5	%
$CSA_{GAIN_ERR_THERM_DRIFT}$	Gain error thermal drift	Guaranteed by characterization ISENSEP-ISENSEM falls within V_{DIFF_RANGE}	-1		+1	LSB/°C
CSA_{OFFSET_ERR}	ADC native offset error	Long term average over 100 samples using Coulomb counter T_{AMB} = 25 °C	-1		1	LSB
$CSA_{LOW_RANGE_ERR}$	Total conversion error in low range, including post-soldering, ageing effects and INL	0 mV < | ISENSEP-ISENSEM | ≤ 2.6 mV Guaranteed by test bench characterization T_{AMB} = 25 °C	-2		+2	LSB
$CSA_{OFFSET_ERR_THERM_DRIFT}$	Offset error thermal drift	Guaranteed by characterization	-0.007		0.007	LSB/°C
V_{CSA_NOISE}	+/- 3σ distribution over 100 samples	Guaranteed by characterization	-7		7	LSB
CSA_{INL_ERR}	ADC integral non linearity error	Guaranteed by characterization	-8		8	LSB

Prerelease product(s)

3.5.2 Coulomb counting

To enable the accumulation function, the CC_ACC_EN bit must be set. When Coulomb counting is active, current samples are continuously accumulated in the CC_ACC register, while the CC_SAMPLE_CNT counts the number of samples stored in the accumulator. Disabling the Coulomb counting will cause accumulator and sample counter reset: to avoid loss of information, the MCU is supposed to download the Coulomb counter information before disabling it.

MCU must periodically poll the Coulomb counter to retrieve the charge information. The following procedure has to be implemented in order to guarantee proper data synchronization between accumulator and sample counter:

1. MCU writes CC_ACC_MSB register with 0xFFFF data[end]
   a. The accumulator is cleared upon write
   b. A snapshot of the internal sample counter and accumulator is loaded into CC_SAMPLE_CNT, CC_ACC_MSB and CC_ACC_LSB fields
   c. The shadow register of the internal sample counter is meanwhile reset.
2. MCU reads the CC_ACC_MSB register
3. MCU reads the CC_ACC_LSB_CNTR register.

The Coulomb counting operation requires the MCU to track the charge added/subtracted from the battery pack over time. L9961 helps tracking the charge variation ΔQ in the battery pack by continuously acquiring and accumulating the current. This significantly reduces the MCU reading rate, simplifying user SW.

Coulomb counting routine may refer to a known previous charge $Q(t_0)$ and apply the following equation:

Coulomb counting algorithm

$$\begin{cases} Q(t_k) = Q_{t0} + \Delta Q = Q_{t0} + \Delta T \Sigma_{k=1}^{K} I_{CELL}(k) = Q_{t0} + \frac{T_{CUR_FILTER}}{R_{SHUNT}} \Sigma_{k=1}^{K} V_{\mathrm{DIFF}}(k) \\ \Sigma_{k=1}^{K} V_{\mathrm{DIFF}}(k) = CC_ACC * V_{CUR_RES} \end{cases} \quad (6)$$

Where:

- V_{DIFF} = ISENSEP-ISENSEM
- CC_ACC is the accumulator, encoded in 2's complement
- R_{SHUNT} is the external shunt resistor mounted between ISENSEP and ISENSEM

Then, the $Q(t_k)$ just evaluated becomes the $Q(t_0)$ for the next iteration.

The CC_SAT read-only flag reports the status of the accumulator and sample counter: if one of the two accumulators of the two saturates, the CC_SAT is set to '1' and a RDY pulse is generated to inform MCU that the registers. Meanwhile, the accumulation is stopped and CC_ACC and CC_SAMPLE_CNT are frozen.

3.5.2.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

VB according operating range of Table 4 *; T_J according operating range of* Table 7.

Table 19. Coulomb counter electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
N_{ACC}	Coulomb counter accumulator size	Design info	-	24	-	bit
N_{SAMPLE_CNT}	Coulomb counter sample counter size	Design info	-	8	-	bit

Prerelease product(s)

3.5.3 Overcurrent monitor

When the CSA is enabled, L9961 can protect the battery pack from overcurrent events in both charge and discharge directions. The absolute value of each current sample is compared to a programmable digital threshold CSA.

This diagnostic can be enabled via OVC_EN bit and covers the failures listed in Table 20.

To avoid false detections, overcurrent thresholds shall only be modified while OVC_EN = 0.

The recommended re-engagement strategy in case of persistent OVC failure detection is:

- *Poll the PERSIST_OVC_<x> flags for at least $5T_{CUR_FILTER}$ to check if fault is still present*
  - *If the flag can be cleared, fault has disappeared and FET can be re-engaged*
  - *Otherwise, re-engaging the FET is not recommended and SW should let L9961 blow the FUSE (if not masked)*

Table 20. Overcurrent diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Overcurrent in charge	If the ISENSEM – ISENSEP voltage raises above $V_{OVC_CHG_TH}$, the OVC_CHG fault is acknowledged.	The OVC_CHG flag is set	If the ISENSEM – ISENSEP voltage falls below V_{OVC_TH}, the OVC_CHG flag can be cleared by MCU	The Charge FET is restored to the status defined by the CHG_ON bit	CSA_EN masks measurement execution. When disabled, the OVC_CHG flag can always be cleared
		The charge FET is turned OFF		FAULTN line is released	OVC_EN masks diagnostic execution and all reactions. When disabled, the OVC_CHG flag can always be cleared
		FAULTN line is asserted			OVC_CHG_PRDRV_MSK masks reaction on CHG pin
					OVC_CHG_FAULTN_MSK masks reaction on FAULTN pin
Persistent charge current	If the CHG FET is OFF (either commanded by user or forced by diagnostics) and the ISENSEM – ISENSEP voltage raises above $V_{PERSIST_OVC_TH}$, for 4 consecutive samples, the PERSIST_OVC_CHG fault is acknowledged.	The PERSIST_OVC_CHG flag is set	If the ISENSEM – ISENSEP voltage falls below $V_{PERSIST_OVC_TH}$ for 4 consecutive samples, the PERSIST_OVC_CHG flag can be cleared by MCU	FUSE pre-driver is disabled	CSA_EN masks measurement execution. When disabled, the PERSIST_OVC_CHG flag can always be cleared
		FUSE pre-driver is enabled	If CHG FET is ON and OVC_EN is ENABLE, the PERSIST_OVC_CHG counter is reset to 0	FAULTN line is released	OVC_EN masks diagnostic execution and all reactions. When disabled, the PERSIST_OVC_CHG flag can always be cleared
		FAULTN line is asserted			PERSIST_OVC_CHG_FUSE_MSK masks reaction on FUSE pin
					PERSIST_OVC_CHG_FAULTN_MSK masks reaction on FAULTN pin

Prerelease product(s)

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Overcurrent in discharge	If the ISENSEP – ISENSEM voltage raises above $V_{OVC_DCHG_TH}$, the OVC_DCHG fault is acknowledged.	The OVC_DCHG flag is set	If the ISENSEP – ISENSEM voltage falls below V_{OVC_TH}, the OVC_DCHG flag can be cleared by MCU	The Discharge FET is restored to the status defined by the DCHG_ON bit	CSA_EN masks measurement execution. When disabled, the DOVC_CHG flag can always be cleared
		The discharge FET is turned OFF		FAULTN line is released	OVC_EN masks diagnostic execution. When disabled, the OVC_DCHG flag can always be cleared
		FAULTN line is asserted			OVC_DCHG_PRDRV_MSK masks reaction on DCHG pin
					OVC_DCHG_FAULTN_MSK masks reaction on FAULTN pin
Persistent discharge current	If the DCHG FET is OFF (either commanded by user or forced by diagnostics) and the ISENSEP – ISENSEM voltage raises above $V_{PERSIST_OVC_TH}$, for 4 consecutive samples, the PERSIST_OVC_DCHG fault is acknowledged.	The PERSIST_OVC_DCHG flag is set	If the ISENSEP – ISENSEM voltage falls below $V_{PERSIST_OVC_TH}$ for 4 consecutive samples, the PERSIST_OVC_DCHG flag can be cleared by MCU	FUSE pre-driver is disabled	CSA_EN masks measurement execution. When disabled, the PERSIST_OVC_DCHG flag can always be cleared
		FUSE pre-driver is enabled	If DCHG FET is ON and OVC_EN is ENABLE, the PERSIST_OVC_DCHG counter is reset to 0	FAULTN line is released	OVC_EN masks diagnostic execution. When disabled, the PERSIST_OVC_DCHG flag can always be cleared
		FAULTN line is asserted			PERSIST_OVC_DCHG_FUSE_MSK masks reaction on FUSE pin
					PERSIST_OVC_DCHG_FAULTN_MSK masks reaction on FAULTN pin

3.5.3.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4*; T_J according operating range of* Table 7.

Table 21. Overcurrent electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OVC_CHG_TH}$	Programmable overcurrent in charge threshold (8 bit) $V_{OVC_{CHG_{TH}}} = -128V_{CUR_RES}{}^{*CODE}$	Tested by SCAN	$-V_{CUR_RES}(2^{NBIT_CSA-1} - 128)$	-	0	mV
$V_{OVC_DCHG_TH}$	Programmable overcurrent in discharge threshold (8 bit)	Tested by SCAN	0	-	$V_{CUR_RES}(2^{NBIT_CSA-1} - 128)$	mV

Prerelease product(s)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	$V_{OVC_{DCHG_{TH}}} = 128V_{CUR_RES}{}^{*CODE}$					
$V_{PERSIST_OVC_TH}$	Programmable persistent overcurrent threshold (8 bit). Check is performed on the current absolute value. $\lvert V_{PERSIST_{OV_{TH}}} \rvert = V_{CUR_RES}{}^{*CODE}$	Tested by SCAN	0	-	$255*V_{CUR_RES}$	mV

Note: Note: accuracy of the thresholds depends on the accuracy of the CSA. Refer to Table 20.

3.5.4 Short-circuit in discharge protection

When the CSA is enabled, L9961 protects the battery pack from short-circuit in discharge by sensing the current through the shunt resistor with a faster filter time T_{SC_FILTER}, programmable in the SC_FILTER field. This diagnostic is enabled using SC_EN bit and covers the failures listed in Table 22.

Writing SC_EN = 1 enables the short-circuit monitor after a maximum delay of 528 µs. To avoid false detections, overcurrent thresholds shall only be modified while SC_EN = 0

Table 22. Short-circuit in discharge diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Short-circuit in discharge	If the (ISENSEP – ISENSEM) voltage raises above V_{SC_TH} for longer than T_{SC_FILTER}, the SC fault is acknowledged.	The SC_DCHG flag is set	If the If the (ISENSEP – ISENSEM) voltage falls below V_{SC_TH} for longer than T_{SC_FILTER}, the SC_DCHG flag can be cleared by MCU	The Discharge FET is restored to the status defined by the DCHG_ON bit	CSA_EN masks measurement execution. When disabled, the SC_DCHG flag can always be cleared
		The Discharge FET is turned OFF		FAULTN line is released	SC_EN masks diagnostic execution. When disabled, the SC_DCHG flag can always be cleared
		FAULTN line is asserted			SC_DCHG_PRDRV_MSK masks reaction on DCHG pin
					SC_DCHG_FAULTN_MSK masks reaction on FAULTN pin
Persistent short-circuit in discharge	If the DCHG FET is OFF (either commanded by user or forced by diagnostics) and the ISENSEP – ISENSEM voltage raises above $V_{PERSIST_SC_TH}$, the PERSIST_SC_DCHG fault is acknowledged. Diagnostic is masked for $T_{PERSIST_SC_BLANK}$ starting from DCHG FET OFF event.	The PERSIST_SC_DCHG flag is set	If the If the (ISENSEP – ISENSEM) voltage falls below $V_{PERSIST_SC_TH}$ for longer than T_{SC_FILTER}, the PERSIST_SC_DCHG flag can be cleared by MCU	FUSE pre-driver is disabled	CSA_EN masks measurement execution. When disabled, the PERSIST_SC_DCHG flag can always be cleared
		FUSE pre-driver is enabled		FAULTN line is released	SC_EN masks diagnostic execution. When disabled, the PERSIST_SC_DCHG flag can always be cleared
		FAULTN line is asserted			PERSIST_SC_DCHG_FUSE_MSK masks reaction on FUSE pin

Prerelease product(s)

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Persistent short-circuit in discharge	If the DCHG FET is OFF (either commanded by user or forced by diagnostics) and the ISENSEP – ISENSEM voltage raises above $V_{PERSIST_SC_TH}$, the PERSIST_SC_DCHG fault is acknowledged. Diagnostic is masked for $T_{PERSIST_SC_BLANK}$ starting from DCHG FET OFF event.	FAULTN line is asserted	If the If the (ISENSEP – ISENSEM) voltage falls below $V_{PERSIST_SC_TH}$ for longer than T_{SC_FILTER}, the PERSIST_SC_DCHG flag can be cleared by MCU	FAULTN line is released	PERSIST_SC_DCHG_FAULTN_MSK masks reaction on FAULTN pin

3.5.4.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4*; T_J according operating range of* Table 7.

Table 23. Short-circuit in discharge electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SC_RES}	Short-circuit measurement resolution	Design info		2.34 (300 mV/2^7)		mV
T_{SC_FILTER}	Programmable short-circuit in discharge filter time (3 bit) $T_{SC_{FILTER}} = 32us*2^{CODE}$	Tested by SCAN	32		512	µs
V_{SC_TH}	Programmable short-circuit in discharge threshold (4 bit) $V_{SC_{TH}} = 49.14mV + 14.04mV*CODE$		50		275	mV
$V_{PERSIST_SC_TH}$	Programmable persistent short-circuit in discharge threshold (4 bit) $V_{SC_{PERSISTTH}} = 49.14mV + 14.04mV*CODE$		50		275	mV
$V_{SC_TH_TOL}$	V_{SC_TH} gain error		-10		+10	%
$V_{SC_TH_OFFSET}$	V_{SC_TH} offset error		-5		+5	mV
$T_{PERSIST_SC_BLANK}$	Persistent short-circuit in discharge blanking time		224		256	µs

3.6 Cell balancing

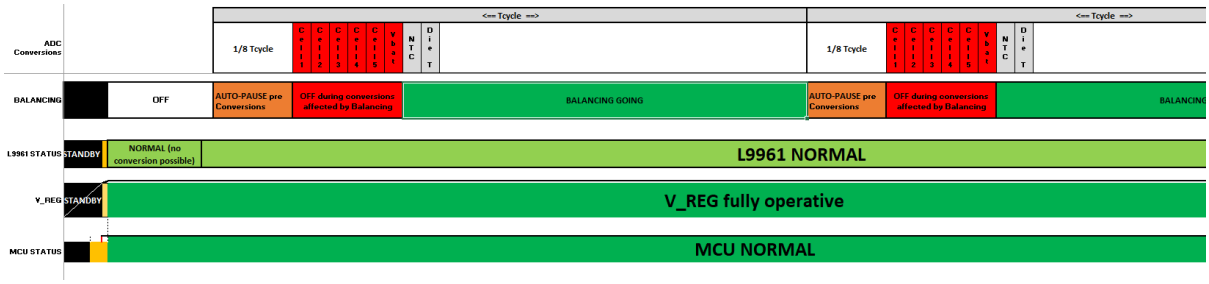
L9961 provides passive cell balancing by discharging battery cells through the Cx pins. To activate the balancing switch on a cell, the corresponding BAL<x>_ON bit must be set. Balancing is inhibited if cell voltage falls below the balance undervoltage threshold (refer to Section 3.4.1 Cell voltage monitor (Cx)).

Balancing current must be limited to a maximum of I_{BAL_MAX} via cell filtering resistors. It is recommended balancing only non-adjacent cells. Care must be taken if balancing adjacent cells in order not to violate the I_{BAL_MAX} constraint.

To allow cell voltage relaxation, balancing is stopped $T_{BAL_SETTLING}$ before running the first step of the Section 3.4 Voltage conversion routine. It is then automatically re-engaged after the VB step completion.

Prerelease product(s)

Figure 9. **Balancing timing diagram**



GADG220620221343SA

3.6.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4*; T_J according operating range of* Table 7.

Table 24. **Balancing electrical parameters**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
R_{DS_ON}	Balancing FET ON resistance	I_{OUT}=70 mA			20	Ω	Cx
I_{BAL_MAX}	Maximum balancing current	For each balancing FET			70	mA	Cx
T_{ON_BAL}	Cell balance driver turn on time	RCx=39 Ω, external Cap 470 nF From BAL<x>_ON command to 30% of VDS	1	5	12	µs	Cx
T_{OFF_BAL}	Cell balance driver turn off time	RCx=39 Ω, external Cap 470nF From BAL<x>_OFF command to 70% of VDS	3	9	20	µs	Cx
$T_{BAL_SETTLING}$	Settling time before cell measurement	Tested by SCAN		TMEAS_CYCLE/8		ms	Cx

3.7 HS/LS pre-drivers (CHG/DCHG/FUSE)

L9961 integrates three pre-driver stages aimed at managing pack connection to external loads and chargers.

3.7.1 Battery pack charge/discharge relays (CHG/DCHG)

L9961 uses a dual pre-driver stage to manage the external charge (CHG) and discharge (DCHG) switches. The pre-driver stage can be configured as high side or low side by programming the CHG_HS_LS and DCHG_HS_LS field.

The gate driver outputs are enabled in NORMAL mode only, and are in HiZ while in STANDBY or SHIPMENT - DEEP SLEEP states.

When in NORMAL state, the CHG an DCHG FETs can be commanded ON/OFF using I2C registers:

- DCHG_ON commands the DCHG FET
- CHG_ON commands the CHG FE

Several diagnostics may have an impact on CHG/DCHG output state, which can be forced low by L9961 independently of the status of the above commands.

3.7.1.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4*; T_J according operating range of* Table 7.

Prerelease product(s)

Prerelease product(s)

Table 25. CHG/DCHG pre-driver electrical parameter

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
F_{PRDRV}	Pre-driver expected switching frequency	Application info		2		Hz	DCHG, VSD, VSC, CHG
C_{PRDRV_LOAD}	Equivalent capacitive load on CHG/DCGH pins	Application info		10		nF	DCHG, VSD, VSC, CHG
V_{GS_ON1}	CHG/DCHG ON voltage	VB > 5.0 V	7.2	10.5	11.7	V	DCHG, VSD, VSC, CHG
V_{GS_ON2}	CHG/DCHG ON voltage	4.3V < VB < 5.0 V	6.0			V	DCHG, VSD, VSC, CHG
V_{GS_OFF}	CHG/DCHG OFF voltage	I(CHG) = I(DCHG) = 0.450 mA V(VSx)=0 V			100	mV	DCHG, VSD, VSC, CHG
I_{PU}	CHG/DCHG current source	V(CHG)-V(VSC)=0 V V(DCHG)-V(VSD)=0 V V(VSx)=0 V	-2.4		-0.6	mA	DCHG, VSD, VSC, CHG
I_{PD}	CHG/DCHG current sink	V(CHG)-V(VSC)=1.4 V V(DCHG)-V(VSD)=1.4 V V(VSx)=0 V	12.5	39.2	85	mA	DCHG, VSD, VSC, CHG
I_{PD_PEAK}	CHG/DCHG current sink peak	Design info	9	18.5		mA	DCHG, VSD, VSC, CHG
R_{PD}	CHG/DCHG pulldown resistance	V(CHG)-V(VSC)=0.3 V V(DCHG)-V(VSD)=0.3 V V(VSx)=0 V			35	Ω	DCHG, VSD, VSC, CHG

3.7.2 FUSE pre-driver

Under certain conditions classified as permanent failures, L9961 can be programmed to activate the FUSE pre-driver. An external NMOS can be driven to blow up a fuse connected in series to the battery pack positive terminal.

The following list of failures is classified as permanent:

- Severe cell UV: aimed at preventing copper deposition (see Section 3.4.1 Cell voltage monitor (Cx))
- Severe cell OV: aimed at preventing explosion hazard (see Section 3.4.1 Cell voltage monitor (Cx))
- VB vs. Sum Of Cells plausibility check fail: aimed at preventing BMS permanent malfunction (see Section 3.4.2 Battery stack monitor (VB))
- Severe NTC OT: aimed at preventing fire hazard (see Section 3.4.3 Cell temperature monitor (NTC))
- Persistent charge current: aimed at preventing overcharge (see Section 3.5.3 Overcurrent monitor)
- Persistent discharge current: aimed at preventing overdischarge (see Section 3.5.3 Overcurrent monitor)
- Persistent short circuit in discharge: aimed at preventing fire hazard (see Section 3.5.4 Short-circuit in discharge protection)

In addition to the internal diagnostics, L9961 can also enable the FUSE predriver upon:

- User request through I2C

FUSE must start from the OFF condition (FUSE_TRIG_FIRE = 01)

FUSE shall be first armed writing FUSE_TRIG_ARM = 10

- 1. *The FUSE can be then fired setting FUSE_TRIG_FIRE = 10 within $T_{FUSE_TIMEOUT}$, otherwise the fire command will be discarded*

Note: Rewriting FUSE_TRIG_ARM = 10 while the timeout is running restarts the timer. Writing FUSE_TRIG_FIRE = 01 interrupts the FUSE activation. Writing FUSE_TRIG_ARM = 10 while FUSE_TRIG_FIRE = 10 immediately fires the FUSE.

- Secondary protector activation detection: if the FUSE voltage rises above V_{FUSE_TH} for longer than T_{FUSE_FILTER}, the FUSE pre-driver is enabled and the FUSE_EXT flag is set. Once triggered, the action can no longer be inhibited unless a GO2SHIP/GO2SLP command is issued.

3.7.2.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4; T_J according operating range of Table 7.

Table 26. Coulomb counter electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
I_{FUSE}	Fuse pre-driver pullup current	VFUSE = 0V	50			µA	FUSE
V_{FUSE_TH}	FUSE external activation detection threshold		0.8		1.8	V	FUSE
V_{FUSE_HYST}	FUSE external activation detection threshold hysteresis		0.1		0.5	V	FUSE
T_{FUSE_FILTER}	FUSE activation/deactivation digital filter	Tested by SCAN	85	104	120	µs	FUSE
$T_{FUSE_TIMEOUT}$	FUSE fire command timeout in respect to fuse arm event	Tested by SCAN	1.6	2	2.3	s	FUSE
R_{FUSE}	FUSE pull down resistance		60	100	150	kΩ	FUSE

Prerelease product(s)

3.8 Digital IOs (RDY/SDA/SCL/FAULTN_SAFE/FAULTN/OD)

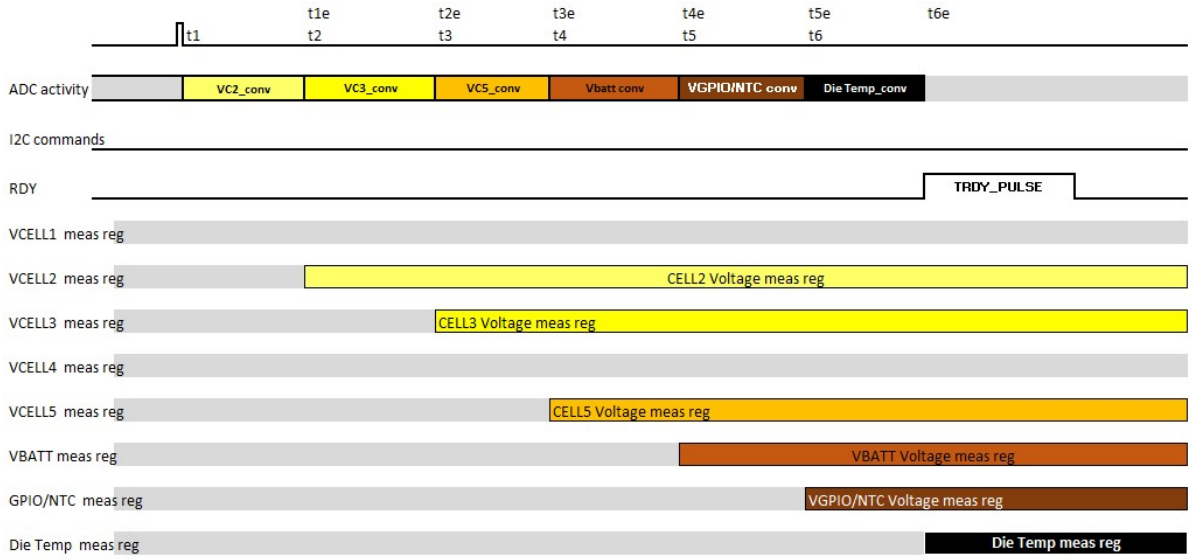
The following paragraph lists the electrical characteristics of the device digital IOs.

3.8.1 Data-ready interrupt pin (RDY)

The RDY pin is used to signal the system MCU when new data is available. The RDY signal is a positive pulse lasting T_{RDY_PULSE} upon the following events:

- After each Section 3.4 Voltage conversion routine task is completed (as shown in Figure 11. I2C clock polarity)
- If the Coulomb counter saturates (upon CC_SAT flag positive edge, see Section 3.5.2 Coulomb counting)
- Any time the device enters NORMAL state

Figure 10. RDY pulse generation upon voltage conversion routine task termination



GADG220620221329SA

3.8.1.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4; T_J according operating range of Table 7.

Table 27. RDY Interrupt pin electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
T_{RDY_PULSE}	RDY interruput pulse duration	Tested by SCAN	85	104	120	us	RDY

3.8.2 Fault interrupt pin (FAULTN)

The FAULTN pin indicates when a failure is detected . FAULTN is an open-drain output active low.

Several failures can be redirected to FAULTN line depending on their masking bit. Refer to Section 3.4 Voltage conversion routine and Section 3.5 Current conversion routine for a list of specific failures.

FAULTN can also be used by a secondary protector in order to disconnect the battery pack from the load or the charger. When not internally pulled low, FAULTN can be externally pulled low for T_{FAULTN_LOW}: L9961 will force the CHG/DCHG outputs low, regardless of CHG_ON and DCHG_ON commands and L9961 internal diagnostics. The event is latched by FAULTN_EXT bit. CHG/DCHG will be released upon flag clear by MCU.

Prerelease product(s)

3.8.2.1 *Electrical parameters*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4; T_J according operating range of Table 7.

Table 28. Digital output electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
T_{FAULTN_LOW}	FAULTN input filter time for secondary protector activation detection	Tested by SCAN	17	21	25	µs	FAULTN

Prerelease product(s)

3.8.3 MCU emergency reset (FAULTN_SAFE)

MCU should normally manage the communication with battery charger, ensuring cells are properly charged to 100% state of charge. In case MCU operation fails, the battery cells could be overcharged, leading to fire/ explosion hazard.

L9961 can reset the MCU should a cell overvoltage condition be detected. This is done connecting the FAULTN_SAFE open-drain output to the MCU reset pin (active low).

When overvoltage failures are directed to FAULTN_SAFE pin, the output is pulled low for $T_{FAULTN_SAFE_LOW}$ to allow proper reset of the MCU.

3.8.3.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

VB according operating range of Table 4; T_J according operating range of Table 7.

Table 29. Digital output electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
$T_{FAULTN_SAFE_LOW}$	FAULTN_SAFE low interval	Tested by SCAN	85	104	120	µs	FAULTN_SAFE

3.8.4 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

VB according operating range of Table 4; T_J according operating range of Table 7.

Table 30. Digital output electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin
V_{IN_L}	Low input level Valid for FAULTN, SDA, SCL	Slow rising ramp on input pin	0.8	-	1.8	V	SCL, FAULTN
V_{IN_HYS}	Input hysteresis Valid for FAULTN, SDA, SCL	Input considered high when VIN > VIN_L + VIN_HYS	0.1	-	0.5	V	SCL, FAULTN
V_{OUT_L}	Low output level	IOUT = 2 mA	0	-	0.4	V	RDY
V_{OUT_H}	High output level	IOUT = 2 mA	VREG-0.4	-	VREG	V	RDY
T_{OUT_RISE}	Output rise time Valid for RDY	Cload=120 pF From 20 to 80% of final value	5	-	35	ns	RDY
T_{OUT_FALL}	Output fall time Valid for RDY.	Cload=120 pF From 80 to 20% of initial value	5	-	35	ns	RDY
V_{OPEN_DRAIN}	Open-drain equivalent ON resistance measurement Valid for SDA, FAULTN, FAULTN_SAFE, OD	I_{OD}=2 mA	0.02	-	0.15	V	SDA, FAULTN, OD, FAULTN_SAFE

3.9 I2C communication interface

L9961 uses an I2C slave peripheral interface to communicate with a host MCU on an addressed I2C bus.

The I2C peripheral uses two lines to implement communication:

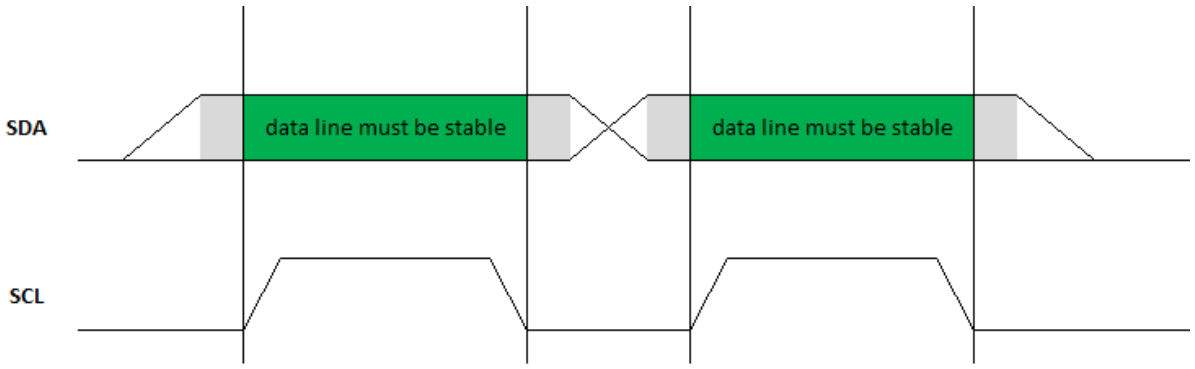
- SCL (Serial CLock): a digital input receiving clock from the master unit of the I2C bus.
- SDA (Serial DAta): a digital input/output used for sending and receiving data clocked by the master unit of the I2C bus

L9961 I2C peripheral is compliant to the I2C fast standard (400 kbit/s).

Prerelease product(s)

3.9.1 Clock polarity

Figure 11. **I2C clock polarity**

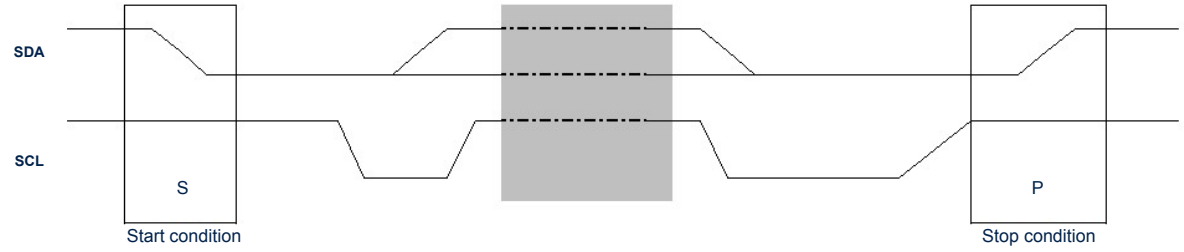


GADG220620221330SA

Data on SDA line is sampled upon SCL rising edge and it must fulfill t_{SU_DAT} (setup) and t_{HD_DAT} (hold) constraints. While it is allowed to change during SCL low semi-period. A single bit is transferred per each clock period.

3.9.2 START/STOP conditions

Figure 12. **I2C START/STOP conditions**



GADG220620221332SA

Every communication window is defined within START and STOP conditions. These are always generated by the master

- A START condition corresponds to a SDA HI→LO transition while SCL is HIGH. The SCL must verify the t_{SU_STA} (setup) and t_{HD_STA} (hold) constraints
  - When a START condition is detected an internal watchdog timer is reset and started
- A STOP condition corresponds to a SDA LO→HI transition while SCL is HIGH. The SCL must verify the t_{SU_STO} (setup) and t_{HD_STO} (hold) constraints
  - If the communication break or any issue occur while a I2C frame is ongoing, the IC will be able to re-engage after TI2C_TIMEOUT time.

After the STOP condition, the bus must be left idle for at least t_{BUF} before issuing a new START condition. L9961 resets its I2C logic upon each START/STOP condition detection.

Prerelease product(s)

3.9.3 ACK/NACK

In a communication window, every byte transferred over the I2C bus is followed by a 9th bit representing the acknowledge (ACK) or not acknowledge (NACK) condition. For each byte, the peripheral receiving data will either confirm its availability to continue the communication (ACK) or will signal unavailable (NACK).

- An ACK is represented by SDA LOW on the 9th SCL pulse
- A NACK is represented by SDA HIGH on the 9th SCL pulse

The following conditions lead to the generation of a NACK by a receiver:

1. *Absence of receiver*: no receiver is present on the bus with the transmitted address so there is no device to respond with an ACK
2. *Receiver busy*: the receiver is unable to receive or transmit because it is performing a real-time function and is not ready to start communication with the master
3. *Wrong data received*: during the transfer, the receiver gets data or commands that it does not understand. If the CRC check is enabled, L9961 will generate a NACK in case corrupted data is detected.
4. *Receiver buffer full*: during the transfer, the receiver cannot receive more data.
5. *Transfer completed*: a master-receiver must signal the end of the transfer to the slave transmitter.

When L9961 generates a NACK, the error state is latched and any subsequent write operation will not be accomplished. The MCU is expected to issue a STOP condition to reset the I2C logic.

3.10 I2C protocol layer

3.10.1 Addressing and R/ $\overline{W}$ bit

The ADDRESS byte is formed by a 7 bit address field plus a R/ $\overline{W}$ bit:

- By default, the ADDRESS is 0b1001001
  - The address can be changed programming the DEV_ADDR_ID register
  - The address can be stored in the NVM in order to allow the integration of L9961 on a multichip bus
- The R/ $\overline{W}$ bit is processed as follows
  - R/ $\overline{W}$ = 1 means READ
  - R/ $\overline{W}$ = 0 means WRITE

3.10.2 CRC

L9961 can check data integrity by means of a CRC. By default, this feature is disabled and can be enabled by programming the CRC_EN bit.

The CRC poly is: x^8+x^2+x+1

The CRC initialization is 0.

L9961 exploits received CRC information to validate each WRITE operation, eventually issuing a NACK and discarding data in case of corruption detection.

In READ operations, L9961 equips the output data with CRC to allow MCU validating the received data. The MCU may:

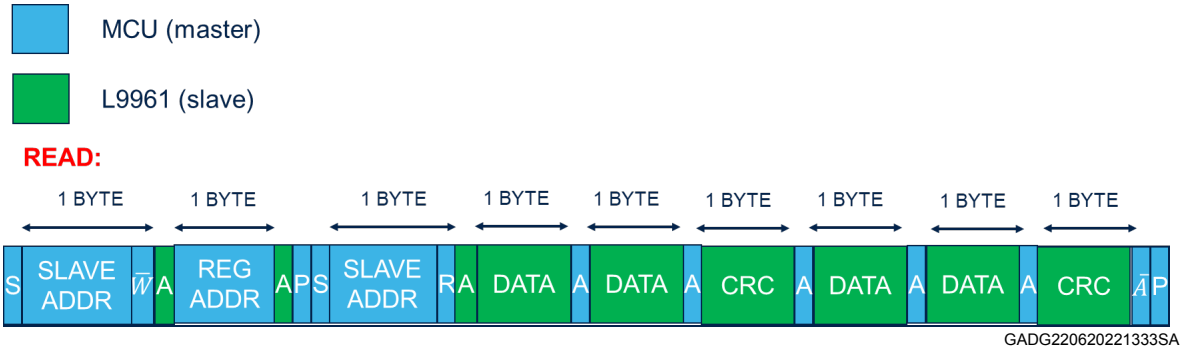
- validate data on-the-fly, generating a real-time NACK in case of corruption detection
- validate the data offline, discarding it in case of corruption detection

Prerelease product(s)

3.10.3 Single read/block read

The READ operation shall be used to retrieve information from the internal I2C registers. However, as the device implements a clear on write approach, it will not clear any latch.

Figure 13. I2C generic READ operation



The elementary READ operation consists of:

1. A START condition
2. The SLAVE ADDRESS byte (with R/ $\overline{W}$ = 0) identifying the slave device to be activated
3. The REGISTER ADDRESS byte identifying the memory address where data has to be read
4. A STOP condition

This first instruction subset loads the starting address into the memory address counter. Then the following sequence starts the download of the data:

1. A START condition
2. The SLAVE ADDRESS byte (with R/ $\overline{W}$ = 1) identifying the slave device to be activated
3. L9961 will output two data bytes
4. L9961 will output an optional CRC byte covering all the previous bytes

In a block read, MCU can continue reading by clocking additional packets of two data bytes (plust a third CRC byte optionally generated by L9961). The REGISTER ADDRESS defined at step 3 will be considered as the starting address, and the memory address counter will be incremented by 1 at every 2 bytes output.

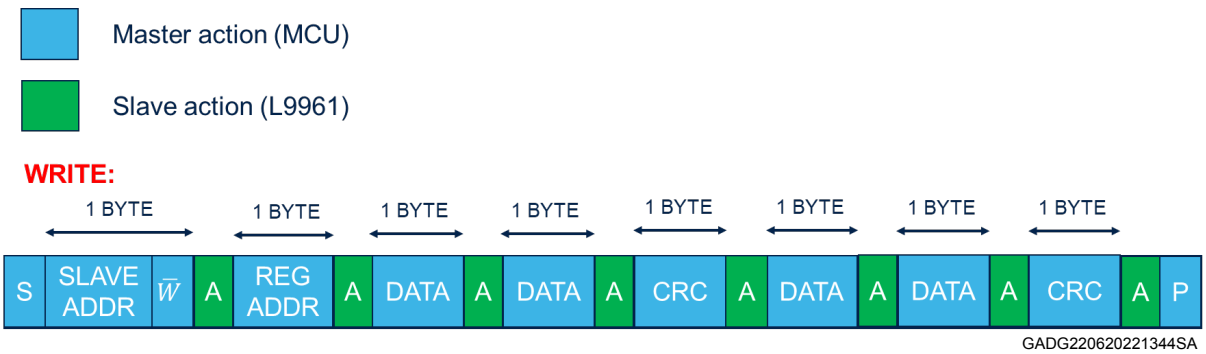
In case REGISTER ADDRESS saturates, L9961 will output 0xFF bytes.

The READ operation terminates with a STOP condition.

3.10.4 Single WRITE/block WRITE

The WRITE operation shall be used for configuring device parameters and sending actuation commands. As the I2C peripheral implements a clear on write approach, the WRITE operation must also be used to reset any latch writing a logic ‘1’ to the corresponding bit.

Figure 14. I2C generic WRITE operation



Prerelease product(s)

The elementary WRITE operation consists of:

1. A START condition
2. The SLAVE ADDRESS byte (with R/ $\overline{W}$ = 0) identifying the slave device to be activated
3. The REGISTER ADDRESS byte identifying the memory address where data has to be written
4. Two data bytes
5. An optional CRC byte covering all the previous bytes.

In a block write, the operation can continue by sending other packets formed by two data bytes and an optional CRC covering the previous two bytes. The REGISTER ADDRESS defined at step 3 will be considered as the starting address, and the memory address counter will be incremented by 1 at every 2 bytes received.

In case REGISTER ADDRESS saturates, L9961 will generate a NACK and data will not be written into internal regs.

In case the received CRC is wrong, L9961 generates a NACK and the corresponding data is not written into internal registers.

The WRITE operation terminates with a STOP condition.

3.10.5 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

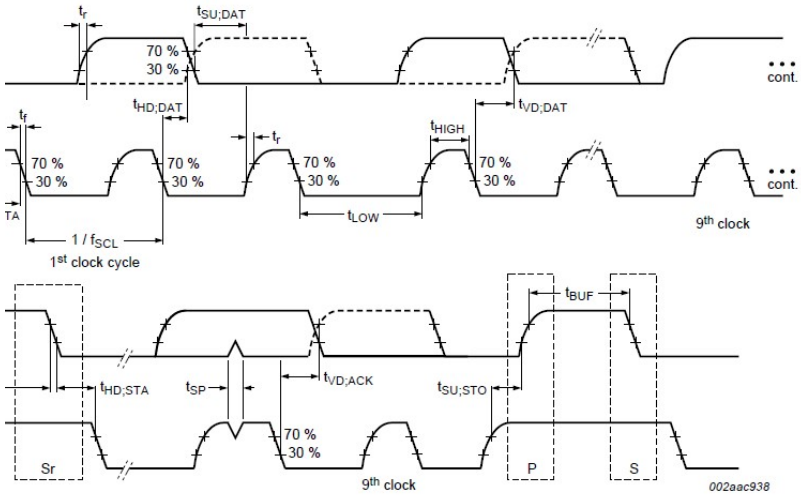
VB according operating range of Table 4*;* T_J *according operating range of* Table 7.

Table 31. I2C electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{SCL}	Communication frequency	Guaranteed by design	80		400	kHz
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{HD_STA}	SCL hold (high) time, after SDA falling edge has created the START condition, for the START condition to be correctly detected		0.6			µs
t_{SU_STA}	SCL set-up time to high (SDA already high) before SDA falling edge creates the START condition sequence (by falling when SCL is steadily high)		0.6			µs
t_{HD_DAT}	SDA hold time after SCL falling edge		300		-	ns
t_{SU_DAT}	SDA set-up time before SCL rising edge		100		-	ns
t_r	Rise time of SDA signal	With 4.7 kΩ pullup resistor and 40 pF load	0		300	ns
t_f	Fall time of SDA signal	With 4.7 kΩ pullup resistor and 40 pF load	0		300	ns
t_{rf_SCL}	Rise/fall time SCL signal		0		300	ns
t_{SU_STO}	SCL set-up time to high (SDA already low) before SDA rising edge creates the STOP condition sequence (by rising when SCL is steadily high)		0.6			µs
t_{HD_STO}	SCL hold (high) time, after SDA rising edge has created the STOP condition, for the STOP condition to be correctly detected		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
C_b	Capacitive load for each bus line				400	pF
$t_{VD_DAT_ACK}$	Data (ACK) valid time				0.9	µs
$T_{I2C_TIMEOUT}$			46	50	54	ms

Prerelease product(s)

Figure 15. **Timing on the I2C bus**



GADG220620221346SA

3.11 Non-volatile memory (NVM)

L9961 allows saving key I2C configuration parameters in the internal NVM. Not all I2C register are stored in the NVM: refer to the register map file attached, where a color code identifies configuration registers stored in the NVM.

The following I2C commands allow interacting with the NVM:

- NVM_WRITE_READ_CODE_CMD = 0xAAAA triggers the NVM upload fetching the data from I2C registers and moving it to the NVM sectors. The operation lasts T_{NVM_UPLOAD} and during such an interval the MCU will not be able to perform I2C R/W operations
- NVM_WRITE_READ_CODE_CMD = 0x5555 triggers the NVM download fetching the data from NVM sectors and moving it to the I2C registers. The operation lasts $T_{NVM_DOWNLOAD}$ and during such an interval the MCU will not be able to perform I2C R/W operations.

The NVM can be written a maximum of $N_{NVM_WRITE_CYCLES}$. If such a limit is exceeded, data retention is not guaranteed. The NVM_UPLOADS_COUNT counter stores the number of NVM write operation executed and is saturated to 31.

At each device wakeup the NVM is autonomously re-downloaded and the related I2C configuration registers are refreshed. Thus, MCU is not required to run configuration functions at each wakeup.

MCU shall disable any load actuation (CHG/DCHG, balancing and FUSE) before launching an NVM download/ upload command.

Data stored in the NVM is checked against corruption:

- If the trimming and calibration data is corrupted, the CRC_TRIM_CAL_FAIL flag is set and the FAULTN pin is asserted
- If the user sectors are corrupted, the CRC_CFG_FAIL flag is set and the FAULTN pin is asserted

Whenever data corruption is detected (CRC_TRIM_CAL_FAIL or CRC_CFG_FAIL), the diagnostic routines will not be stopped and faults might be inadvertently flagged. However, all the actuations due to internal faults will be inhibited as if the corresponding masking bit (*_MSK) was set.

A corrupted NVM sector will be downloaded as 0x0.

Prerelease product(s)

3.11.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according operating range of Table 4; T_J according operating range of Table 7.

Table 32. NVM electrical parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$N_{NVM_WRITE_CYCLES}$	NVM allowed write cycles	Guaranteed by design	-	-	16	cycles
T_{NVM_UPLOAD}	NVM upload time	Guaranteed by design	-	-	65	ms
$T_{NVM_DOWNLOAD}$	NVM download time	Guaranteed by design	-	-	5	ms

Prerelease product(s)

4 Device register map

L9961 register map is available in the *“L9961_I2C_Register_Map.xlsx*“ embedded in this document.

Registers are classified according to the following syntax:

- RO = Read Only
- RW = Read/Write
- WO = Write Only
- RLW = Clear On Write

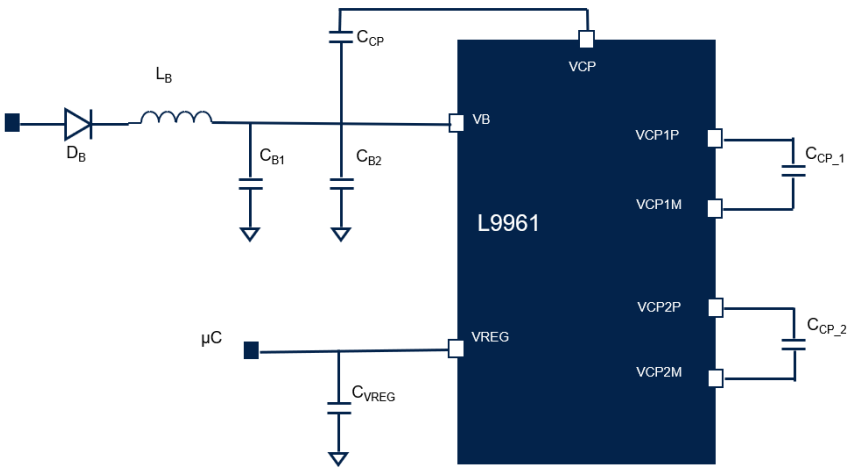
Default values of configuration registers written in the NVM correspond to the default ST factory settings. If these values are rewritten by user FW and pushed into the NVM, the default value at each powerup will correspond to the user settings.

Prerelease product(s)

5 Application information

5.1 Power supply circuit

Figure 16. **Power supply circuit**



GADG220620221348SA

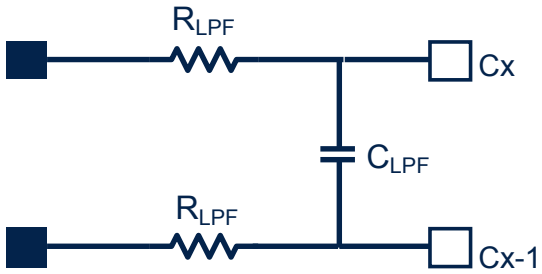
Table 33. **Recommended power supply components**

Components	Value	Unit	Max. tolerance	Rating	Comments
L_B	1	µH	20%	100 mA	LPF inductance for battery path. The filter cut-off frequency is $f_C = \frac{1}{2\pi\sqrt{L_B(C_{B1}+C_{B2})}}$
C_{B1}	10	µF	10%	50 V	Provide battery stabilization. Filter noise on VB sense line.
C_{B2}	220	nF	10%	50 V	Filter high frequency noise on VB sense line. Place as close as possible to VB pin.
C_{CP}	68	nF	10%	25 V	Charge pump tank capacitor. Mount as close as possible to VCP pin.
C_{CP_1}	6.8	nF	10%	50 V	Charge pump flying capacitor. Mount as close as possible to VCP1P/1M pin.
C_{CP_2}	6.8	nF	10%	50 V	Charge pump flying capacitor. Mount as close as possible to VCP2P/2M pin.
C_{VREG}	4.7	µF	10%	16 V	Tank for the VREG regulator. Mount as close as possible to VREG pin. Part number C0805C475K4RACAUTO
D_B	40	V			The BAT54SWFILMY is recommended for protecting VB against reverse battery

Prerelease product(s)

5.2 Cell voltage sensing and balancing circuit

Figure 17. **Cell voltage sensing and balancing circuit**



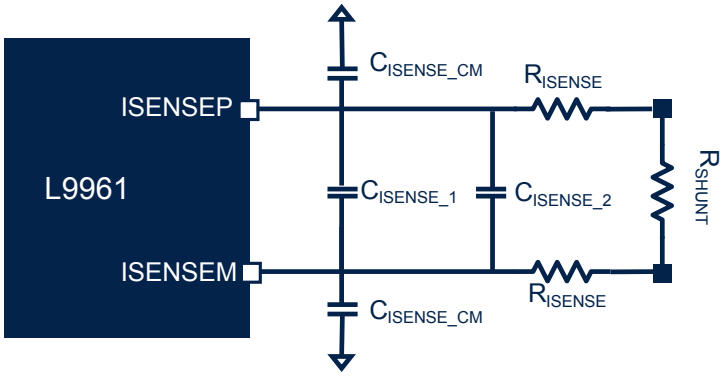
GADG220620221356SA

Table 34. **Typical BOM for cell voltage sensing and balancing circuit**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{LPF}	39	Ω	10%	1/8 W	LPF resistor for cell voltage measurement. It is used also to limit the balancing current. The differential filter cut-off frequency is $f_C = \frac{1}{4\pi R_{LPF} C_{LPF}}$
C_{LPF}	470	nF	10%	16 V	LPF capacitor for cell voltage measurement. The differential filter cut-off frequency is $f_C = \frac{1}{4\pi R_{LPF} C_{LPF}}$

5.3 Current sense circuit

Figure 18. **Current sense circuit**



GADG220620221357SA

Table 35. **Typical current sense BOM**

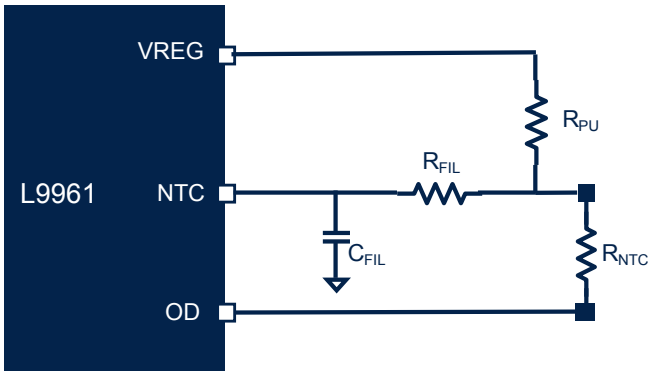
Components	Value	Unit	Max. tolerance	Rating	Comments
R_{SHUNT}	9	mΩ	1%	3 W	Shunt resistor used for current sensing and coulomb counting. Rating depends on the maximum battery current (R_{SHUNT} * $I_{SENSE_MAX}^2$). Different R_{SHUNT} values are possible as long as R_{SHUNT} * I_{SENSE} stays in the differential measurement range [-200; +200] mV and the ISENSEp/ ISENSEm AMR are not violated

Prerelease product(s)

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{ISENSE}	22	Ω	1%	1/10 W	It is used both filter differential and common mode noise on the ISENSEp/ISENSEm input. The differential filter cut-off frequency is $f_C = \frac{1}{4\pi R_{ISENSE}\left(C_{ISENSE_1} + C_{ISENSE_2} + \frac{C_{ISENSE_CM}}{2}\right)}$. The common mode filter cut-off frequency is $f_C = \frac{1}{2\pi R_{ISENSE} C_{ISENSE_CM}}$
C_{ISENSE_CM}	4.7	µF	10%	16 V	Filter common mode noise. The common mode filter cut-off frequency is $f_C = \frac{1}{2\pi R_{ISENSE} C_{ISENSE_CM}}$
C_{ISENSE_1}	4.7	µF	10%	16 V	Filter differencial low frequency noise on the ISENSEp/ISENSEm input. The differential filter cut-off frequency is $f_C = \frac{1}{4\pi R_{ISENSE}\left(C_{ISENSE_1} + C_{ISENSE_2} + \frac{C_{ISENSE_CM}}{2}\right)}$
C_{ISENSE_2}	22	nF	10%	16 V	Filter differencial high frequency noise on the ISENSEp/ISENSEm input. The differential filter cut-off frequency is $f_C = \frac{1}{4\pi R_{ISENSE}\left(C_{ISENSE_1} + C_{ISENSE_2} + \frac{C_{ISENSE_CM}}{2}\right)}$.

5.4 NTC analog front end

Figure 19. NTC measurement circuit



GADG220620221358SA

Table 36. NTC analog front end BOM

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{NTC}	33	kΩ	10%	1/10 W	NTC resistor
R_{PU}	33	kΩ	10%	1/10 W	Provide VREG/2 polarization for NTC typical value
R_{FIL}	10	kΩ	10%	1/10 W	Filter the NTC signal: cut-off frequency is $f_C = \frac{1}{2\pi R_{FIL} C_{FIL}}$
C_{FIL}	10	nF	10%	16 V	Filter the NTC signal: cut-off frequency is $f_C = \frac{1}{2\pi R_{FIL} C_{FIL}}$

Prerelease product(s)

5.5 HS/LS pre-drivers circuit

Figure 20. **HS/LS pre-drivers circuit**

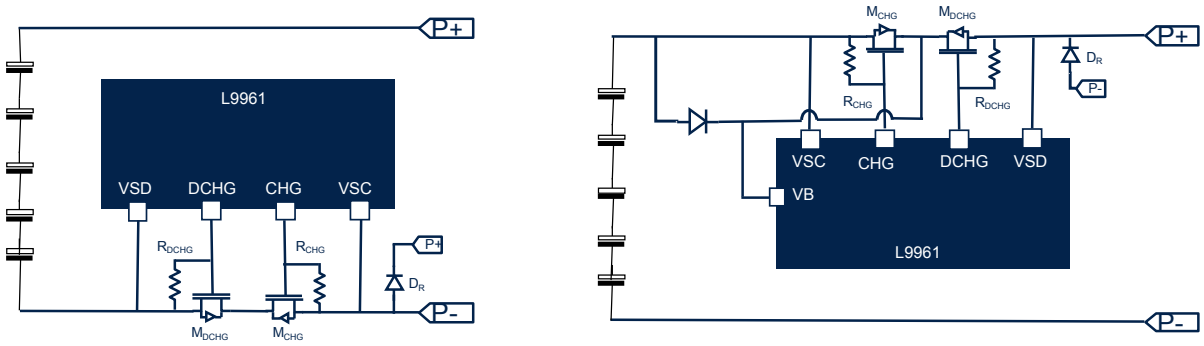
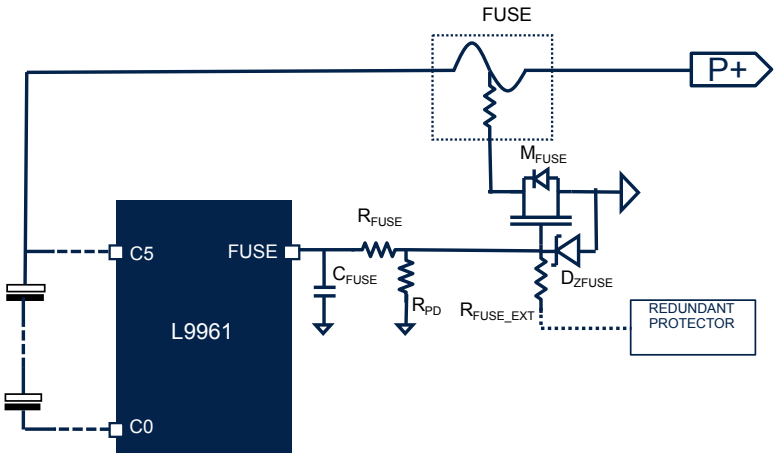


Table 37. **Typical HS/LS Pre-Drivers BOM**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{CHG}	2	MΩ	10%	1/10 W	Pull-down resistor
R_{DCHG}	2	MΩ	10%	1/10 W	Pull-down resistor
M_{CHG}				40 V	Battery charge FET. The STL210N4F7 is suggested
M_{DCHG}				40 V	Battery discharge FET. The STL210N4F7 is suggested
D_R	40	V			Recirculation diode. It is intended to protect VSD/VSC pin by recirculating the energy stored in the parasitic inductance of wires in case of the discharge phase is sudden interrupted.

5.6 Fuse circuit

Figure 21. **Fuse circuit**



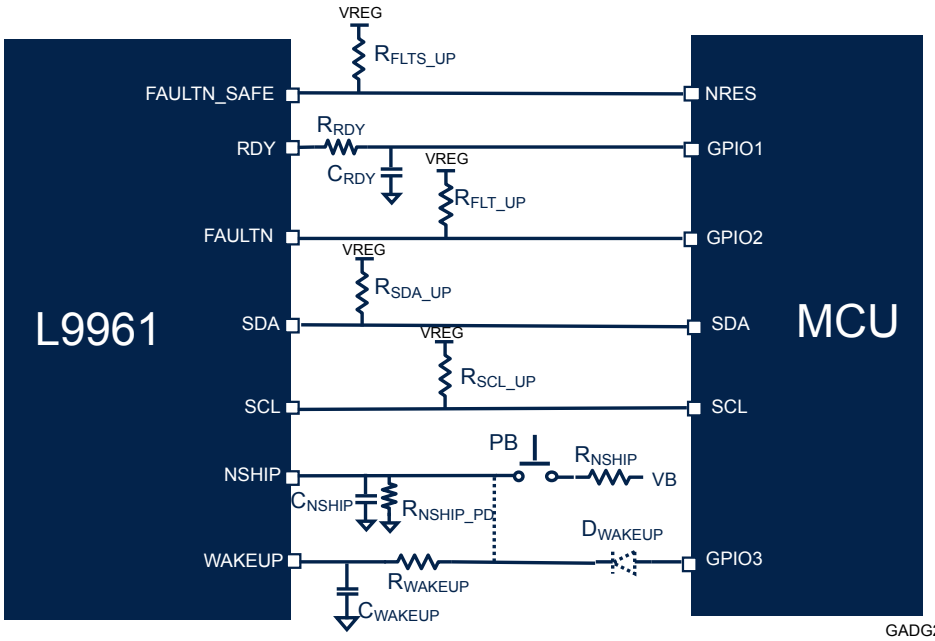
Prerelease product(s)

Table 38. **Typical BOM of fuse circuit**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{FUSE}	2.2	kΩ	10%	1/8 W	Filter the signal coming from redundand protector
C_{FUSE}	2.2	nF	10%	16 V	Filter the signal coming from redundand protector
R_{FUSE_EXT}	2.2	kΩ	10%	1/8 W	Decoupling resistor for wired-OR connection with a secondary protector
M_{FUSE}				40 V	The STL7N6F7 is suggested
D_{ZFUSE}	14	V			Clamp the V_{GS} of the fuse MOSFET
FUSE	15	A		36 V	The ITV4030L2015NR is suggested
R_{PD}	1	MΩ	10%	1/8 W	Pull-down resistor. It is intended to keep the voltage low in standby state.

5.7 Digital IOs

Figure 22. **Typical digital IOs circuit**



GADG220620221406SA

Table 39. **Typical BOM for digital IOs circuit**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{FLTS_UP}	4.7	kΩ	10%	1/10 W	Pull-up resistor
R_{FLT_UP}	4.7	kΩ	10%	1/10 W	Pull-up resistor
R_{SCL_UP}	4.7	kΩ	10%	1/10 W	Pull-up resistor
R_{SDA_UP}	4.7	kΩ	10%	1/10 W	Pull-up resistor
R_{RDY}	100	Ω	10%	1/8 W	LPF resistor for RDY signal. The differential filter cut-off frequency is $f_C = \frac{1}{2\pi R_{RDY} C_{RDY}}$
R_{NSHIP}	10	kΩ	10%	1/10 W	Debouncing filter resistor for pushbutton
R_{NSHIP_PD}	100	kΩ	10%	1/10 W	Pull-down resistor

Prerelease product(s)

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{WAKEUP}	1	kΩ	10%	1/10 W	Debouncing filter resistor for pushbutton
C_{NSHIP}	100	nF	10%	50 V	Debouncing filter capacitor for pushbutton
C_{WAKEUP}	100	nF	10%	50 V	Debouncing filter capacitor for pushbutton
C_{RDY}	100	pF	10%	16 V	LPF capacitor for RDY signal. The filter cut-off frequency is $f_C = \frac{1}{2\pi R_{RDY} C_{RDY}}$
PB					Pushbutton to wakeup L9961 from SHIPMENT - DEEP SLEEP state
D_{WAKEUP}	40	V			Blocking diode

5.8 Charger connection

In case of LS configuration if the charger is hot-plugged (that is with its two terminals not in HiZ condition), the VSC pin needs to be protected against AMR violation. ST recommends the application circuit in Figure 23.

On the contrary, the HS configuration does not require any additional component but requires to connect FET's common drain to Vb in order to feed the CP with the higher voltage between battery stack and battery charger, thus ensuring the rigth overdrive to switch on discharge MOSFET.

Figure 23. Application circuit in LS/HS configuration

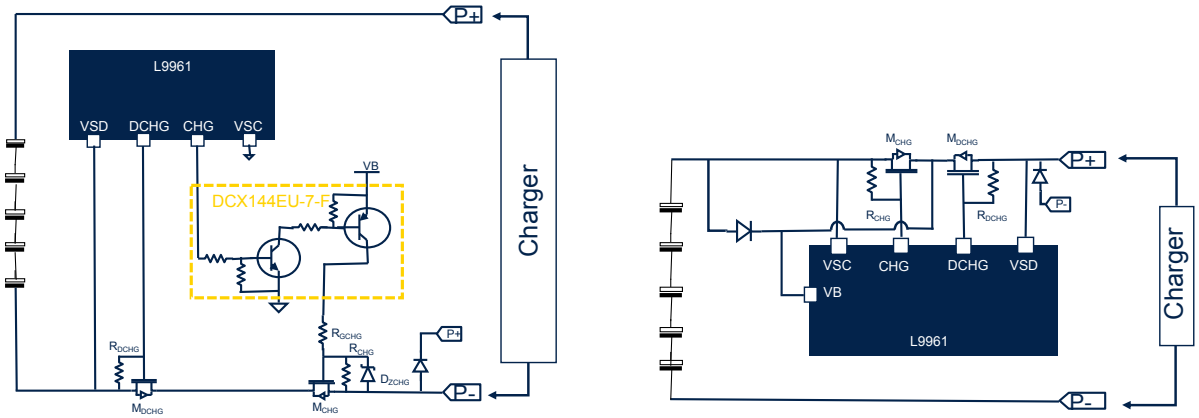


Table 40. BOM in LS configuration when charger is hot-plugged

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{CHG}	220	kΩ	10%	1/10 W	Pull-down resistor
R_{GCHG}	20	kΩ	10%	1/10 W	Limits Zener current
D_{ZCHG}	14	V			Clamps the V_{GS} of the CHG MOSFET
DCX144EU-7-F					Level shifter used to drive the CHG MOSFET. DCX144EU-7-F NPN-PNP transistor switch pair is suggested.

5.9 Safety bypass

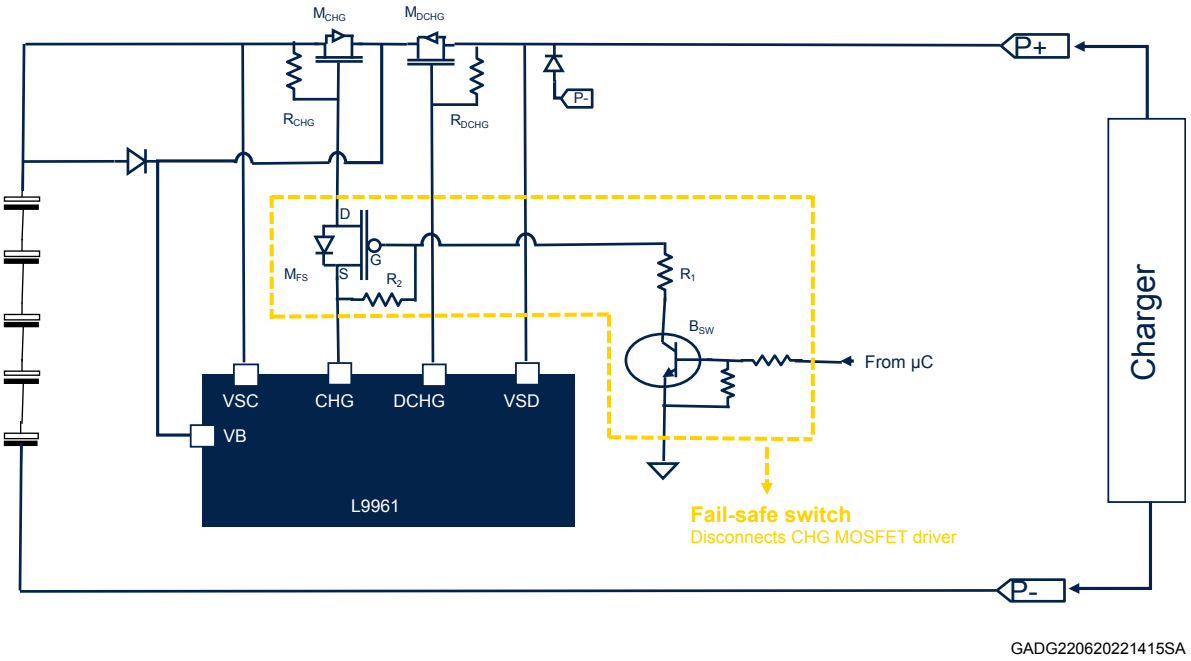
To comply with UL2595 requirements, charging function shall be designed to be inhibited by a safing circuitry independent from L9961. For this reason, ST propose the circuits shown in Figure 25 and Figure 26.

Prerelease product(s)

5.9.1 Safety bypass in HS configuration

During normal operation, the µC shall drive high the NPN base, thus generating a proper Vgs to turning on the PMOS. In case of fault, the µC shall drive low the NPN base in order to ensure the PMOS turning off.

Figure 24. Fail-safe switch in HS configuration



GADG220620221415SA

Table 41. BOM for Fail-safe switch in HS configuration

Components	Value	Unit	Max. tolerance	Rating	Comments
M_{FS}				40 V	Smal signal P-Channel MOSFET used to interrupt the current flowing through CHG pin in case of fault during the charger fase.
R_1	1	MΩ	10%	1/10 W	
R_2	330	kΩ	10%	1/10 W	
B_{sw}				40 V	NPN fail-safe switch driven by MCU. In case of fault the µC drives low the BJT base in order to turns off the P-Channel MOSFET.

Prerelease product(s)

5.9.2 Safety bypass in LS configuration

Figure 25. **Fail-safe switch in LS configuation**

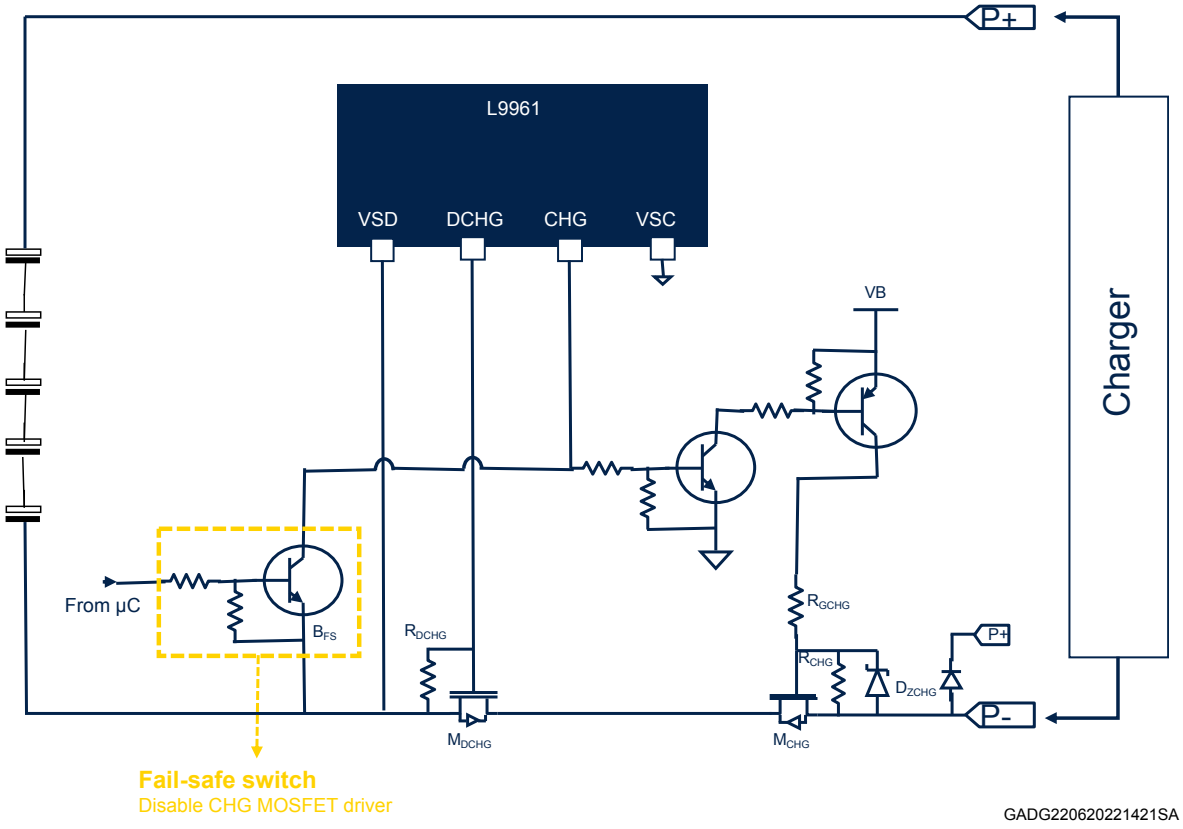


Table 42. **BOM for Fail-safe switch in HS configuration**

Components	Value	Unit	Max. tolerance	Rating	Comments
B_{FS}	-	-	-	40 V	NPN fail-safe switch driven by MCU. It shall be sized in order to sink I_{PU} (charge current source) in case of fault during the charger fase. In case of fault the NPN base shall be driven high by MCU.

Prerelease product(s)

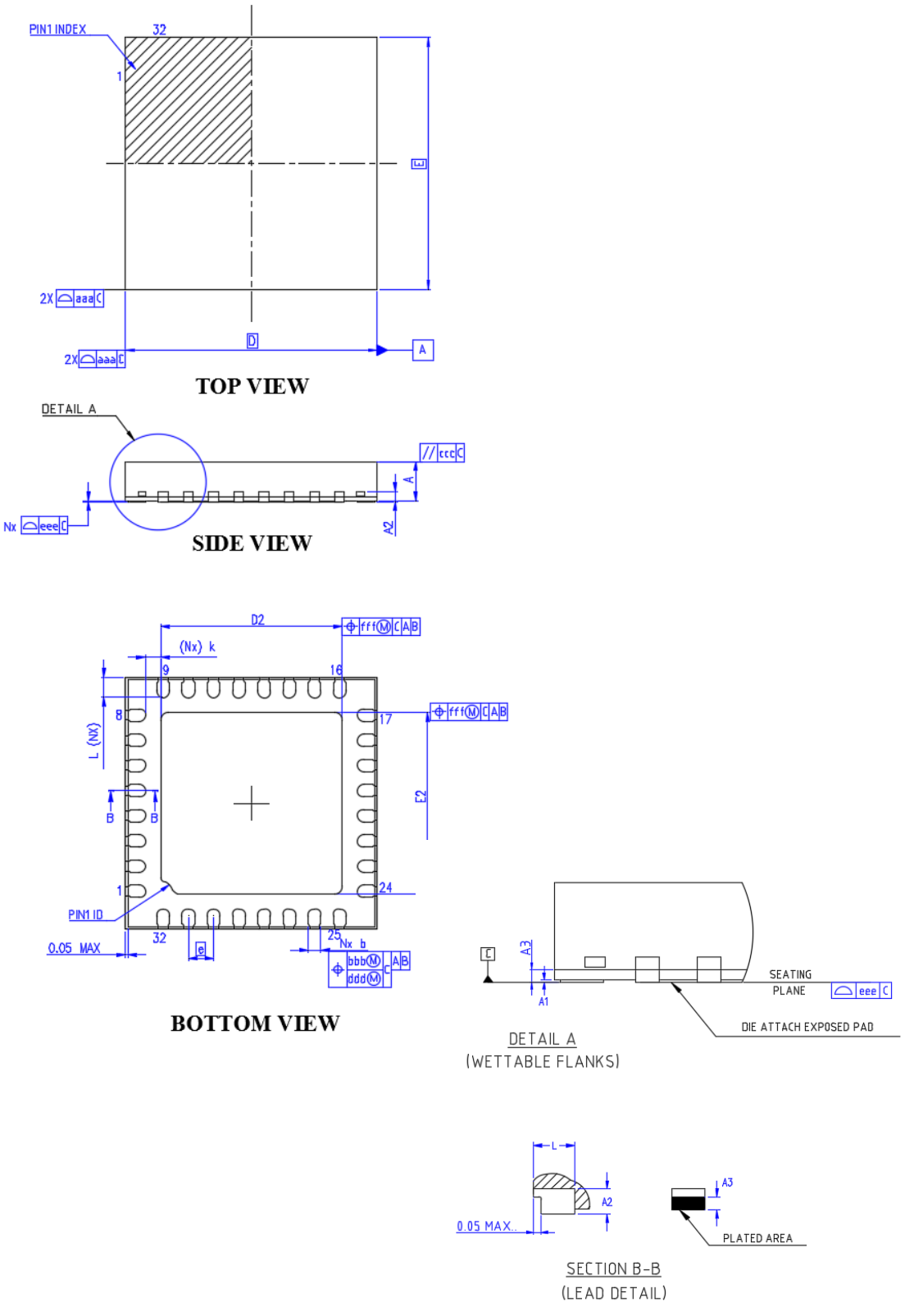
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Prerelease product(s)

6.1 VFQFPN (5x5x1.00 mm) package information

Figure 26. **VFQFPN (5x5x1.00 mm) package outline**



DM00353515_REV2

Prerelease product(s)

Prerelease product(s)

Table 43. VFQFPN (5x5x1.00 mm) package mechanical data

Symbol	Dimensions in mm			
	Min.	Typ.	Max.	Notes
A	0.80	0.90	1.00	12
A1	0.00		0.05	9, 12
A2		0.2 REF.		
A3	0.10			12
b	0.20	0.25	0.30	5, 6, 7, 12, 13
D		5.00 BSC		4, 12
D2	3.50	3.60	3.70	10, 12
e		0.50 BSC		12
E		5.00 BSC		4, 12
E2	3.50	3.60	3.70	10, 12
L	0.30	0.40	0.50	12, 13
k	0.20			
N		32		8

Table 44. Tolerance of form and position

Symbol	Tolerance of form and position	Notes
aaa	0.15	
bbb	1.10	
ccc	0.10	
ddd	0.05	
eee	0.08	
fff	0.10	
Note	1, 12	
Ref		
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
bbb	The tolerance that controls the position of the entire terminal pattern with respect to Datum's A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to Datum's A and B.	
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.

Symbol	Tolerance of form and position	Notes
// // //	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be the datum's defined by the centerlines of the package body.	

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994
2. All Dimensions are in millimeters
3. Terminal A1 identifier and terminal numbering convention shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded, or metalized feature. Optional indicator on bottom surface may be a molded, marked or metallized feature
4. Outlines with "D" and "E" increments less than 0.5 mm should be registered as "stand alone" outlines. These outlines should use as many of the algorithms and dimensions states in the design standard as possible to insure predictability in manufacturing
5. Dimension 'b' / 'b1' / 'b2' applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension 'b' / 'b1' / 'b2' should not be measured in that radius area
6. Inner edge of corner terminals may be chamfered or rounded in order to achieve minimum gap "k". This feature should not affect the terminal width "b" / 'b1' / 'b2', which is measured L/2 from the edge of the package body
7. Exact shape of the leads at the edge of the package is optional
8. "N" is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions
   - Depopulation scheme must be consistent in each quadrant of the package.
   - Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics
9. A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff)
10. Dimension D2 and E2 refer to exposed pad. For exposed pad dimensions see variations table Table 43
11. For tolerance of form and position see Table 44.
12. Critical dimensions:
    - 12.1 A
    - 12.2 A1
    - 12.3 A3
    - 12.4 D & E
    - 12.5 B & L
    - 12.6 e
    - 12.7 D2 & E2
13. Dimensions "b" / 'b1' / 'b2' and "L" are measured at terminal plating surface.
14. For symbols, recommended values and tolerances see table Table 44: (according to package or JEDEC SPEC if registred).

Prerelease product(s)

Revision history

Table 45. **Document revision history**

Date	Revision	Changes
10-Oct-2022	1	Initial release.

Prerelease product(s)

Contents

1 **Pin description and block diagram . . . 3**
1.1 Device pinout . . . 3
1.2 Block diagram . . . 5
2 **Product electrical and thermal ratings . . . 6**
2.1 Operating range (OR) . . . 6
2.2 Absolute maximum ratings (AMR) . . . 7
2.3 ESD ratings . . . 7
2.4 Thermal ratings . . . 8
3 **Functional description . . . 9**
3.1 Device funcional states . . . 9
3.1.1 Shipment - DEEP SLEEP . . . 9
3.1.2 STANDBY . . . 9
3.1.3 NORMAL . . . 10
3.1.4 Electrical parameters . . . 11
3.2 Wakeup sources (NSHIP/WAKEUP) . . . 12
3.2.1 Electrical parameters . . . 12
3.3 VREG LDO . . . 13
3.3.1 Electrical parameters . . . 13
3.4 Voltage conversion routine . . . 14
3.4.1 Cell voltage monitor (Cx) . . . 15
3.4.2 Battery stack monitor (VB) . . . 19
3.4.3 Cell temperature monitor (NTC) . . . 20
3.4.4 Die temperature monitor (T_J) . . . 22
3.4.5 Diagnostics principle . . . 23
3.5 Current conversion routine . . . 25
3.5.1 Current sense ADC (ISENSEP/ISENSEM) . . . 25
3.5.2 Coulomb counting . . . 28
3.5.3 Overcurrent monitor . . . 29
3.5.4 Short-circuit in discharge protection . . . 31
3.6 Cell balancing . . . 32
3.6.1 Electrical parameters . . . 33
3.7 HS/LS pre-drivers (CHG/DCHG/FUSE) . . . 33
3.7.1 Battery pack charge/discharge relays (CHG/DCHG) . . . 33
3.7.2 FUSE pre-driver . . . 34
3.8 Digital IOs (RDY/SDA/SCL/FAULTN_SAFE/FAULTN/OD) . . . 36

Prerelease product(s)

3.8.1 Data-ready interrupt pin (RDY) . . . 36
3.8.2 Fault interrupt pin (FAULTN) . . . 36
3.8.3 MCU emergency reset (FAULTN_SAFE) . . . 38
3.8.4 Electrical parameters . . . 38
3.9 I2C communication interface . . . 38
3.9.1 Clock polarity . . . 39
3.9.2 START/STOP conditions . . . 39
3.9.3 ACK/NACK . . . 40
3.10 I2C protocol layer . . . 40
3.10.1 Addressing and R/ $\overline{W}$ bit . . . 40
3.10.2 CRC . . . 40
3.10.3 Single read/block read . . . 41
3.10.4 Single WRITE/block WRITE . . . 41
3.10.5 Electrical parameters . . . 42
3.11 Non-volatile memory (NVM) . . . 43
3.11.1 Electrical parameters . . . 44
4 Device register map . . . 45
5 Application information . . . 46
5.1 Power supply circuit . . . 46
5.2 Cell voltage sensing and balancing circuit . . . 47
5.3 Current sense circuit . . . 47
5.4 NTC analog front end . . . 48
5.5 HS/LS pre-drivers circuit . . . 49
5.6 Fuse circuit . . . 49
5.7 Digital IOs . . . 50
5.8 Charger connection . . . 51
5.9 Safety bypass . . . 51
5.9.1 Safety bypass in HS configuration . . . 52
5.9.2 Safety bypass in LS configuration . . . 53
6 Package information . . . 54
6.1 VFQFPN (5x5x1.00 mm) package information . . . 55
Revision history . . . 58

Prerelease product(s)

List of tables

Table 1. Device pinout . . . 3
Table 2. Operating ranges . . . 6
Table 3. Absolute maximum ratings . . . 7
Table 4. ESD protection . . . 7
Table 5. Thermal ratings . . . 8
Table 6. L9961 operating states electrical parameters . . . 11
Table 7. VREG electrical parameters . . . 12
Table 8. VREG electrical parameters . . . 13
Table 9. Voltage conversion routine execution parameters . . . 15
Table 10. Cell voltage monitor diagnostics . . . 15
Table 11. Cell voltage monitor electrical parameters . . . 17
Table 12. Battery stack monitor diagnostics . . . 19
Table 13. Battery stack monitor external parameters . . . 20
Table 14. NTC temperature monitor diagnostics . . . 21
Table 15. NTC measurement parameters . . . 22
Table 16. Die temperature monitor diagnostics . . . 22
Table 17. Die temperature monitor electrical parameters . . . 23
Table 18. Current sense ADC electrical parameters . . . 26
Table 19. Coulomb counter electrical parameters . . . 28
Table 20. Overcurrent diagnostics . . . 29
Table 21. Overcurrent electrical parameters . . . 30
Table 22. Short-circuit in discharge diagnostics . . . 31
Table 23. Short-circuit in discharge electrical parameters . . . 32
Table 24. Balancing electrical parameters . . . 33
Table 25. CHG/DCHG pre-driver electrical parameter . . . 34
Table 26. Coulomb counter electrical parameters . . . 35
Table 27. RDY Interrupt pin electrical parameters . . . 36
Table 28. Digital output electrical characteristics . . . 37
Table 29. Digital output electrical characteristics . . . 38
Table 30. Digital output electrical characteristics . . . 38
Table 31. I2C electrical parameters . . . 42
Table 32. NVM electrical parameters . . . 44
Table 33. Recommended power supply components . . . 46
Table 34. Typical BOM for cell voltage sensing and balancing circuit . . . 47
Table 35. Typical current sense BOM . . . 47
Table 36. NTC analog front end BOM . . . 48
Table 37. Typical HS/LS Pre-Drivers BOM . . . 49
Table 38. Typical BOM of fuse circuit . . . 50
Table 39. Typical BOM for digital IOs circuit . . . 50
Table 40. BOM in LS configuration when charger is hot-plugged . . . 51
Table 41. BOM for Fail-safe switch in HS configuration . . . 52
Table 42. BOM for Fail-safe switch in HS configuration . . . 53
Table 43. VFQFPN (5x5x1.00 mm) package mechanical data . . . 56
Table 44. Tolerance of form and position . . . 56
Table 45. Document revision history . . . 58

Prerelease product(s)

List of figures

Figure 1. Block diagram . . . 5
Figure 2. Device FSM . . . 9
Figure 3. Timing diagram: transition from NORMAL to STANDBY upon GO2STBY command . . . 10
Figure 4. Timing diagram: transition from STANDBY to NORMAL upon WAKEUP detection . . . 11
Figure 5. Voltage conversion routine steps . . . 15
Figure 6. Correct management of the task execution periodicity . . . 15
Figure 7. Example of cell UV detection . . . 24
Figure 8. Current sense ADC total conversion error . . . 26
Figure 9. Balancing timing diagram . . . 33
Figure 10. RDY pulse generation upon voltage conversion routine task termination . . . 36
Figure 11. I2C clock polarity . . . 39
Figure 12. I2C START/STOP conditions . . . 39
Figure 13. I2C generic READ operation . . . 41
Figure 14. I2C generic WRITE operation . . . 41
Figure 15. Timing on the I2C bus . . . 43
Figure 16. Power supply circuit . . . 46
Figure 17. Cell voltage sensing and balancing circuit . . . 47
Figure 18. Current sense circuit . . . 47
Figure 19. NTC measurement circuit . . . 48
Figure 20. HS/LS pre-drivers circuit . . . 49
Figure 21. Fuse circuit . . . 49
Figure 22. Typical digital IOs circuit . . . 50
Figure 23. Application circuit in LS/HS configuration . . . 51
Figure 24. Fail-safe switch in HS configuration . . . 52
Figure 25. Fail-safe switch in LS configuation . . . 53
Figure 26. VFQFPN (5x5x1.00 mm) package outline . . . 55

Prerelease product(s)

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved

Prerelease product(s)